

ICM1115/D, ICM1115/W Stepper Motor Quartz Clock



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GENERAL DESCRIPTION

The ICM1115 is a single battery analog quartz clock circuit intended for use with bipolar stepper motors and fabricated using Intersil's low voltage metal gate CMOS process. The circuit consists of a divider chain, output gating, output buffers and an oscillator which, when using the specified 4.19 MHz crystal and capacitors, provides excellent stability. The high frequency portion of the divider chain consists of dynamic dividers, while the remainder are static. The dynamic dividers feature low power consumption and operating voltage, but limit low frequency operation. The large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during an output pulse, resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester. Motor drive will continue 1 sec. after RESET is released.

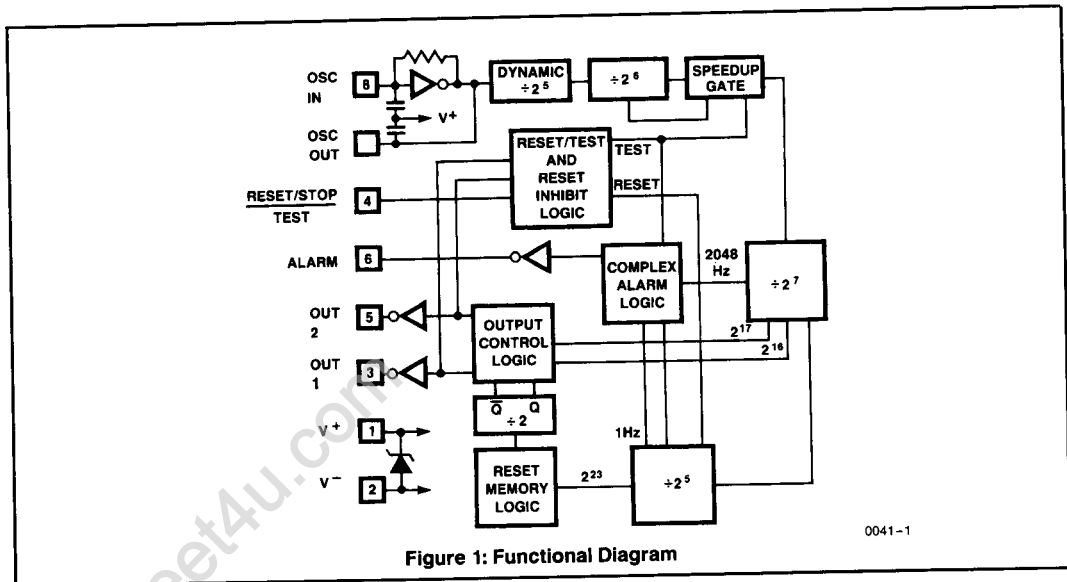
FEATURES

- Single Battery Operation
- Very Low Current—Typically 40 μA at 4.19 MHz
- Reset or Stop Function, Inhibited During Output
- Extremely Low Output Saturation Resistance: Less Than 100 Ω

Device	Motor Output	Alarm Output
ICM1115	0.5 Hz Square Wave	64 Hz Tone

ORDERING INFORMATION

Part Number	Temperature	Form
ICM1115A/D	+ 25°C	Dice
ICM1115B/D	+ 25°C	Dice
ICM1115A/W	+ 25°C	Wafer
ICM1115B/W	+ 25°C	Wafer



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NOTE: All typical values have been characterized but are not tested.

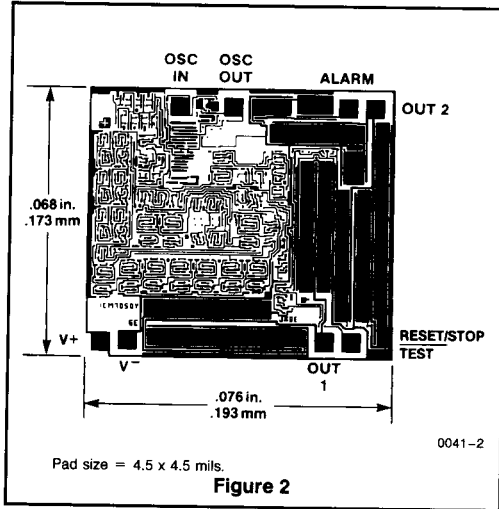
ABSOLUTE MAXIMUM RATINGS

Supply Voltage3V
Output Voltage (Note 1)Equal to but never
Input Voltage (Note 1)exceeding the supply voltage
Storage Temperature+ 25°C
Operating Temperature25°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1 mA.

CHIP TOPOGRAPHY



ELECTRICAL CHARACTERISTICS

V+ = 1.5V, fosc = 4,194,304 Hz, TA = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current (Note 2) ICM115B ICM115A	I+	No Load		40	60	μA
				80	120	
Operating Voltage	V+		1.2		1.8	V
Total Output Saturation Resistance	ROUT	IL = 4 mA		70	100	Ω
Alarm Saturation Resistance	RAL (on)	P, IL = 1 mA		400	700	Ω
		N, IL = 2 mA		100	400	Ω
Oscillator Stability	fstab	1.2 ≤ V+ ≤ 1.6		1		ppm
Oscillator Start-Up Time	tstart	V+ = 1.2V			1.0	sec
Oscillator Transconductance (Note 2)	gm	ICM115A	150	400		μmho
		ICM115B	75	200		

NOTE 2: Two options are available with the ICM115. The ICM115B is designed to be used with crystals whose load capacitance is 12 pF or less. Using input and output capacitors of 15 pF to 20 pF, this device will provide stable operation at very low supply current. For applications with larger load capacitance (15 pF to 20 pF), the ICM115A ensures that an increased oscillator current is available to guarantee startup and operation over the voltage range. Using input and output capacitors of 30 pF to 40 pF, the ICM115A will offer good stability at a supply current approximately twice that of the ICM115B.

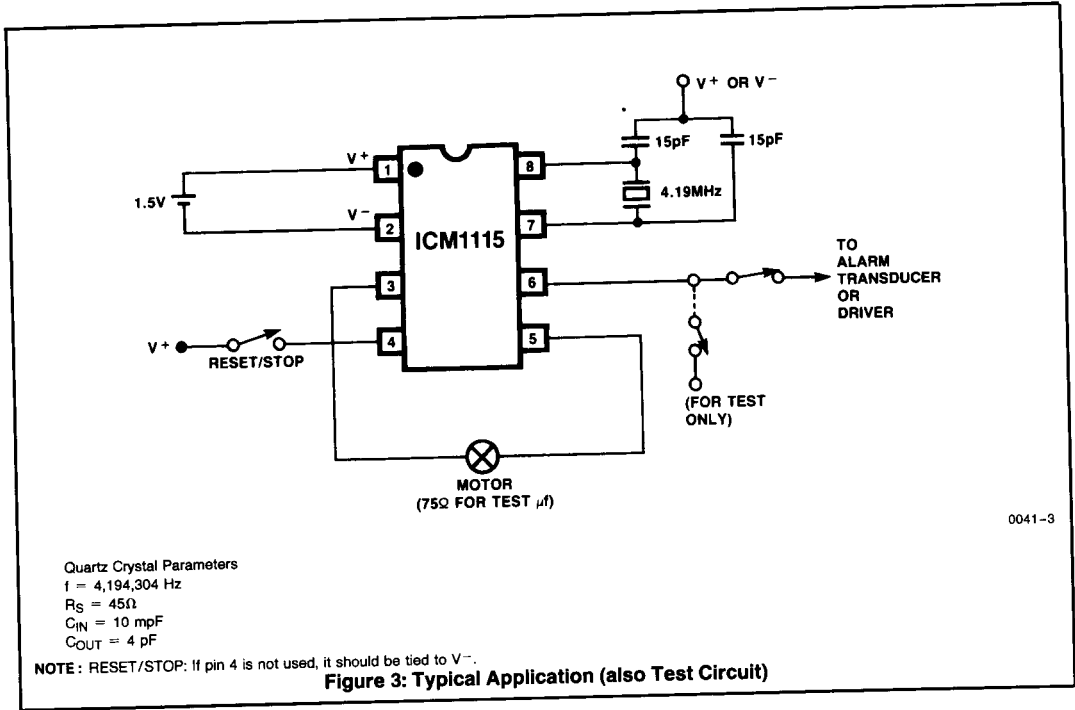
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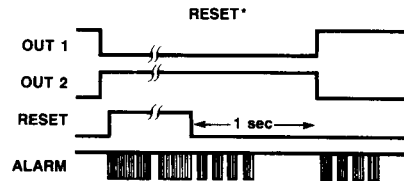
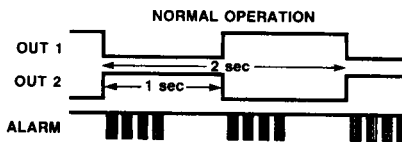
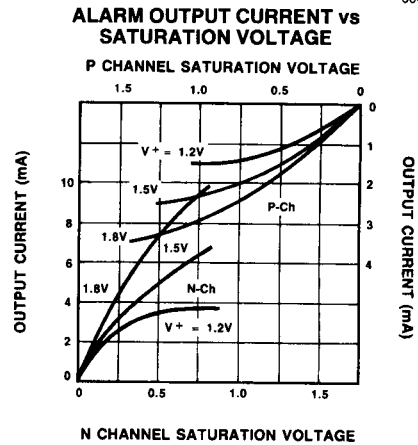
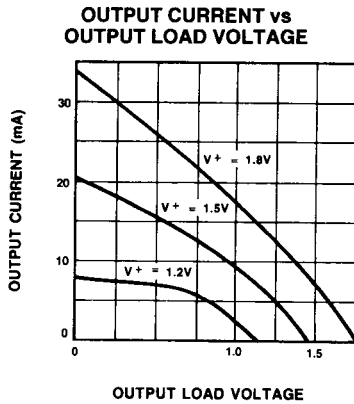
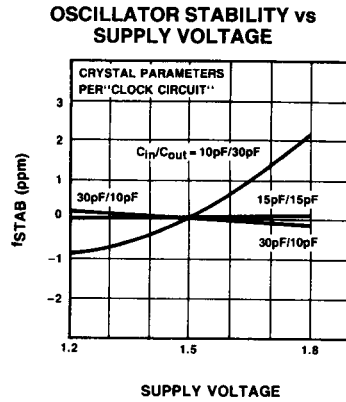
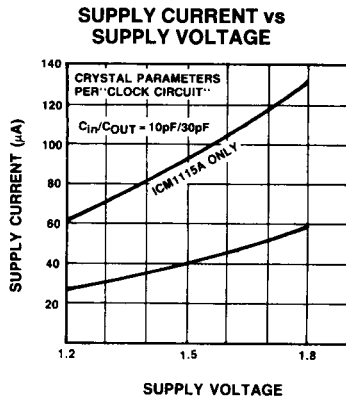
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TYPICAL PERFORMANCE CHARACTERISTICS

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*Shown during OUTput 1; exchange OUTput 1 and OUTput 2 for opposite case.

Figure 4: Output Waveforms

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