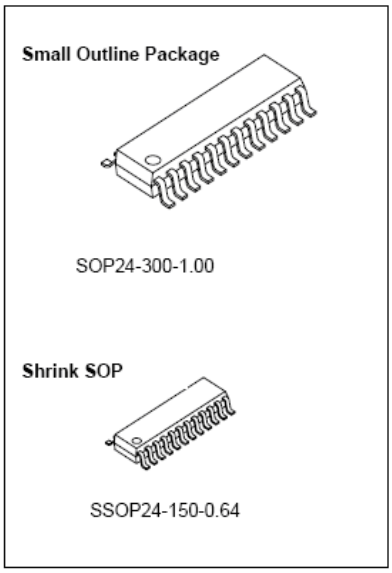
Description

The ICN2024 is a LED module and display driver IC with 16-constant current output driving capability. The 16-output current can be adjusted by using different external resistors, which gives users flexibility in controlling the light intensity of LEDs.

The ICN2024 contains 16-bit shift registers and latches which convert serial input data into parallel output format, therefore, the ON or OFF of LED can be controlled by an external enable signal $\overline{OE}$. And ICN2024 exploits current presision controlling technology, which makes error between ICs less than ±3%, and error between channels less than ±1.5%. At ICN2024 output stage, 16-regulated output ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of forward voltage(V_F) variations. The high clock frequency, 30MHz, also satisfies the system requirements of high volume data transmission.

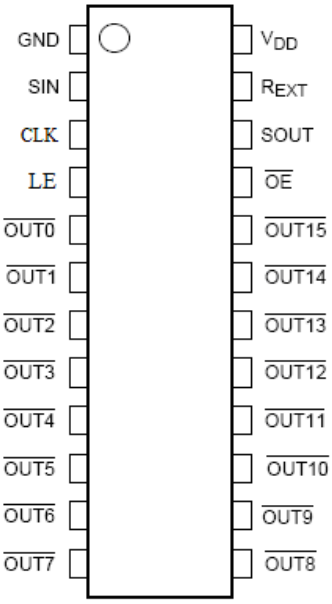


Features

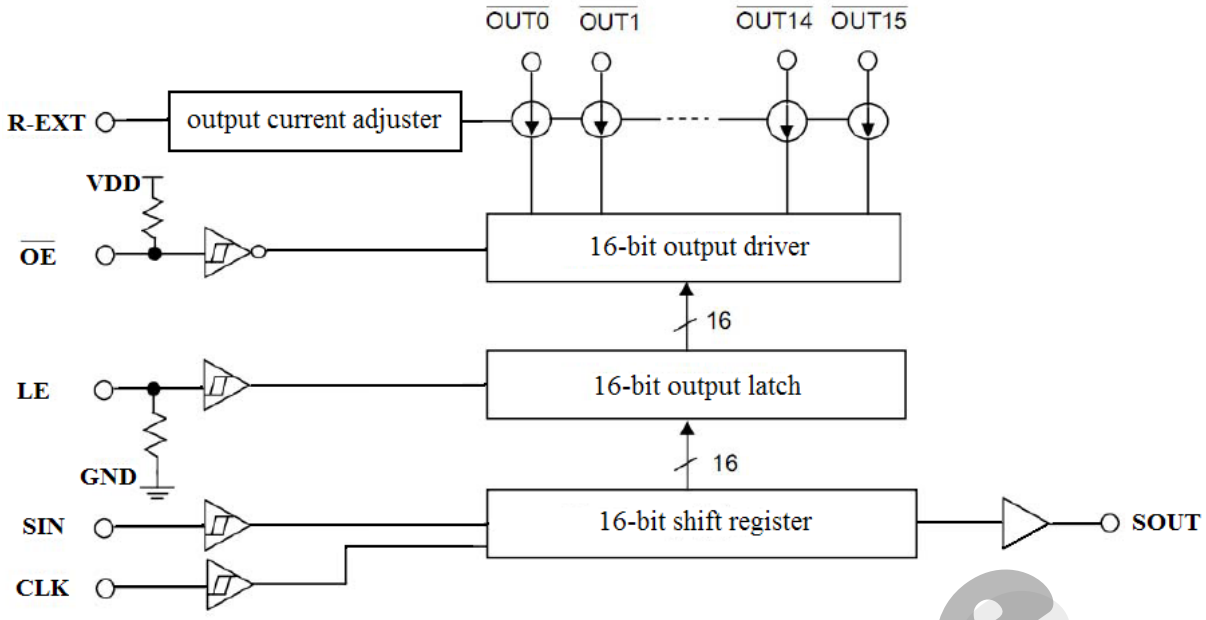
- ✧ 16 constant-current output channels
- ✧ Output current setting range:
  3~45mA×16@V_{DD}=5V constant current output
  3~30mA×16@V_{DD}=3.3V constant current output
- ✧ Current accuracy
  Between channel:<± 1.5%
  Between ICs:<± 3%
- ✧ Fast response of output current, $\overline{OE}$ (min):150ns@V_{DD}=5V
- ✧ Output current adjusted through an external resistor
- ✧ I/O:Schmitt trigger input
- ✧ Data transfer frequency:f_{MAX}=30MHz(Max)
- ✧ Power supply voltage:V_{DD}=3.3～5V

Pin Description

Pin Name	Function
GND	Ground terminal
SIN	Serial-data input to the shift register
CLK	Clock input terminal for data shift on rising edge
LE	Data input terminal, LE high level, serial data is transferred to the output latch; LE low level, the data is latched
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminal
$\overline{OE}$	Output enable terminal, $\overline{OE}$ high level, all output drivers are enabled; $\overline{OE}$ low level, all output drivers are turned OFF
SOUT	Serial-data output to the following SIN of next driver IC
R-EXT	Connect an external resistor for setting up output current for all output channels
VDD	3.3V/5Vsupply voltage terminal

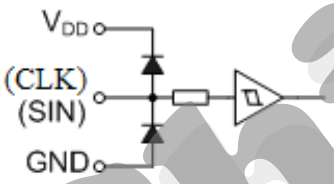


Block Diagram

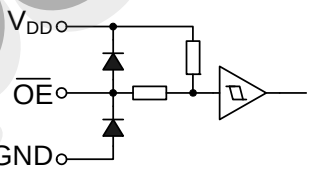


I/O equivalent Circuits

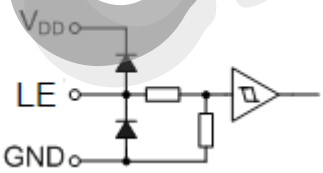
1. CLK, SIN



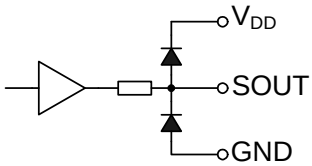
2. $\overline{OE}$



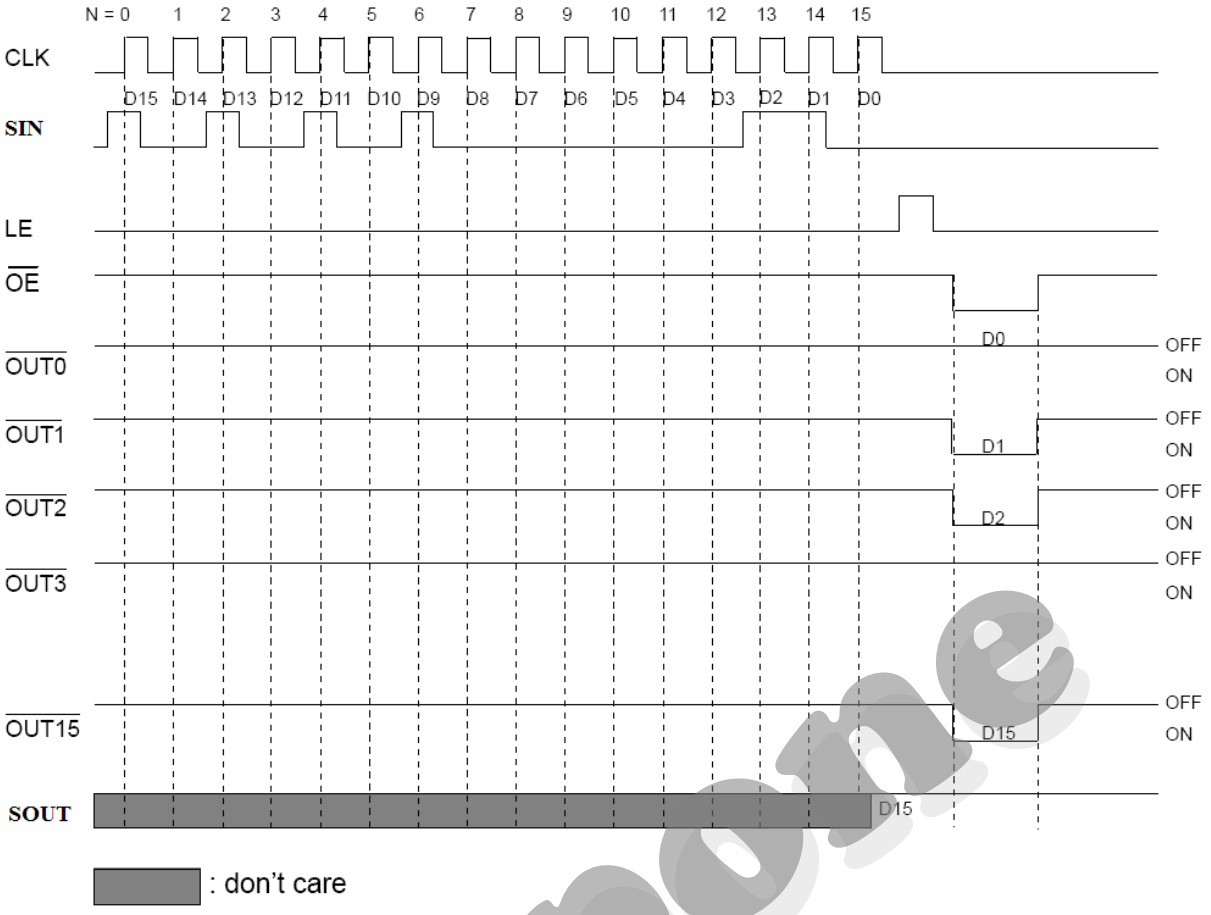
3. LE



4.SOUT



Timing Diagram



Note 1：Keep the LE pin is set to L to enable the latch circuit to hold data. When the LE pin is set to H, the latch circuit does not hold data. The data will instead pass onto output. When the $\overline{OE}$ pin is set to L, the $\overline{OUT0}$ to $\overline{OUT15}$ output pins will go ON and OFF in response to the data. In addtion, when the $\overline{OE}$ pin is set to H all the output pins will be forced OFF regardless of the data.

Truth Table

CLK	LE	$\overline{OE}$	SIN	$\overline{OUT0}$ ⋯ $\overline{OUT7}$ ⋯ $\overline{OUT15}$	SOUT
↑	H	L	D_n	D_n … D_{n-7} … D_{n-15}	D_{n-15}
↑	L	L	D_{n+1}	NO change	D_{n-14}
↑	H	L	D_{n+2}	D_{n+2} … D_{n-5} … D_{n-13}	D_{n-13}
↓	×	L	D_{n+3}	D_{n+2} … D_{n-5} … D_{n-13}	D_{n-13}
↓	×	H	D_{n+3}	OFF	D_{n-13}

Maximum Ratings(T_a =25℃)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Output Current		I_O	45	mA
Input Voltage		V_{IN}	-0.4~V_{DD}+0.4	V
Clock Frequency		F_{CLK}	30	MHz
GND Terminal Current		I_{GND}	+1000	mA
Power Dissipation (On PCB，25℃)	CSA-type	P_D	1.9	W
	CSB-type		1.4	
Thermal Resistance	CSA-type	$R_{th(j-a)}$	66.66	℃/W
	CSB-type		88.39	
Operating Temperature		T_{opr}	-40 ~ 85	℃
Storage Temperature		T_{stg}	-55 ~ 150	℃

DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	-	4.5	5	5.5	V
Output Voltage when ON	$V_{O(ON)}$	$\overline{OUTn}$	0.7	-	4	V
High leve logic input voltage	V_{IH}	-	0.7*V_{DD}	-	V_{DD}	V
High leve logic input voltage	V_{IL}	-	GND	-	0.3*V_{DD}	V
SOUT high level output Current	I_{OH}	V_{DD}=5V	-	-	-1	mA
SOUT low level output Current	I_{OL}	V_{DD}=5V	-	-	1	mA
Constant current output	I_O	$\overline{OUTn}$	3	-	45	mA

Transition Items (Unless otherwise specified, V_{DD}==4.5~5.5V，T_a =-40℃~85℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	f_{CLK}	6	-	-	-	30	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	-	-	ns
Latch pulse width	t_{wLE}	6	LE=H	20	-	-	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}$ =H or L，R_{EXT}=890Ω	150	-	-	ns
Hold time	t_{HOLD1}	6	-	5	-	-	ns
	t_{HOLD2}	6	-	5	-	-	ns
Setup time	t_{SETUP1}	6	-	5	-	-	ns
	t_{SETUP2}	6	-	5	-	-	ns
Maximum clock rise time	t_r	6		-	-	500	ns
Maximum clock fall time	t_f	6		-	-	500	ns

Electrical Characteristics (Unless otherwise specified, V_{DD} =4.5~5.5V，T_a =25℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	-	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	-	-	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	-	-	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	-	-	-1	μA
Power supply current	I_{DD1}	4	Rext=open, OUT off	-	2.5	5.0	mA
	I_{DD2}	4	Rext=1240，OUT off	-	4.5	7.0	mA
	I_{DD3}	4	Rext=620，OUT off	-	6	9.0	mA
	I_{DD4}	4	Rext=1240，OUT on	-	5.2	8.5	mA
	I_{DD5}	4	Rext=620，OUT on	-	6.5	9.5	mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.24kΩ	-	15	-	mA
	I_{O2}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=620Ω	-	30	-	mA
Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.24 kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	-	±1	±3	mA

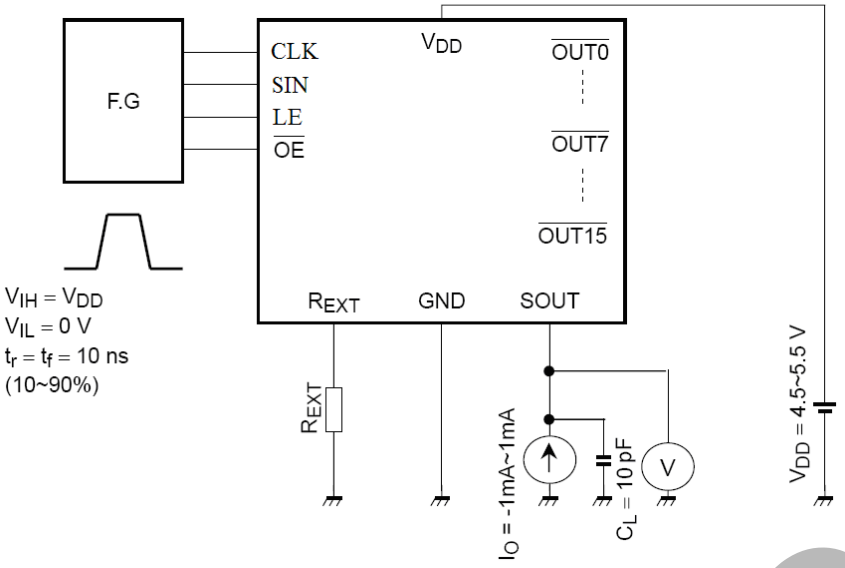
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24 kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	-	±1	-	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24 kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	-	±0.1		%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	kΩ

Switching Characteristics (Unless otherwise specified, T_a =25℃, V_{DD} =5.0V)

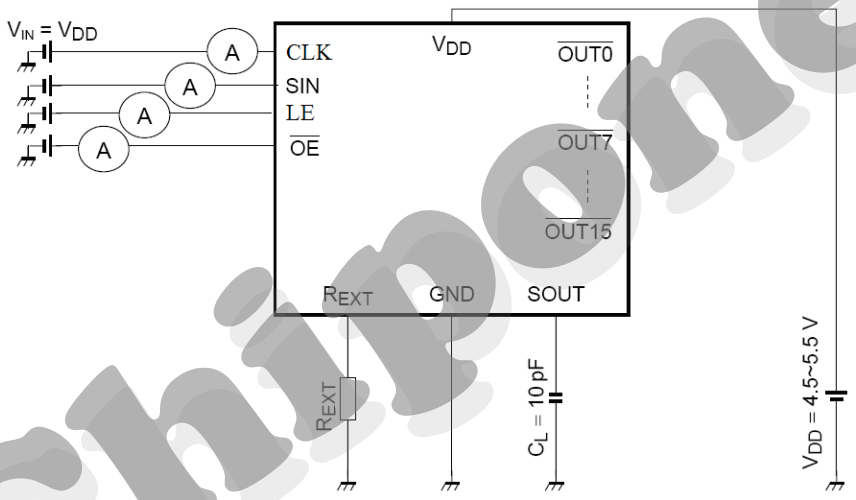
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	CLK- $\overline{OUT0}$	t_{pLH1}	6	LE=H, $\overline{OE}$ =L	-	80	100	ns
	LE- $\overline{OUT0}$	t_{pLH2}	6	$\overline{OE}$ =L	-	80	100	
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	6	LE=H	-	115	135	
	CLK-SOUT	t_{pLH}	6	-	-	20	40	
	CLK- $\overline{OUT0}$	t_{pHL1}	6	LE=H, $\overline{OE}$ =L	-	80	100	
	LE- $\overline{OUT0}$	t_{pHL2}	6	$\overline{OE}$ =L	-	80	100	
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}	6	LE=H	-	115	135	
	CLK-SOUT	t_{pHL}	6	-	-	20	40	
Output rise time		t_{or}	6	10~90% of voltage waveform	-	10	15	ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	30	50	ns

Test Circuit

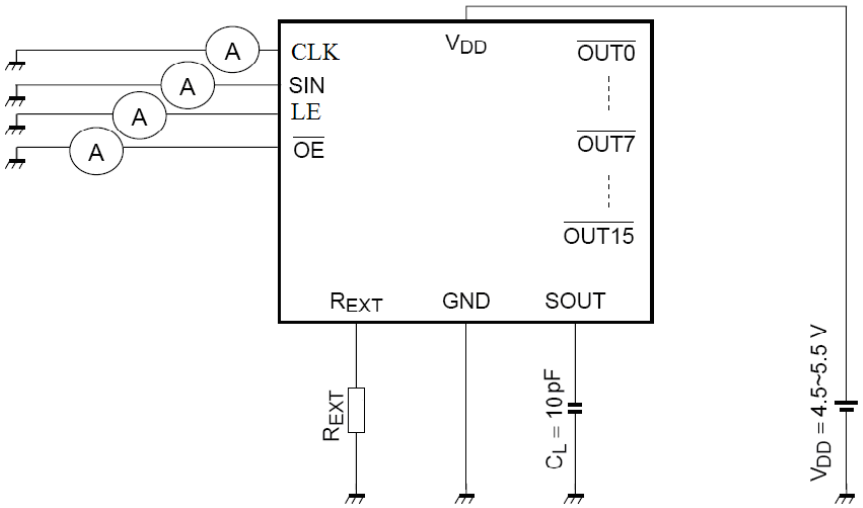
Test Circuit1: High level logic input voltage/Low level logic input voltage



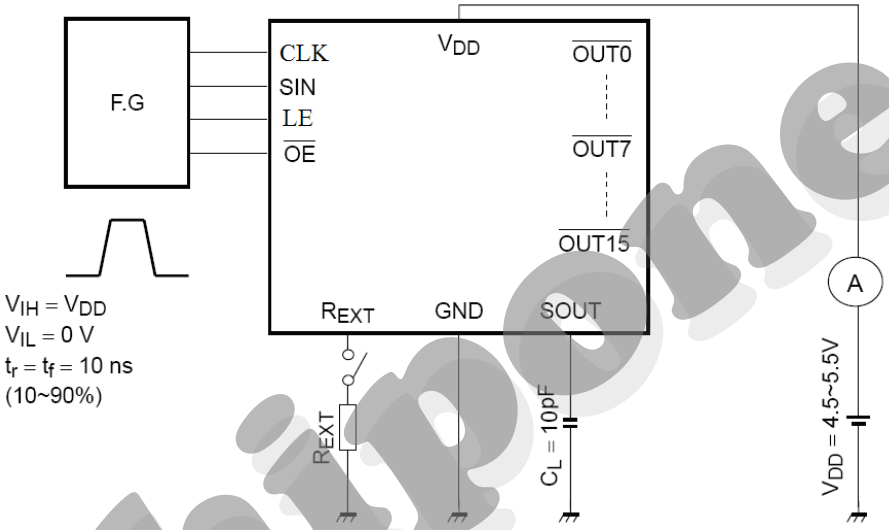
Test Circuit2: High level logic input current/Pull-down resistor



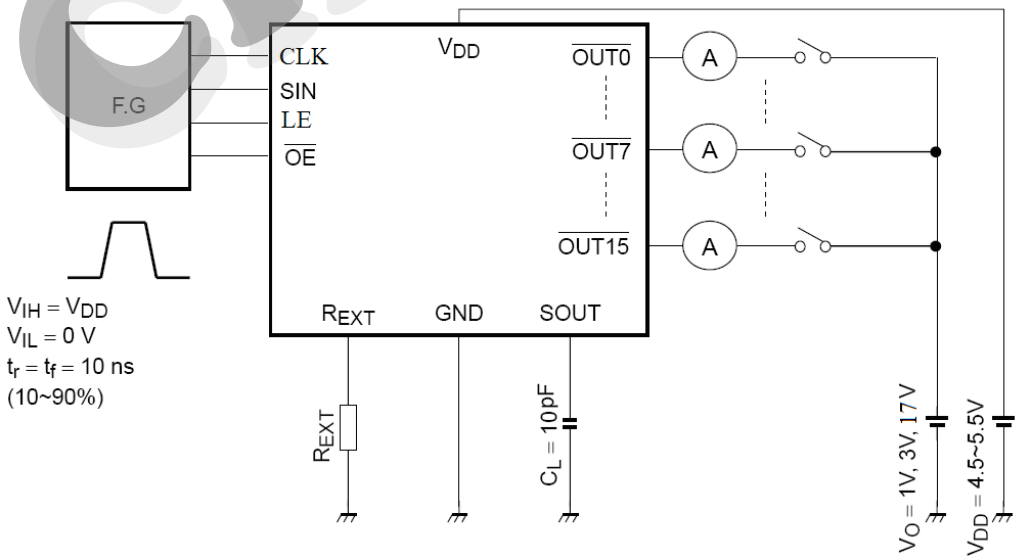
Test Circuit3：Low level logic input current/Pull-up resistor



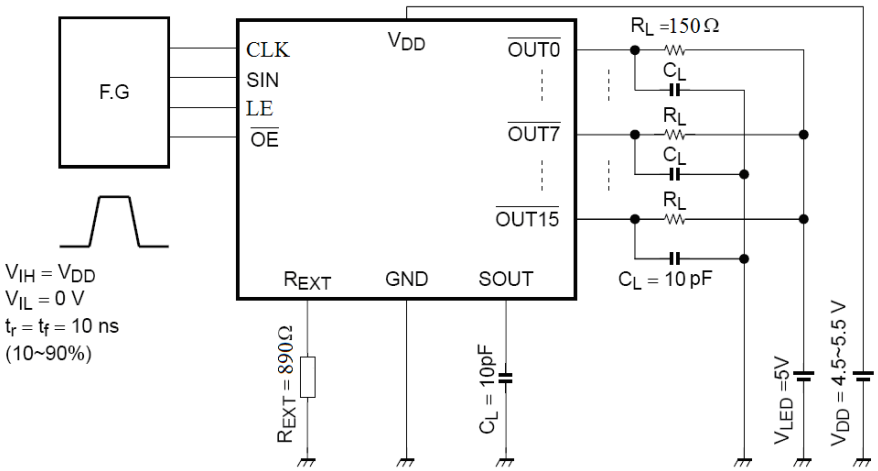
Test Circuit4: Power supply current



Test Circuit5: Constant current output/Output OFF leak current/Constant current error
Constant current power supply voltage regulation/Constant current output voltage regulation

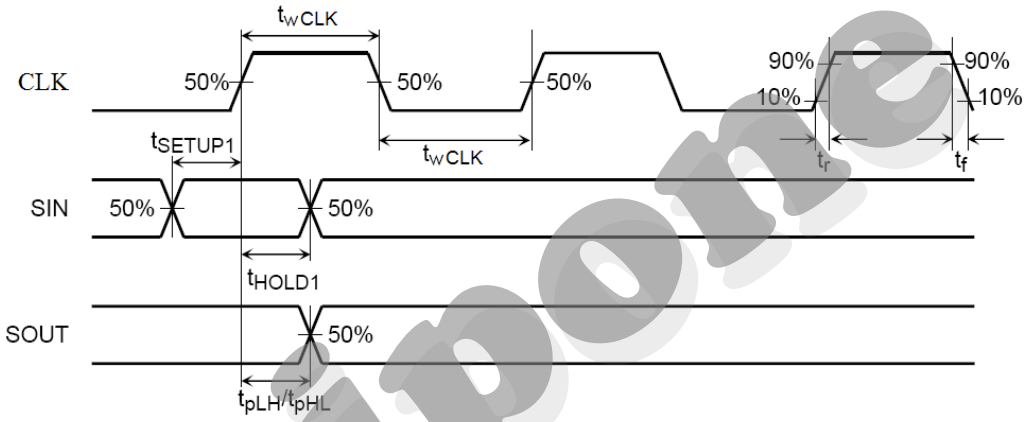


Test Circuit6: Switching Characteristics

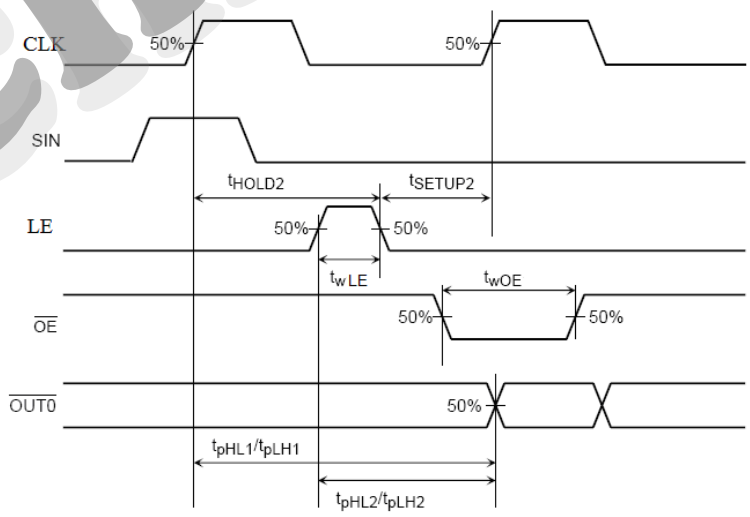


Timing Waveforms

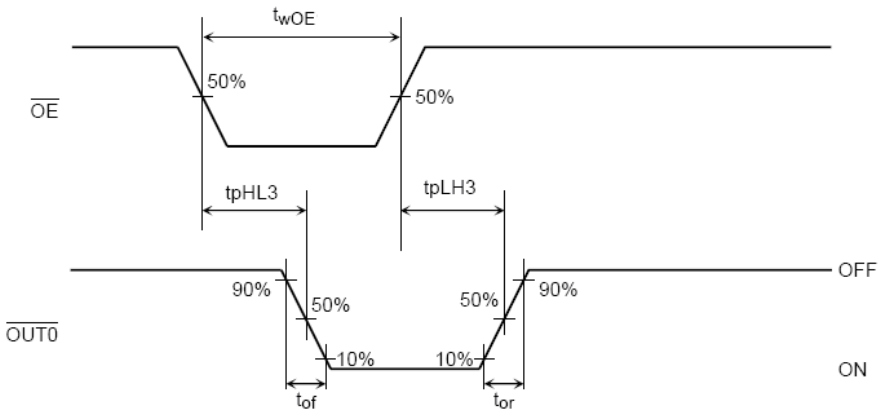
1. CLK, SIN, SOUT



2. CLK, SIN, LE, $\overline{OE}$, $\overline{OUT0}$



3. $\overline{OUT0}$

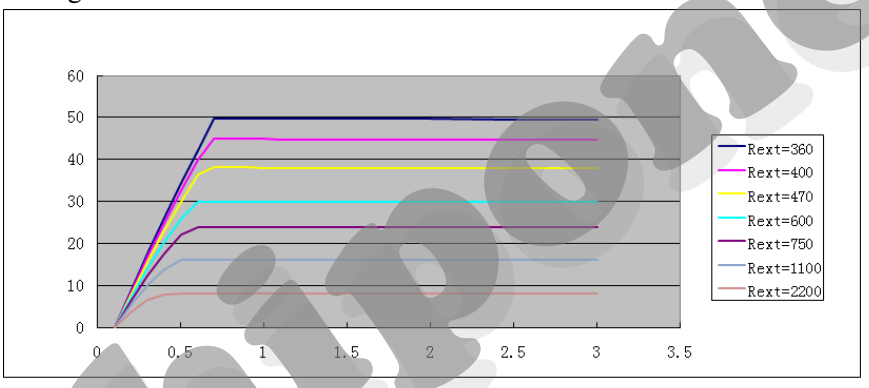


Application information

ICN2024 exploits current presision controlling technology，and provides nearly no variations in current from channel and from ICs.

1) The maximum current variation between channels is less than±1%，and that between ICs<±3%.

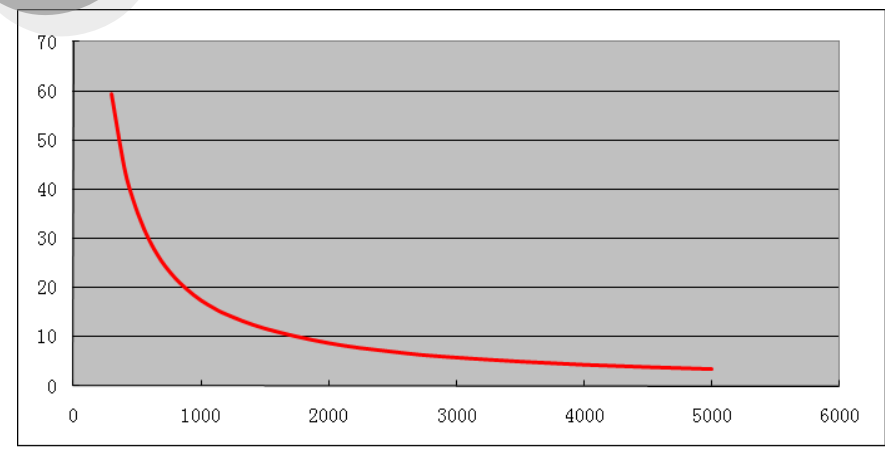
2) The current characteristic of output stage is flat, and can be kept constant regardless of the variations of LED forward voltage.



Adjusting Output Current

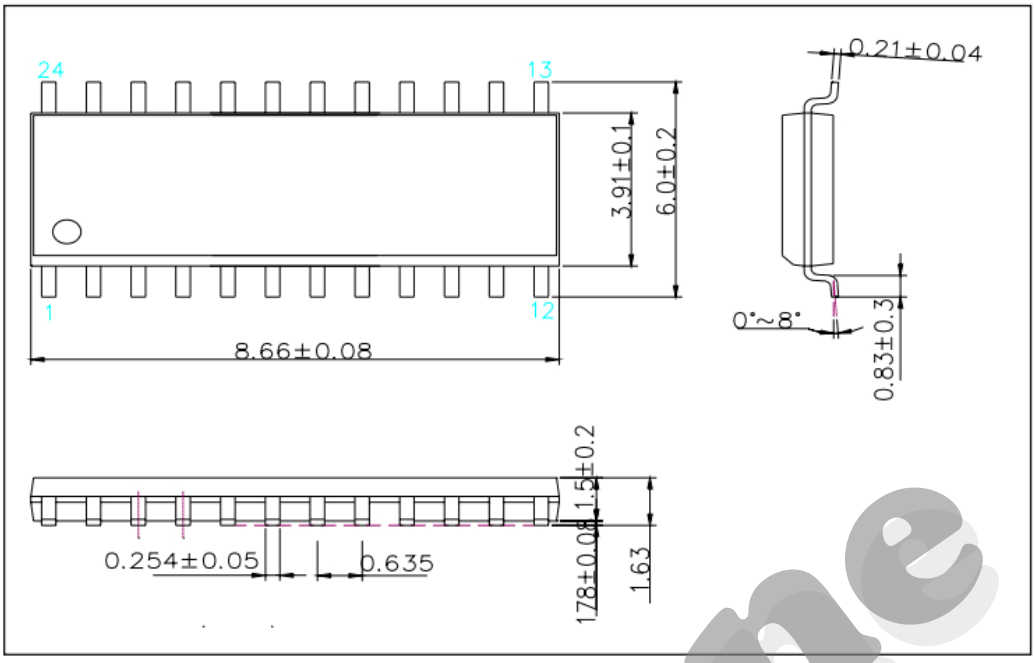
The output current of ICN2024 each channel(Iout) is set by an external resistor, Rext. The relationship equation between Iout and Rext is

V_{R-EXT}=1.24V； Iout=(V_{R-EXT}/Rext)*15

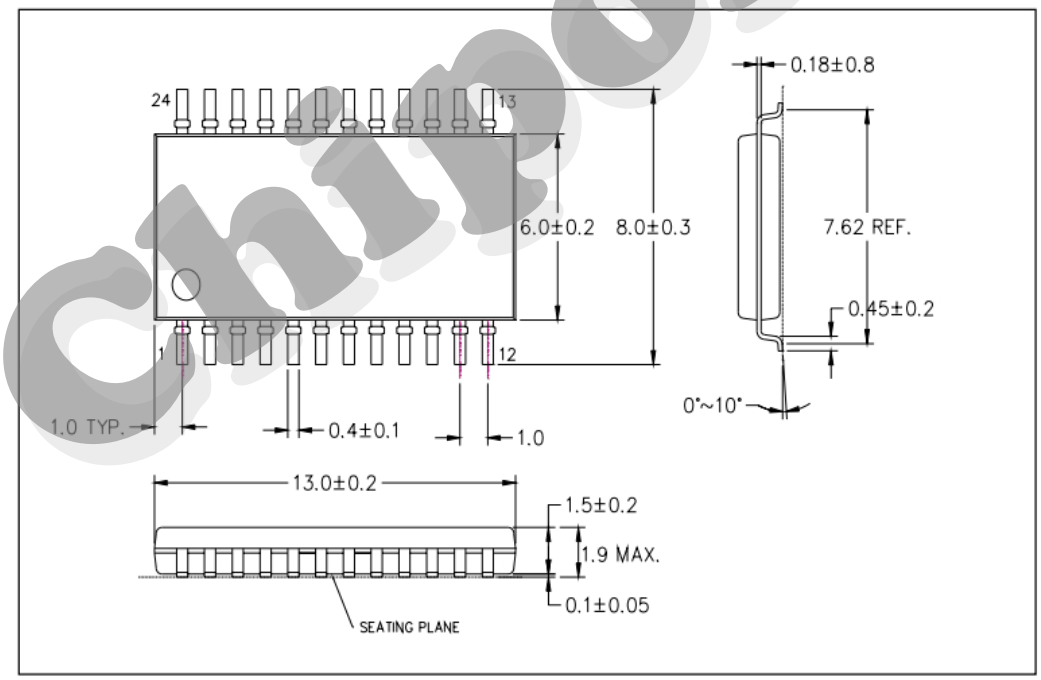


Package Outline

(1) SSOP24-P-150-0.65



(2) SSOP24-P-300-1.0



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