CHIPONE
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ICNL9706 a-Si TFT Mobile Display Driver IC Specifications

ICNL9706

Specification Version

Model No ：	*ICNL9706*
Document Version ：	*V0.7*
Release Date ：	*2017/10/26*

Chipone Technology (Beijing) Co.,Ltd.

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1、Features

1. Single chip WXGA a-Si TFT LCD Controller/driver without Display RAM.
2. Panel driving:
   - 2402 source pads.
   - CGOUTL 1~22 and CGOUTR 1~22 pads for GIP timings control.
   - 1-dot / 2-dot / 4-dot / 8-dot / Zig-Zag / Column inversion.
   - DC **VCOM** voltage generator and adjustment.
3. Display resolution:
   - 800RGB x (480+4 x NL)
   - 720RGB x (480+4 x NL)
4. Display color modes
   - Full color mode 16.7M colors
   - Reduce color mode : 262K colors
5. Output voltage level
   - Positive gate driver voltage range for **VGH**: 10V to 20V
   - Negative gate driver voltage range for **VGL**: -7.0V to -16V
   - Positive gamma high voltage range for **VSPR**: 3.0V to 6.0V
   - Negative gamma low voltage range for **VSNR**: -3.0V to -6.0V
   - GIP timings control voltage range for **VGH** to **VGL**.
   - Common electrode voltage range for **VCOM**: -0.3V to -2.2V.
   - Negative level shift voltage range for **VCL** : -1xVCI
6. Input voltage level
   - Logic and interface power supply (**IOVCC**): 1.65V to 3.3V.
   - Analog power supply (**VCI**): 2.5V to 3.3V
   - Positive source driver power supply (**VSP**): 4.5V to 6.5V
   - Negative source driver power supply (**VSN**) : -4.5V to -6.5V
   - OTP programming voltage (**VPP**): 8.5V
7. Interface
   - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0)

8. On-chip functions.
   - Oscillator for display clock generation
   - **CABC** (Content Adaptive Brightness Control) function
   - Support **CE** (Color Enhancement) function
   - Support **DGC** (Digital Gamma Correction) function
   - **VGH/VGL** voltage generator for gate control signal in panel
   - 3 times OTP for **VCOM** and **ID 1~3**
   - OTP (One-Time Programming) memory store initialization register settings

2、Description

This document describes Chipone's ICNL9706 supports WXGA resolution driving controller. It includes a timing controller with glass interface level-shifters and a glass power supply circuit to drive a dot-matrix TFT LCD with 800 (RGB) x1280 dots at maximum.

The ICNL9706 supports MIPI DSI (Display Serial Interface) interface mode.

- Four data lanes support up to 500Mbps on the MIPI DSI.

The ICNL9706 also supports various functions to reduce the power consumption of a LCD system via software control.

- Sleep In mode
- Deep standby mode

The ICNL9706 is suitable for any small portable battery-driven and long-term driving products, such as digital cellular phones, smart phones.

3、Device Overview

3.1、Block diagram

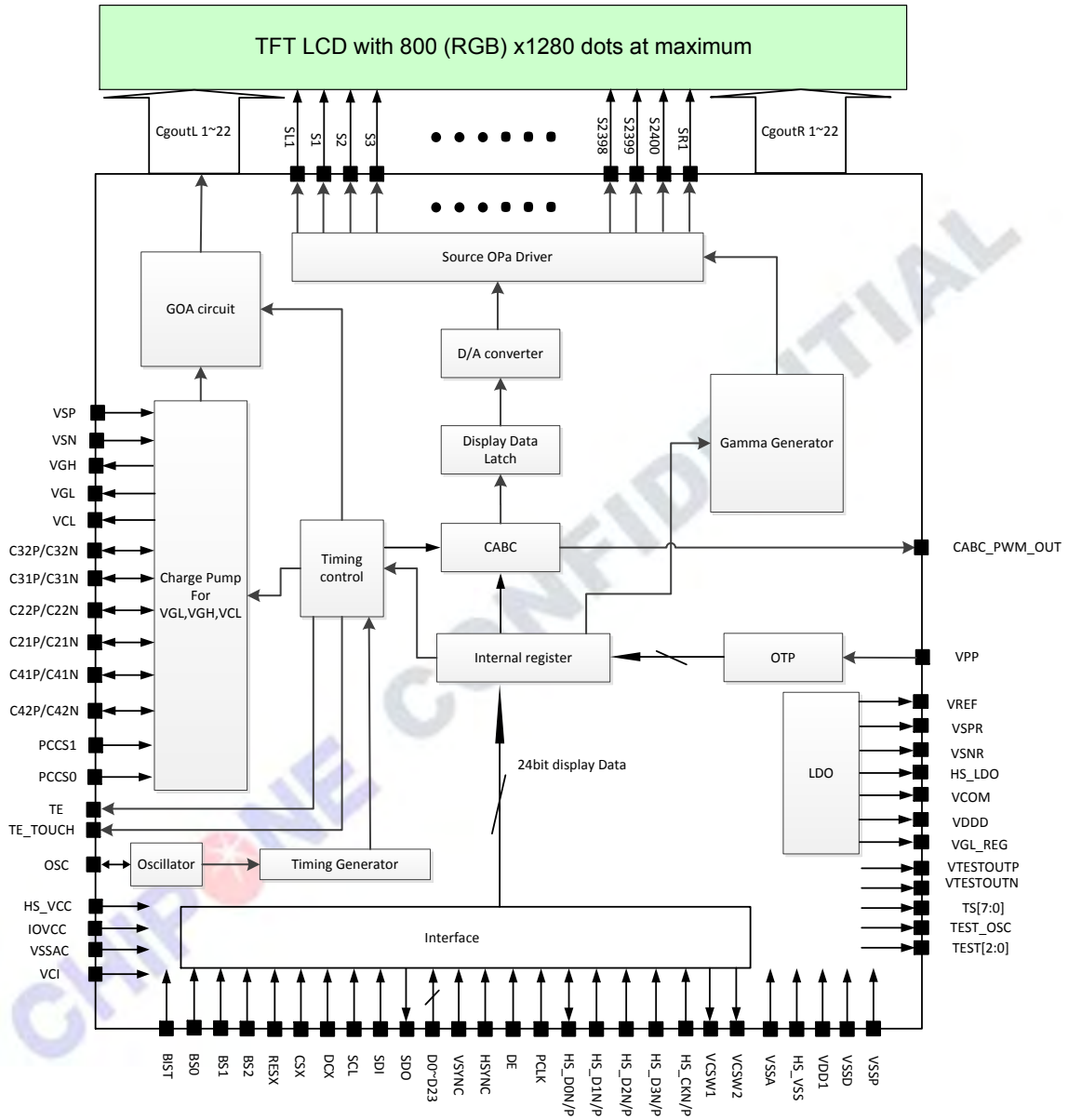


Figure 3-1: Block diagram

3.2、Pin description

3.2.1 Power Input Pads

Symbol	Pad Type	Voltage Range	Description
VCI	Power Supply	2.6V ~ 6.5V	Power supply to the analog circuit.
IOVCC	Power Supply	1.65V ~ 3.3V.	Power supply for the logic power and I/O circuit.
HS_VCC	Power Supply	1.65V ~ 3.3V	Power supply for MIPI D-PHY analog power.
VSP	Power Supply	4V ~ 6.5V	Power supply for Charge pump circuit.
VSN	Power Supply	-4V ~ -6.5V	Power supply for Charge pump circuit.
VPP	Power Supply	8.3V ~8.7V	Power supply for OTP.
VSSP	Power Supply	0V	Charge Pump circuit ground.
VSSD	Power Supply	0V	Logic power and I/O circuit ground.
VSSAC	Power Supply	0V	Analog circuit ground.
HS_VSS	Power Supply	0V	MIPI High speed circuit ground.
VSSA	Power Supply	0V	Analog circuit ground.

3.2.2 Power Output Pads

Symbol	Pad Type	Voltage Range	Description
HS_LDO	Analog output	1.2V ~ 1.3V	LDO output for MIPI. It must be connected a stabilizing capacitor 1.0uF to VSS.
VDDD	Analog output	1.5V ~ 1.6V	LDO output for Digital circuit. It must be connected a stabilizing capacitor 1.0uF to VSS.
VCL	Analog pump	-1xVCI	Charge pump circuit for Level shift and VCOM It must be connected a stabilizing capacitor 1.0uF to VSS.
VGH	Analog pump	10V ~ 20V	Charge pump circuit for Panel TFT. It must be connected a stabilizing capacitor 1.0uF to VSS.
VGL	Analog pump	-7V ~ -16V	Charge pump circuit for Panel TFT. It must be connected a stabilizing capacitor 1.0uF to VSS.
VGL_REG	Analog output	-6.5V ~ -15.5V	LDO output for Panel TFT. It must be connected a stabilizing capacitor 1.0uF to

			VSS.
VSPR	Analog output	3.0V ~ 6.0V	LDO output for Positive Gamma. It must be connected a stabilizing capacitor 1.0uF to VSS.
VSNR	Analog output	-3.0V ~ -6.0V	LDO output for Negative Gamma. It must be connected a stabilizing capacitor 1.0uF to VSS.
VCOM	Analog output	0V ~ -2.2V	LDO output for Panel common. It must be connected a stabilizing capacitor 1.0uF to VSS.
VREF	Analog output	0V ~ VCI	Analog refer power. It must be connected a stabilizing capacitor 1.0uF to VSS.
C21P / N	Charge pump	VCI ~ VGH	Connect to the step-up capacitors for generating VGH voltage.
C22P / N	Charge pump	VCI ~ VGH	Connect to the step-up capacitors for VGH voltage.
C31P / N	Charge pump	VCL ~ VGL	Connect to the step-up capacitors for VGL voltage.
C32P / N	Charge pump	VCL ~ VGL Or Open	Connect to the step-up capacitors for VGL voltage. It can be Open or connector to the step-up capacitors.
C41P / N	Charge pump	VCI ~ VCL	Connect to the step-up capacitors for VCL voltage.
C42P /N	Charge pump	VCI ~ VCL	Test pad for VCL. Connect to the step-up capacitors for VCL or Floating.
VCSW1 / 2	Analog output	0V ~ VCI	Analog clock phase output for PMIC
CgoutL 1~22 CgoutR 1~22	Analog output	VGH ~ VGL	GOA circuit output for Panel TFT.
S1~S2400	Analog output	VSPR ~ VSNR	Analog output for Panel TFT source
SL1, SR1	Analog output	VSPR ~ VSNR	Analog output for Panel TFT ZigZag source

3.2.3 Digital Interface Output Pads

Symbol	Voltage Range	Description
CABC_PWM_OUT	0V ~ IOVCC	Backlight on/off control pin. This pin can connect to external LED driver IC.
TE	0V ~ IOVCC	Tearing Effect pin.
TE_TOUCH	0V ~ IOVCC	Tearing Effect pin. (Each scan line).

3.2.4 MIPI Interface Pads

Symbol	Pad Type	Description
HS_D0N/P	I/O	MIPI-DSI Data differential signal input / Output pins.
HS_D1N/P	I	MIPI-DSI Data differential signal input pins.
HS_D2N/P	I	MIPI-DSI Data differential signal input pins.
HS_D3N/P	I	MIPI-DSI Data differential signal input pins.
HS_CN/P	I	MIPI-DSI Clock differential signal input pins.

3.2.5 Digital Interface Input Pads

<table>
<tr><th>Symbol</th><th>Voltage Range</th><th>Description</th></tr>
<tr><td>RESX</td><td>0V ~ IOVCC</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>PCCS1/PCCS0</td><td>0V ~ IOVCC</td><td>Select the power mode method as listed below.
<table>
<tr><th>PCCS [1:0]</th><th>IOVCC</th><th>VCI</th><th>VSP</th><th>VSN</th><th>VGH/VGL</th></tr>
<tr><td>00</td><td>External</td><td>X</td><td>External</td><td>External</td><td>External</td></tr>
<tr><td>10</td><td>External</td><td>External</td><td>PMIC</td><td>PMIC</td><td>Internal</td></tr>
<tr><td>11</td><td>External</td><td>X</td><td>External</td><td>External</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>BS2/BS1/BS0</td><td>0V ~ IOVCC</td><td>BS[2:0] are used for the combination of polarity swap and data lane swap of DSI. Input mode method as listed below.
<table>
<tr><th>BS[2:0]</th><th>HS_CN</th><th>HS_CP</th><th>HS_D0N</th><th>HS_D0P</th><th>HS_D1N</th><th>HS_D1P</th><th>HS_D2N</th><th>HS_D2P</th><th>HS_D3N</th><th>HS_D3P</th></tr>
<tr><td>000</td><td>CN</td><td>CP</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>001</td><td>CP</td><td>CN</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>010</td><td>CN</td><td>CP</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>011</td><td>CP</td><td>CN</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>100</td><td>CN</td><td>CP</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>101</td><td>CP</td><td>CN</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>110</td><td>CN</td><td>CP</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>111</td><td>CP</td><td>CN</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
</table></td></tr>
</table>

3.2.6 Test Pads

Symbol	Voltage Range	Description
VTESTOUTN	Open	Test mode for Gamma voltage output.
VTSETOUTP	Open	Test mode for Gamma voltage output.
TS[7:0]	Open	Test mode for Internal Logic function test.
TEST_OSC	Open or VSSD	Test mode for Oscillator input for test purpose.
DB[23:0]	Open	Test mode for Data Bus signals.
BIST	Open	Internal Logic function test.
HSYNC	IOVCC or VSSD	Test mode for Line synchronizing signal.
VSYNC	IOVCC or VSSD	Test mode for Frame synchronizing signal.
DE	IOVCC or VSSD	Test mode for Data enable signal.
PCLK	IOVCC or VSSD	Test mode for Dot clock input.
DCX	IOVCC or VSSD	Test mode for Select Command / Data.
CSX	IOVCC	Test mode for Chip select.
SCL	IOVCC	Test mode for Serial clock input.
SDI	Open	Test mode for Serial data input.
SDO	Open	Test mode for Serial data output.
TEST[2:0]	Open or VSSD	Test mode for Internal Logic function test.

4、Electrical Characteristics

4.1、Absolute Maximum Ratings

The absolute maximum rating is listed in below table. When the ICNL9706 is used out of the absolute maximum ratings, it may be permanently damaged.
To use the ICNL9706 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ICNL9706 will malfunction and cause poor reliability.

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage	IOVCC ~ VSSD	-0.3	-	+3.6	V
Supply voltage	VCI ~ VSSA	-0.3	-	+6.6	V
Supply voltage	HS_VCC ~ HS_VSS	-0.3	-	+3.6	V
Supply voltage	VSP ~ VSSA	-0.3	-	+6.6	V
Supply voltage	VSSA ~ VSN	-6.6	-	0	V
Supply voltage	VGH ~ VGL	|VGH-VGL| ≦30			V
Operating temperature	Topr	-40		+85	℃
Storage temperature	Tstg	-55		+110	℃
Input voltage	Vin	-0.3		IOVCC+0.3	V
HS input voltage	Vhsin	-0.3		+2	V

4.2、DC CHARACTERISTICS

Condition : Ta =25℃

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.6	3.0	3.6	V	1
Analog Operating voltage	VCI	Operating Voltage	4	5.5	6.5	V	2
Analog Operating voltage	VSP	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	VSN	Operating Voltage	-6.5	-5.5	-4.5	V	
Analog Operating voltage	VCOM	Operating Voltage	-2.2		0.3	V	
Analog Operating voltage	VSPR	Operating Voltage	3	4.5	6	V	
Analog Operating voltage	VSNR	Operating Voltage	-6	-4.5	-3	V	
Analog Operating voltage	|VGH-VGL|	Operating Voltage	|VGH-VGL| ≦30			V	
I/O operating voltage	IOVCC	I/O supply voltage	1.6	1.8	3.6	V	
MIPI Operating voltage	HS_VCC	HS_VCC supply voltage	1.1	1.2	1.3	V	
Digital Operating voltage	VDDD	Digital supply voltage	1.5	1.6	1.7	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	VIH		0.7*IOVCC	-	IOVCC	V	3
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	3
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	4
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	4
Logic High level leakage	ILIH1	Vin = 0 to *IOVCC*			1	μA	3,4
Logic Low level leakage	ILIL1	Vin = 0 to *IOVCC*	-1			μA	3,4
VCSW High level leakage	ILIH2	Vin = 0 to *VCI*			1	μA	5
VCSW Low level leakage	ILIL2	Vin = 0 to *VCI*	-1			μA	5
Source OPa Output							
Output deviation voltage	V,dev	Sout>=4.2V,Sout<=0.8V			30	mV	6
Output deviation voltage	V,dev	4.2V>Sout>0.8V			20	mV	
Output offset voltage	VOFSET				40	mv	6
Standby Current							
Sleep In mode	Istlp	DSI LP mode IOVCC Current			TBD	uA	
		DSI LP mode VCI Current			TBD	uA	1
	Istul	DSI Ultra Low power IOVCC Current			TBD	uA	
		DSI Ultra Low power VCI Current			TBD	uA	1
DSTB	Idstb	DSTB mode IOVCC			1	uA	
		DSTB mode VCI			1	uA	1
Oscillator Output							
Oscillator tolerance	△OSC	Ta =25℃	-5	-	+5	%	7

Note 1: PCCS[1:0] pin = 10 mode
Note2: PCCS[1:0] pin =00, 11 mode

Note3: RESET,PCCS[1:0],BS[2:0],TEST_OSC,BIST,HSYNC,VSYNC,DE,PCLK,DCX,CSX,SCL,TEST[2:0] pin
Note4: CABC_PWM_OUT,TE,TE_TOUCH pin
Note5: VCSW1,VSCW2 pin
Note6: SAP =0110
Note7: Oscillator =45MHz

4.3、MIPI DC Characteristics

4.3.1 DC Characteristics for DSI LP Mode

Condition : Ta =25℃,IOVCC =1.6V~3.6V, VCI =2.6V~6.5V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input voltage	I_{IH}	LP-RX,Vin =0~1.3V			10	uA	
Logic Low level input voltage	I_{IL}	LP-RX,Vin =0~1.3V	-10			uA	
Input pulse rejection	SGD	DSI-CLK+/-,DSI Dn+/-			300	Vps	1

Note 1: Peak interference amplitude max. 200mV and interferene frequency min. 450MHz

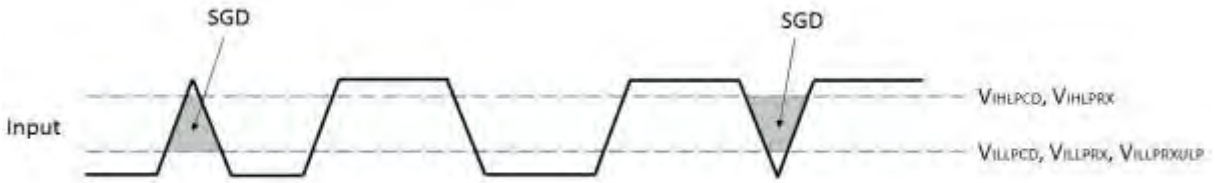


Figure 4.3.1-1: Spike/Glitch Rejection

4.3.2 DC Characteristics for DSI HS Mode

Condition : Ta =25℃,IOVCC =1.6V~3.6V, VCI =2.6V~6.5V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLK+/-, Dn+/-	70		330	mV	1,2
Input voltage common mode variation(≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLK+/-, Dn+/-	-50		50	mV	3
Input voltage common mode variation(≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLK+/-, Dn+/-			100	mV	
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	CLK+/-, Dn+/-	-70			mV	
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	CLK+/-, Dn+/-			70	mV	
Single-ended input low voltage	V_{ILHS}	CLK+/-, Dn+/-	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLK+/-, Dn+/-			460	mV	2
Differential input termination resistor	R_{TERM}	CLK+/-, Dn+/-	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLK+/-, Dn+/-			450	mV	
Termination capacitor	C_{TERM}	CLK+/-, Dn+/-			14	pF	

Note 1: Includes 50mV (-50mV to 50mV) ground difference
Note 2: Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$
Note3: Without 50mV (-50mV to 50mV) ground difference
Note4: Dn =D0,D1,D2 and D3

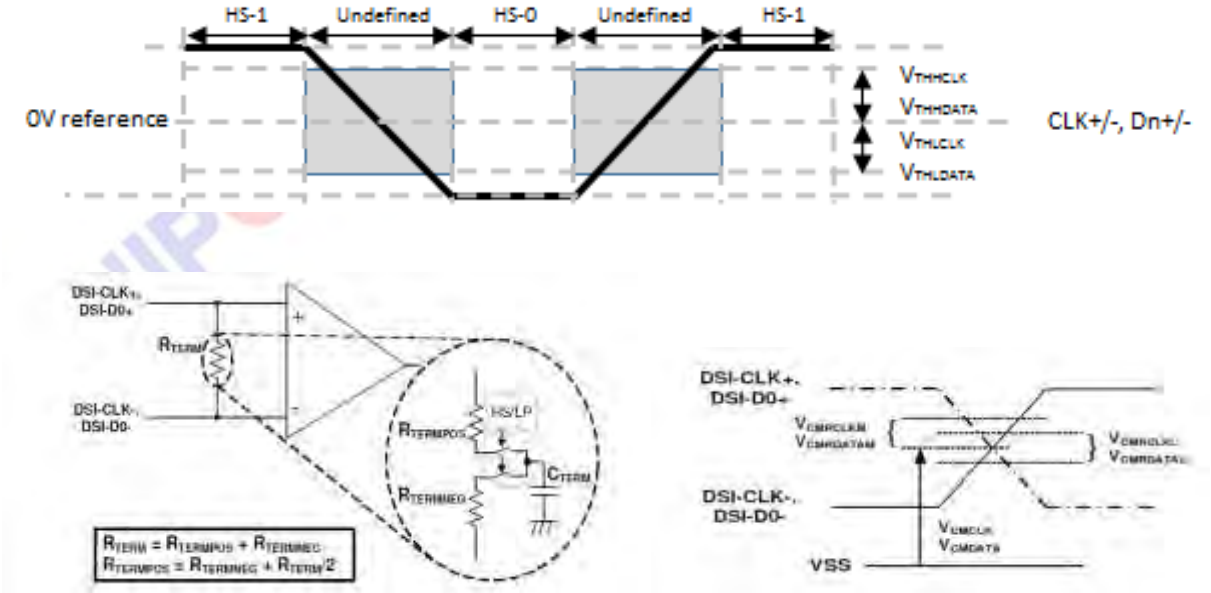


Figure 4.3.2-1: Differential voltage range, termination resistor and Common mode voltage

4.4、AC Timings Characteristics

4.4.1 Vertical Timings for DSI video mode

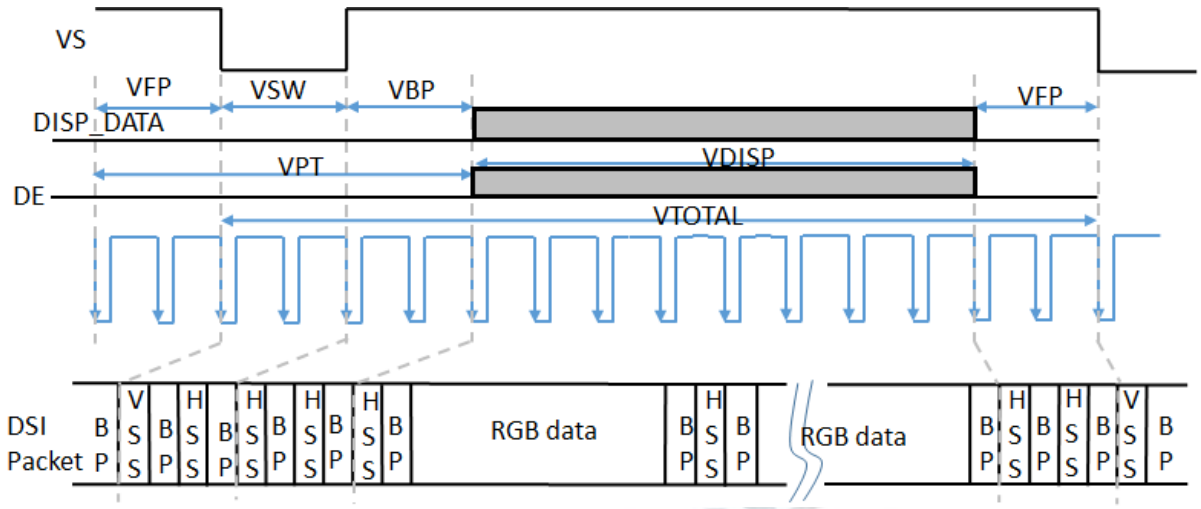


Figure 4.4.1-1: Vertical timings for DSI interface

Condition : Ta =25℃,Resolution = 800(RGB)* 1280

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Vertical Total	VTOTAL		1286			Line	
Vertical low pulse width	VSW		2			Line	1
Vertical front porch	VFP		2			Line	
Vertical back porch	VBP		2			Line	1
Vertical data start point		VSW+VBP	4			Line	1
Vertical blanking period	VPT	VSW+VBP+VFP	6			Line	
Vertical active area		VDISP		1280		Line	
Vertical Frame rate	VFR			60		Hz	

Note 1: The VSW and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCM normal display.

4.4.2 Horizontal Timings for DSI video mode

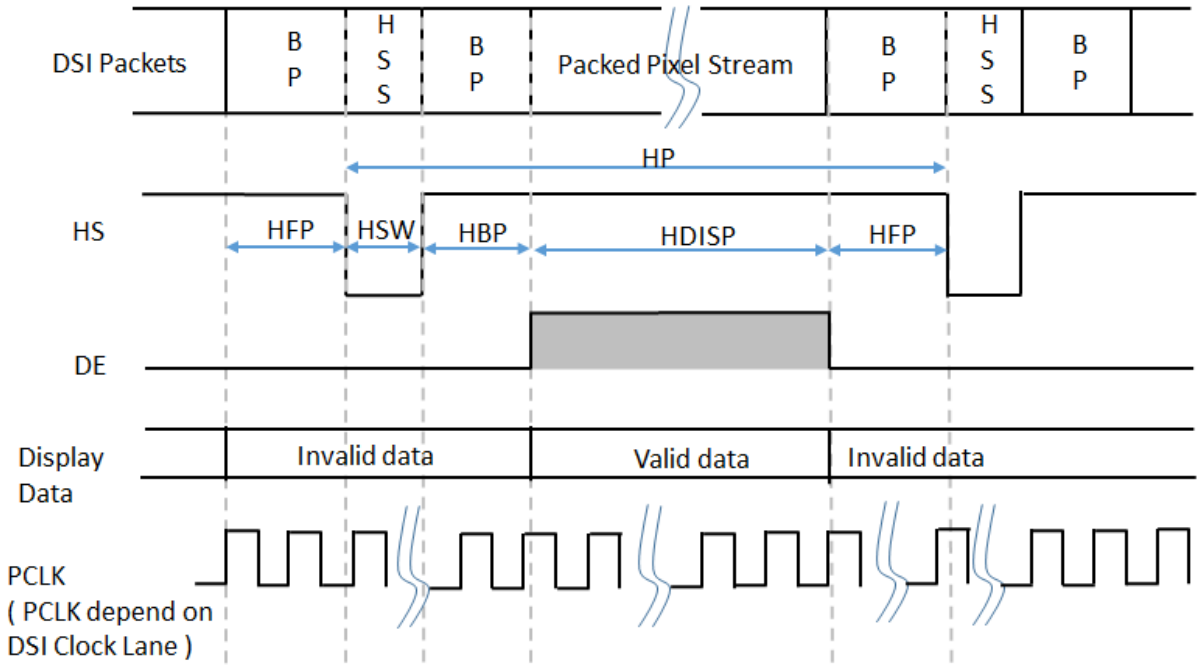


Figure 4.4.2-1: Horizontal timings for DSI video mode

Condition : Ta =25℃,Resolution = 800(RGB)* 1280

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW		0.2			uS	
Horizontal back porch	HBP		1.0			uS	
Horizontal front porch	HFP		1.0			uS	
Horizontal data start point		HSW+HBP	1.2			uS	
Horizontal blanking period	HBLK	HSW+HBP+HFP	2.2			uS	
Horizontal active area	HDISP			800		DCK	

4.5、MIPI AC Characteristics

4.5.1 High Speed Mode - Clock Timings

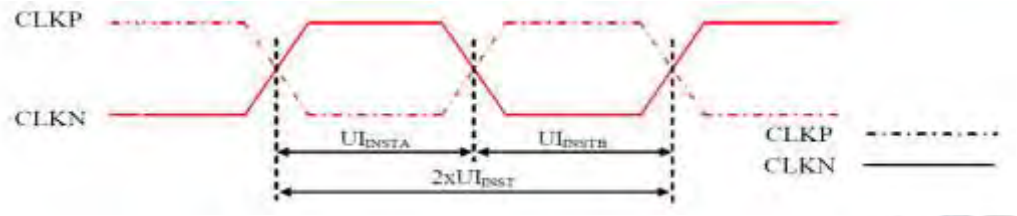


Figure 4.5.1-1: Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	4		25	nS	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	2		12.5	nS	1

Note 1: UI = UIINSTA = UIINSTB

4.5.2 High Speed Mode - Clock / Data Timings

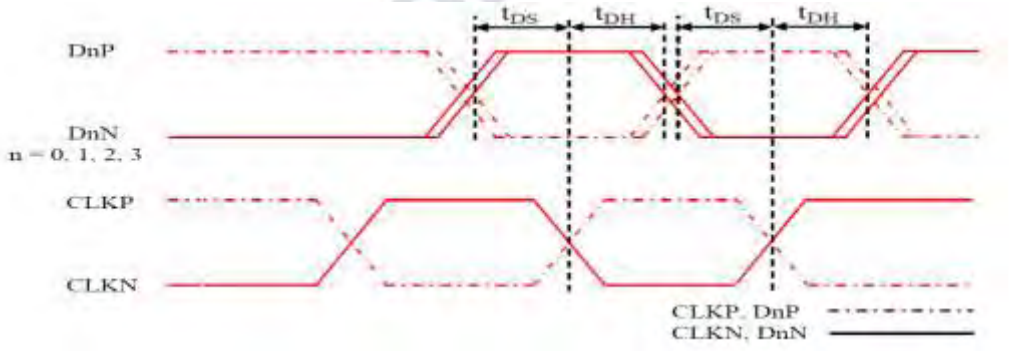


Figure 4.5.2-1: DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

4.5.3 High Speed Mode - Rising and Falling Timings

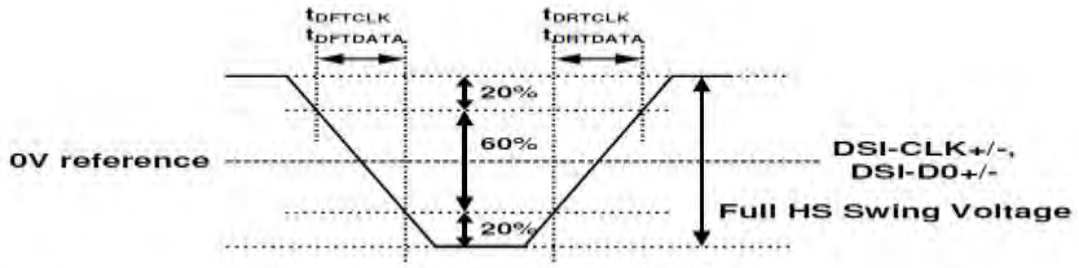


Figure4.5.3-1: Rising and Falling Timings

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,23

Note 1: Dn =0,1,2 and 3
Note2: The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.
Note3: DSI-CLK+ = CLKP
DSI-CLK- =CLKN
DSI-D0+ =D0P
DSI-D0- =D0N

4.5.4 Low Speed Mode - Bus Turn Around

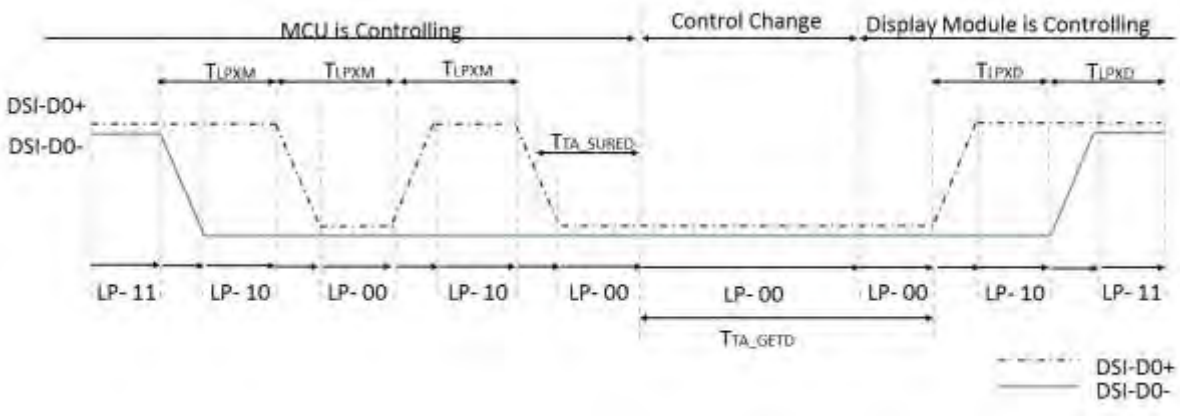


Figure 4.5.4-1: Bus Turnaround (BTA) from MCU to display module Timing

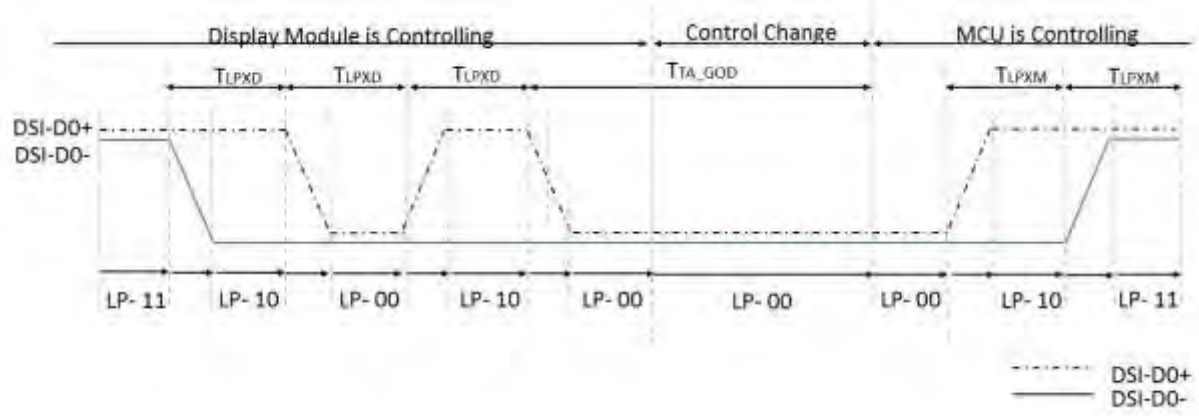


Figure 4.5.4-2: Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-

4.5.5 Data Lanes from Low Power Mode to High Speed Mode

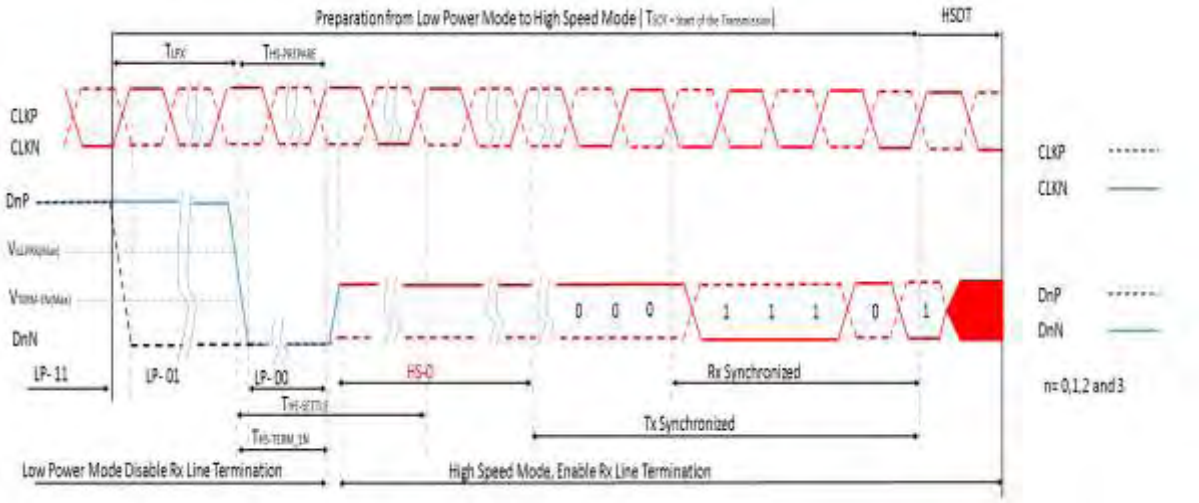


Figure 4.5.5-1: Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
D0P/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
D0P/N	$T_{HS-TREM-EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: Dn =0,1,2 and 3

4.5.6 Data Lanes from High Speed Mode to Low Power Mode

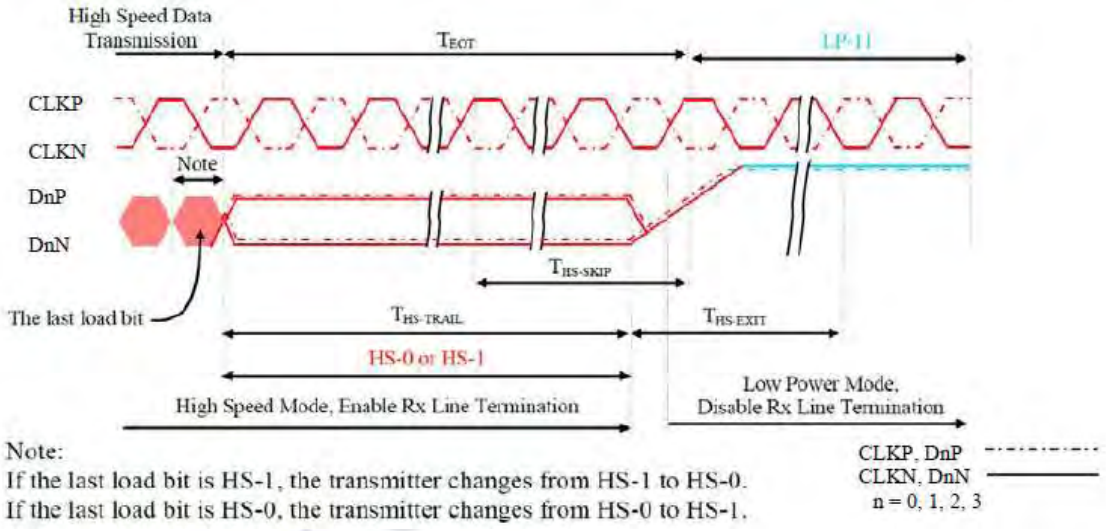


Figure 4.5.6-1: Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
D0P/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	1

Note 1: Dn =0,1,2 and 3

4.5.7 DSI Clock Burst – High speed mode to /from Low Power Mode

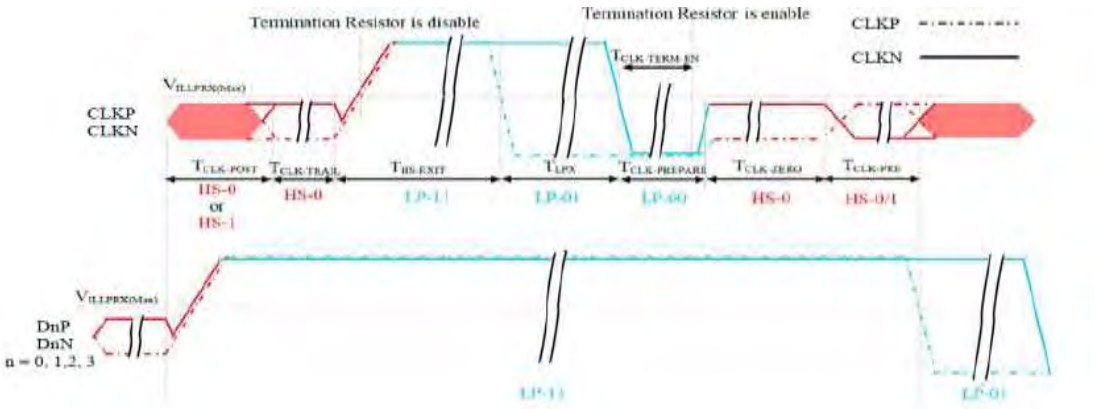


Figure 4.5.7-1: Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

4.6、Reset Input Timing

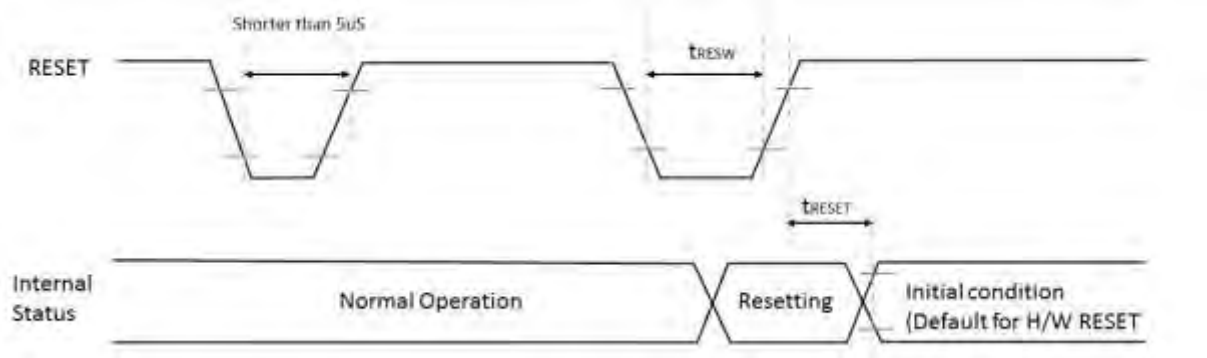


Figure 4.6-1: Reset Input Timing

Condition : Ta =25℃

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

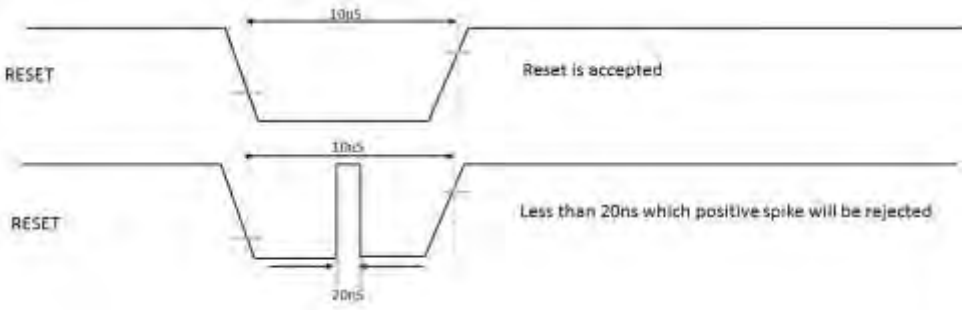
Note 1: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10uS	Reset
Between 5us and 10uS	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time(tRESET) within 5ms after a rising edge of RESET.

Note4: Spike Rejection also applies during a valid reset pulse as shown below:



Note5: It is necessary to wait 5msec after releasing RESET before sending commands. Also Sleep Out command can not be sent for 120msec.

5、Interface

5.1、Interface Level Communication

5.1.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.
Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.
High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.
Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.
The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential - 0	Note1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note1	Note1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Note 1: Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.

Note2 : If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.

Note3: n = 0, 1, 2 and 3 (D1P/N, D2 P/N and D3 P/N lanes only for HS-0 and HS-1)

5.1.2 DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM).These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

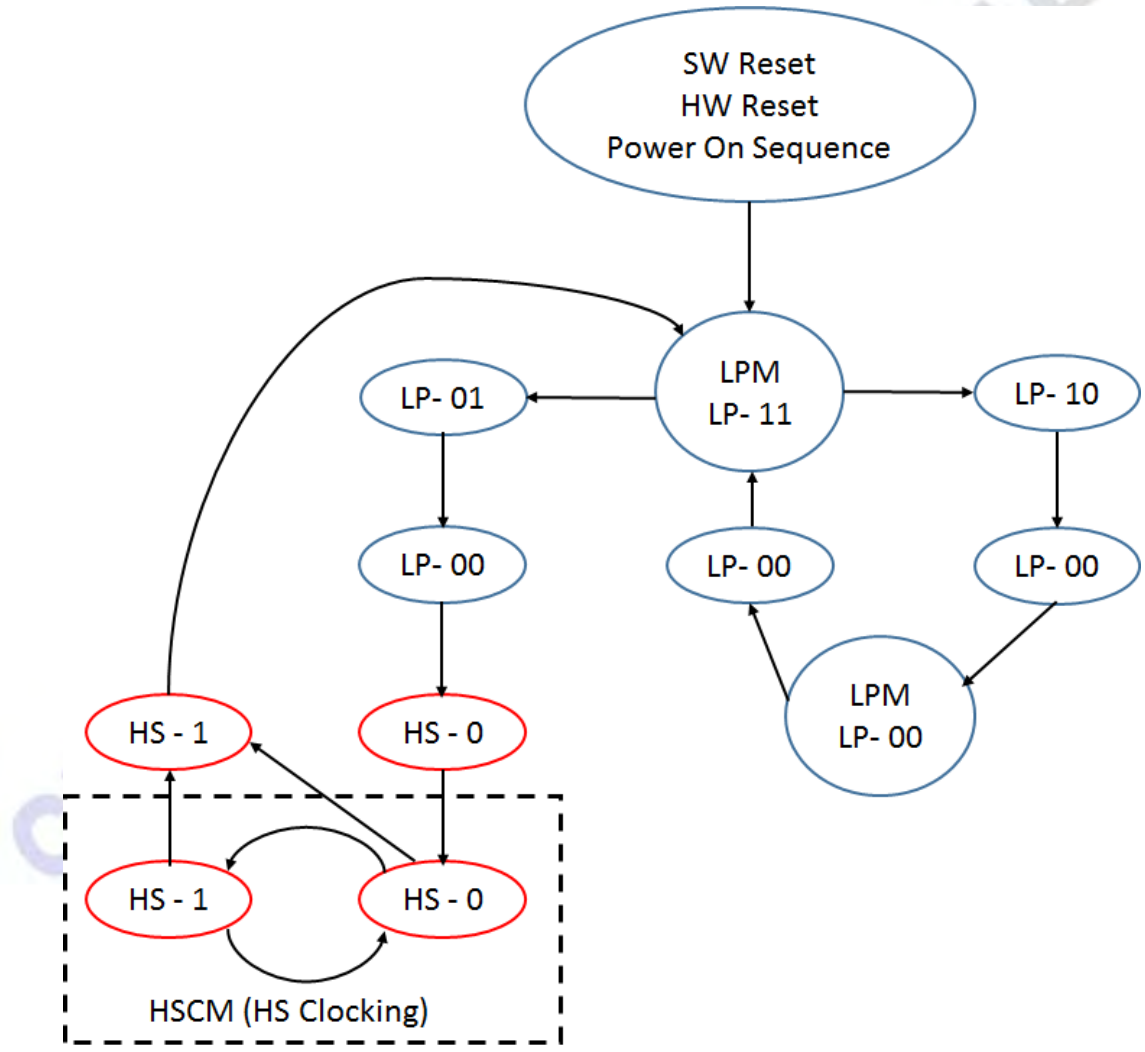


Figure 5.1.2-1: Clock Lane Power Modes

5.1.3 Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11
2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

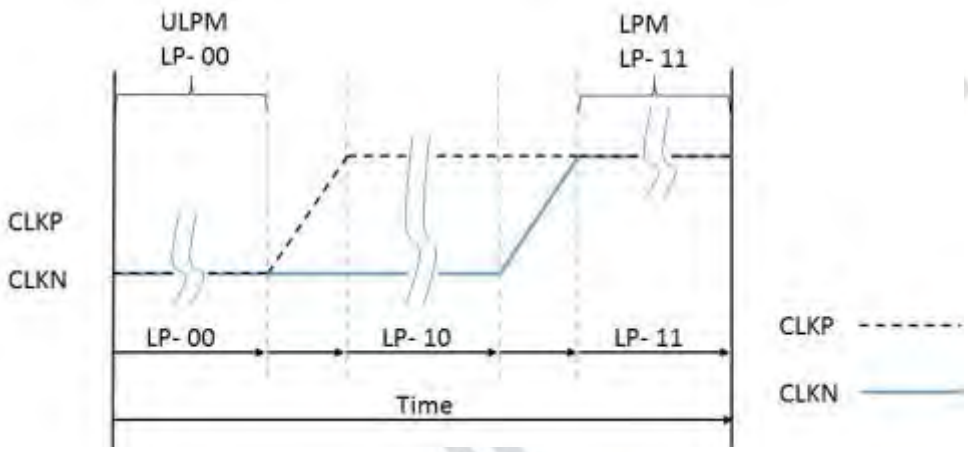


Figure 5.1.3-1: From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM).

This sequence is illustrated below.

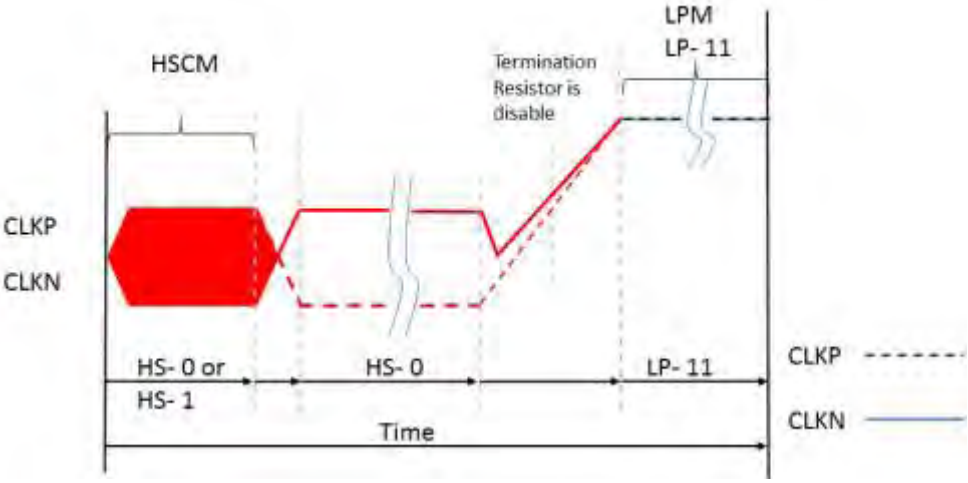


Figure 5.1.3-2: From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

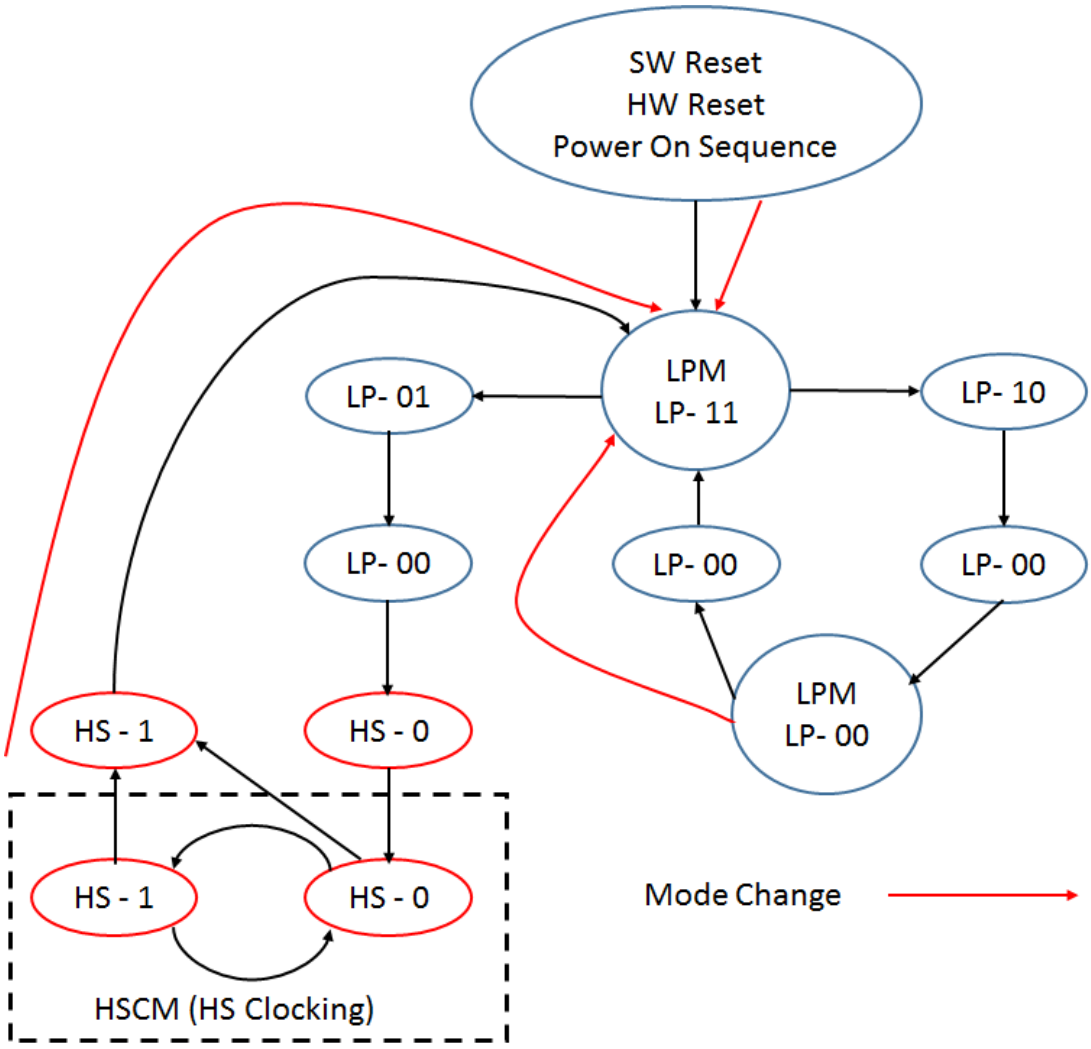


Figure 5.1.3-3: All Three Mode Changes to LPM

5.1.4 Ultra- Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:
1) After SW Reset, HW Reset or Power On Sequence => LP-11
2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).
This sequence is illustrated below.

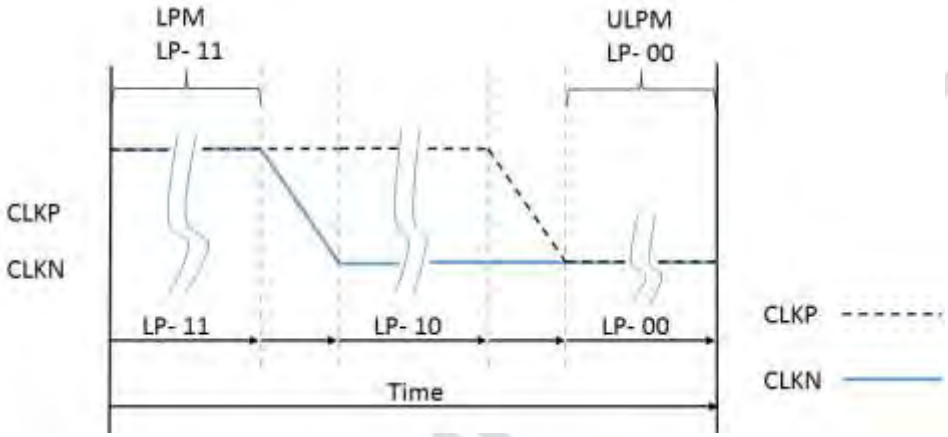


Figure 5.1.4-1: From LPM to ULPM

The mode change is also illustrated below.

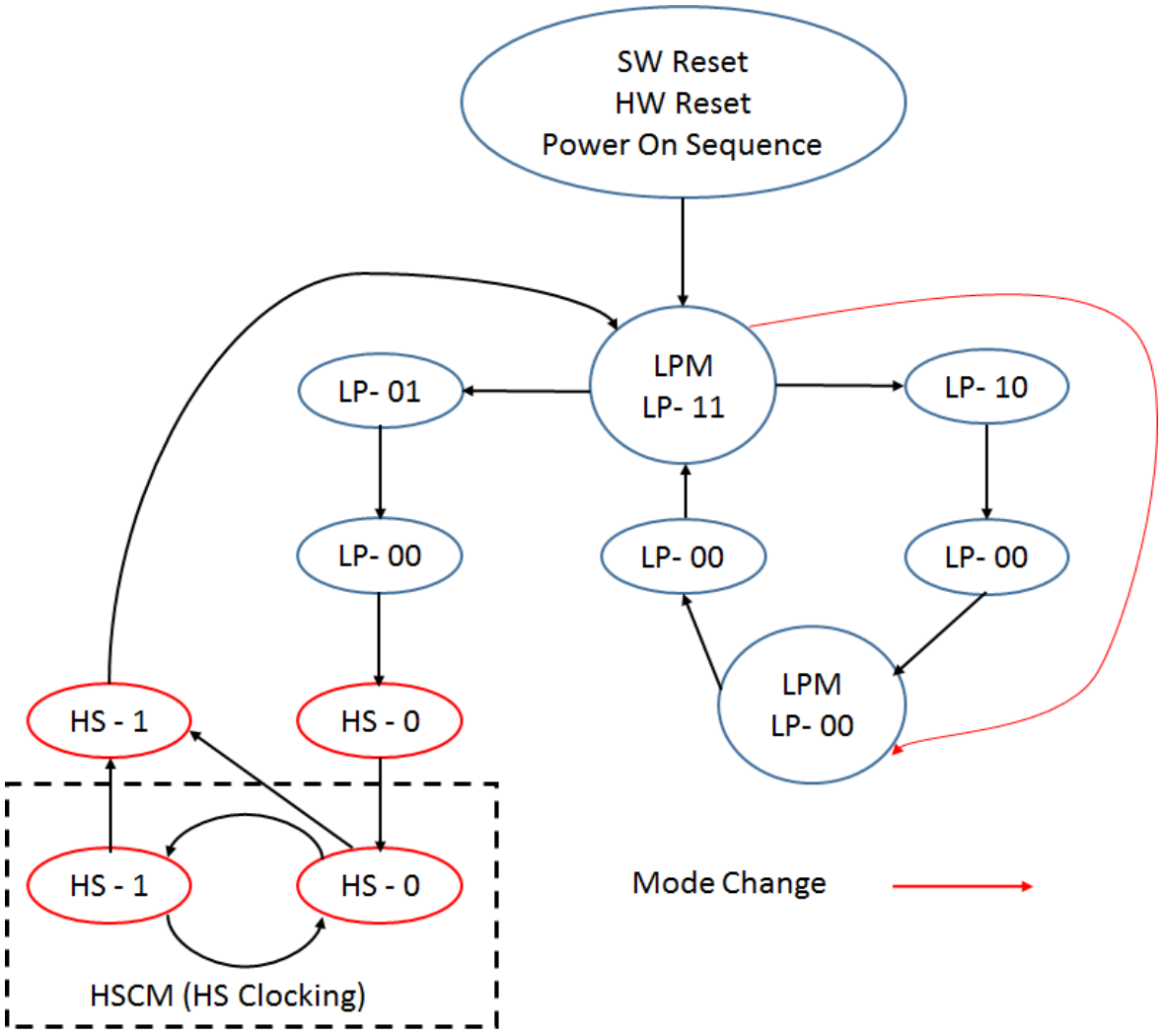


Figure 5.1.4-2: Mode Change from LPM to ULPM

5.1.5 High- Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM).
This sequence is illustrated below.

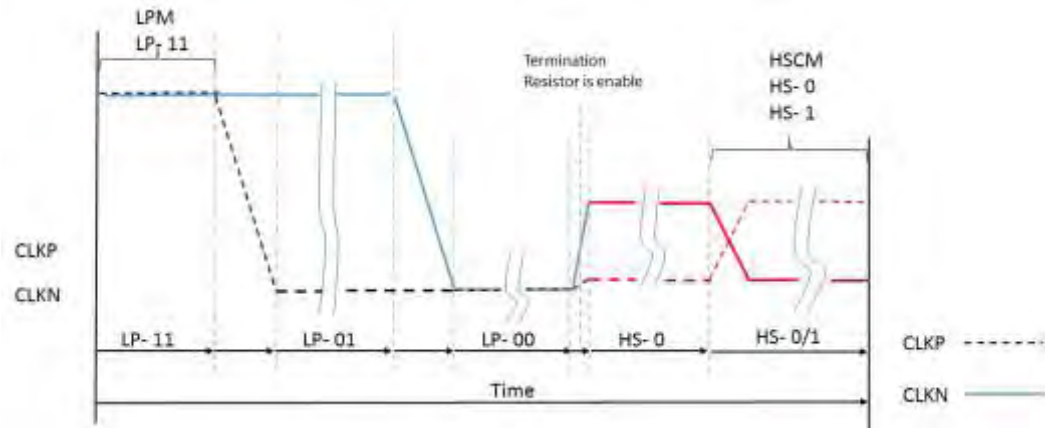


Figure 5.1.5-1: From LPM to HSCM

The mode change is also illustrated below.

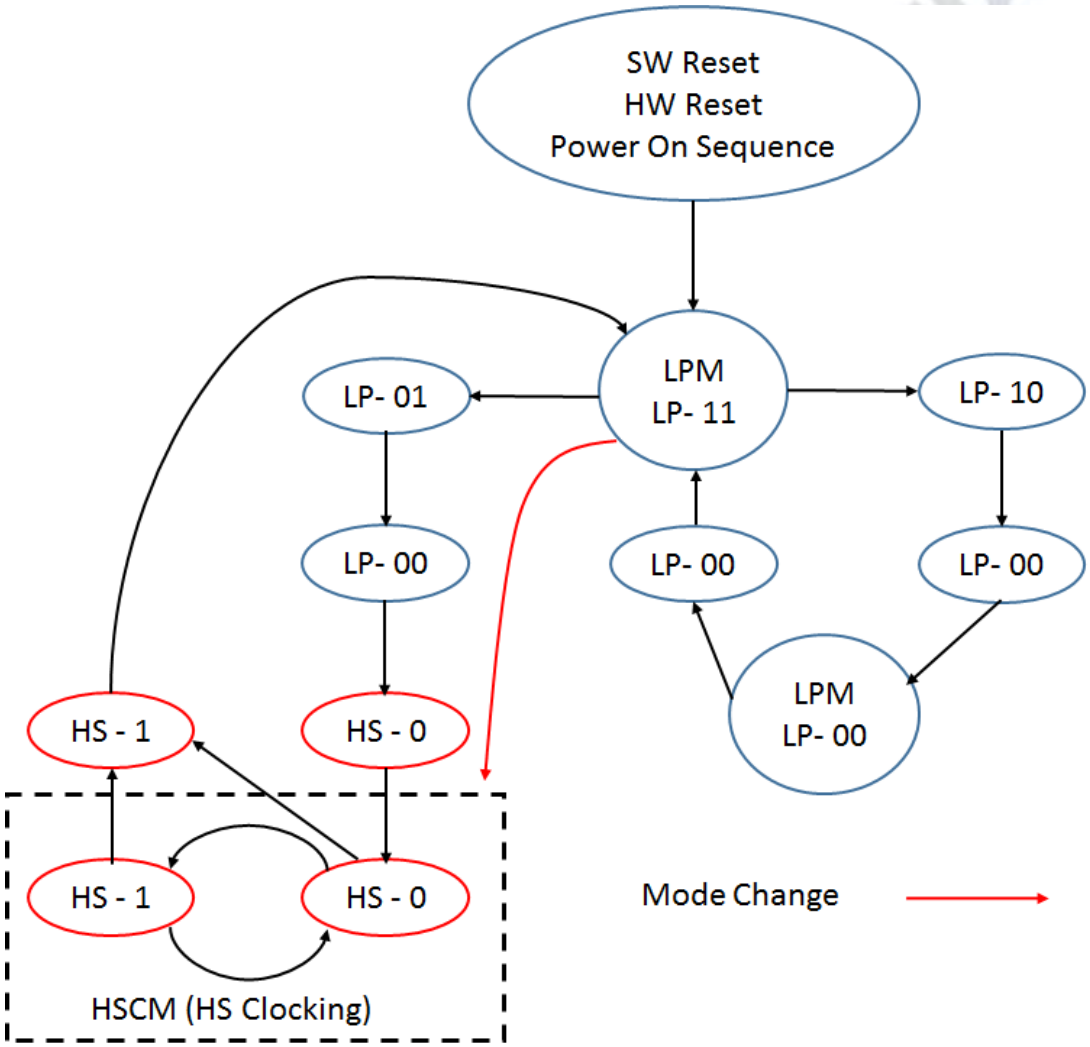
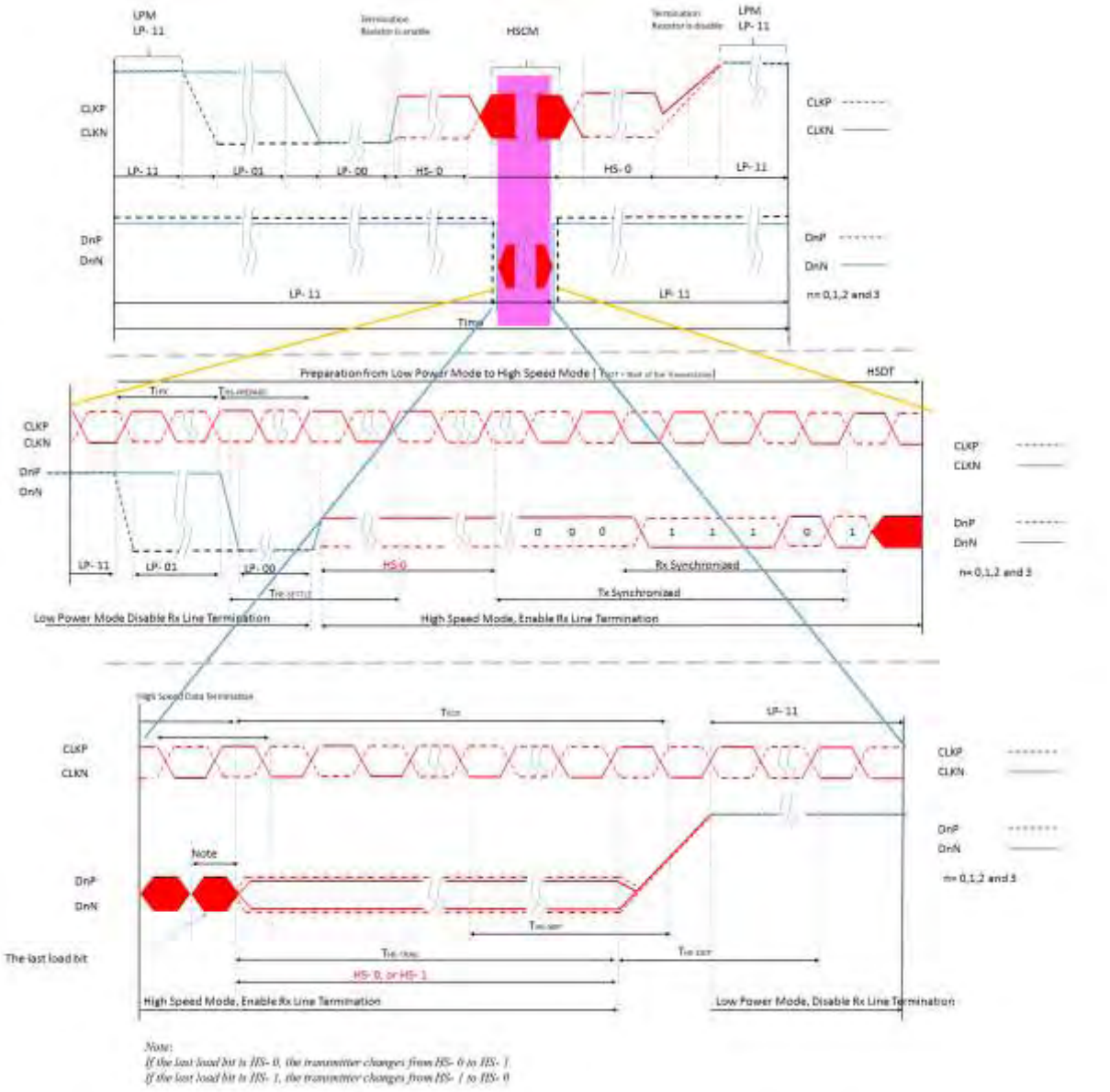


Figure 5.1.5-2: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes.
The high speed clock continues clocking after the high speed data sending is stopped.
The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS- 0
- End state is HS- 0



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 5.1.5-3: High Speed Clock Burst

5.2、Interface Level Communication - DSI Data Lane

5.2.1 General

D3P/N, D2P/N, D1P/N, and D0P/N Data lanes can be driven into different modes:
- Escape Mode (Only D0P/N data lane is used)
- High- Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only D0P/N data lane are used)

These modes and their entering codes are defined in the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP- 11→ LP- 10→ LP- 00 → LP- 01 → LP- 00	LP- 00→ LP- 10→ LP- 11 (Mark-1)
High- Speed Data Transmission	LP- 11→ LP- 01 → LP- 00 → HS- 0	(HS- 0 or HS- 1)→ LP11
Bus Turnaround Request	LP- 11→ LP- 10→ LP- 00 → LP- 10→ LP- 00	Hi- Z

5.2.2 Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:
- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module.
- Drive data lanes to “Ultra-Low Power State” (ULPS).
- Indicate “Remote Application Reset” (RAR), which can reset the display module.
  Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:
- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

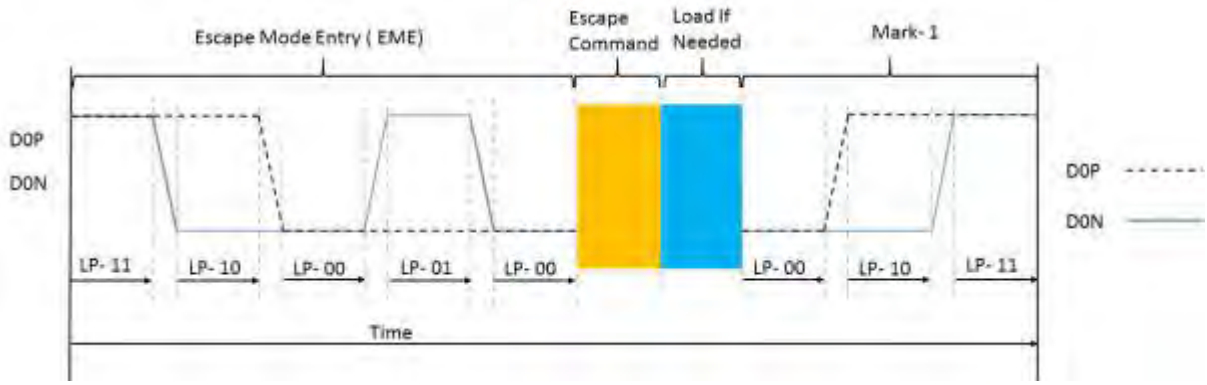


Figure 5.2.2-1: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in below Table.
An example of the Mode type Escape Command is „Ultra-Low Power Mode", where the MCU instructs the display module to enter its Ultra-Low Power Mode.
Escape commands are defined in the following table.

Escape Command	Command Type Mode / Trigger	Entry command Pattern (First Bit→ Last Bit Transmitted)	Dn	D0
Low- Power Data Transmission	Mode	1110 0001 bin		x
Ultra- Low Power Mode	Mode	0001 1110 bin	x	x
Underfined- 1, Note1	Mode	1001 1111 bin		
Underfined- 2, Note1	Mode	1101 1110 bin		
Remote Application Reset	Trigger	0110 0010 bin		x
Acknowledge	Trigger	0010 0001 bin		x
UnKnow- 5, Note1	Trigger	1010 0000 bin		

Note 1: This Escape command support is not implemented on the display module.

Note2: n=1

Note3: x= supported

5.2.3 Low- Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module.
The display module also uses the same sequence when it sends data to the MCU.
The Low Power Data
Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
- One or more bytes (one byte = 8 bit)
- Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

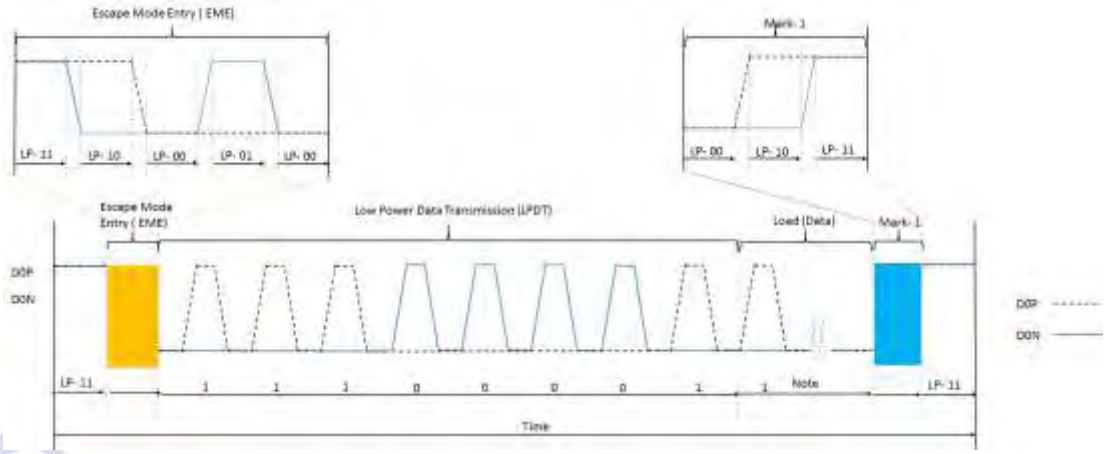


Figure 5.2.3-1: Low- Power Data Transmission (LPDT)

Note: Load (Data) presents that the first bit is the logical 1 in this example.

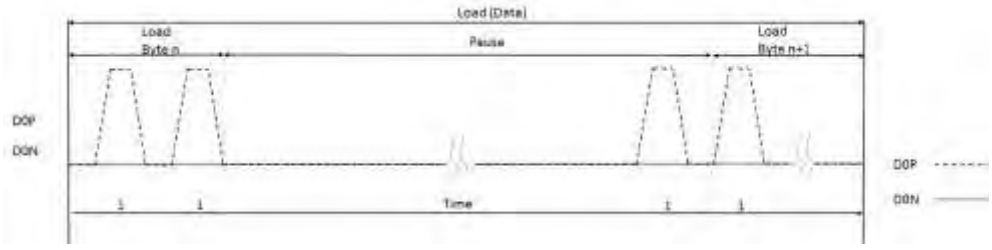


Figure 5.2.3-2: Pause (Example)

5.2.4 Ultra- Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

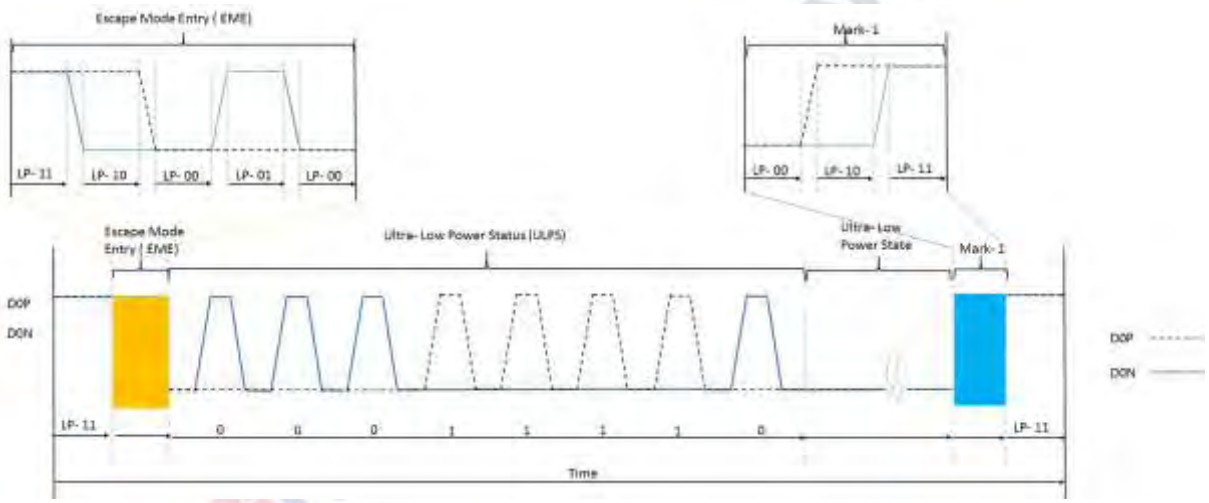


Figure 5.2.4-1: Ultra- Low Power State (ULPS)

5.2.5 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

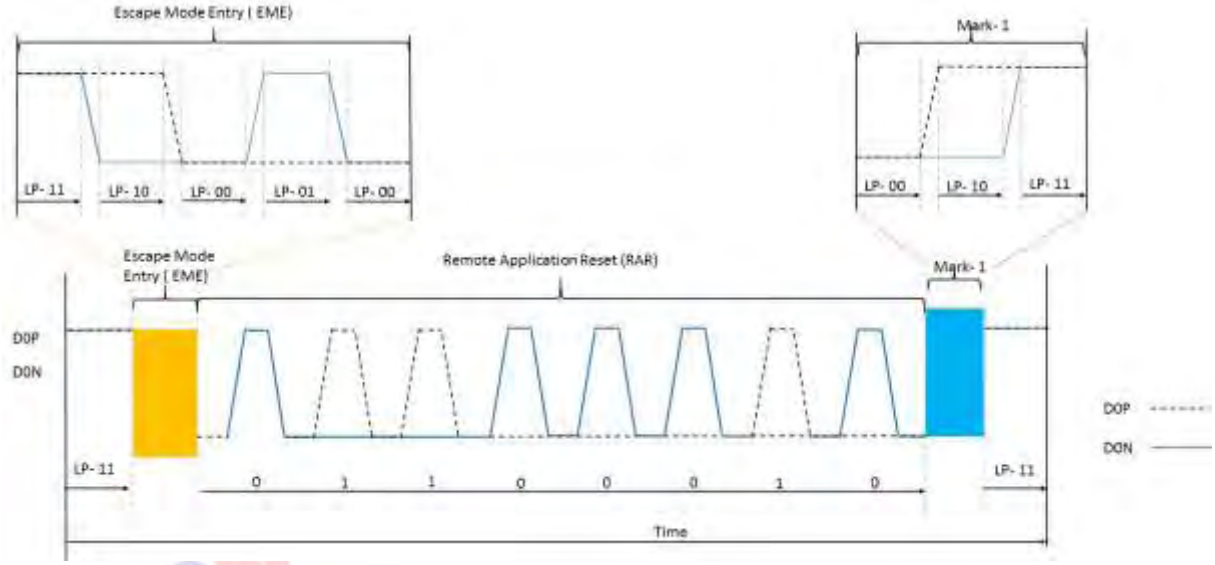


Figure 5.2.5-1: Remote Application Reset (RAR)

5.2.6 Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

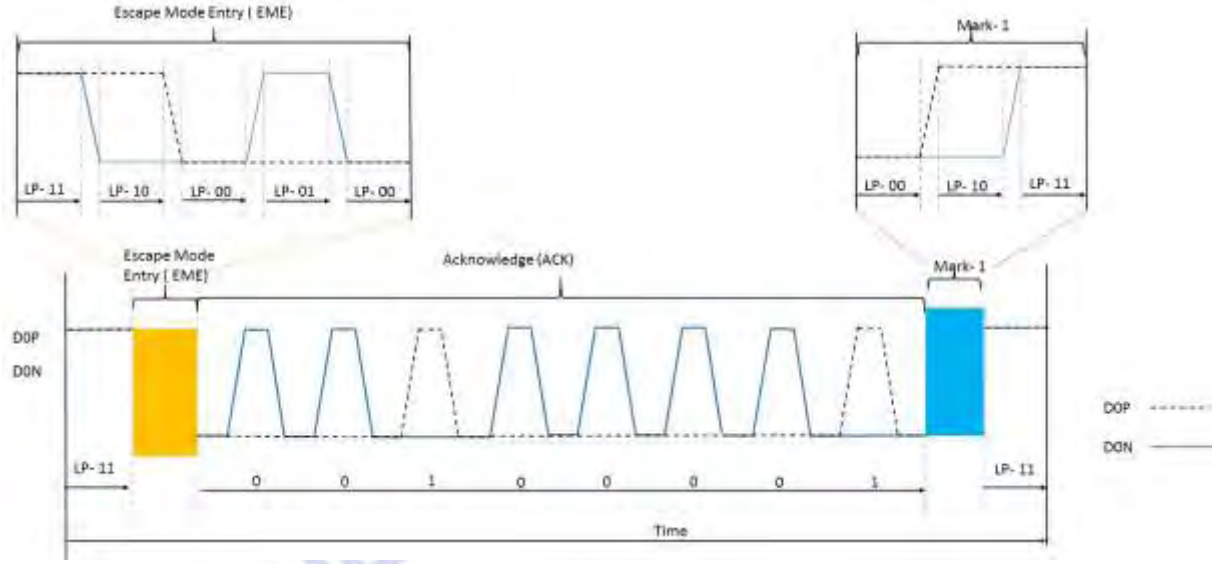


Figure5.2.6-1: Acknowledge (ACK)

5.2.7 Entering High- Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

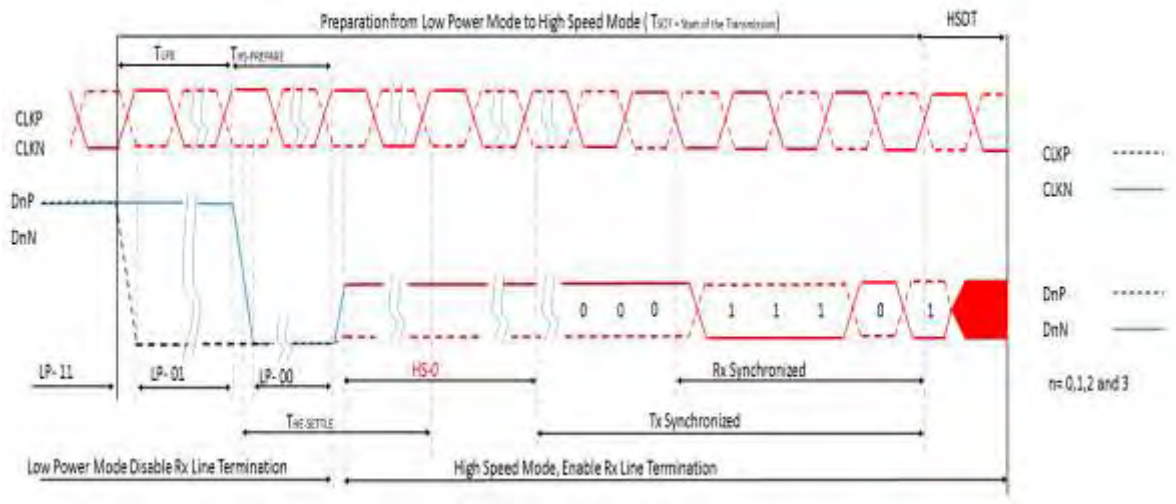


Figure 5.2.7-1: Entering High- Speed Data Transmission (TSOT of HSDT)

5.2.8 Leaving High- Speed Data Transmission (TEOP of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D3P/N, D2P/N, D1P/N and D0P/N are in the LP-11 mode. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

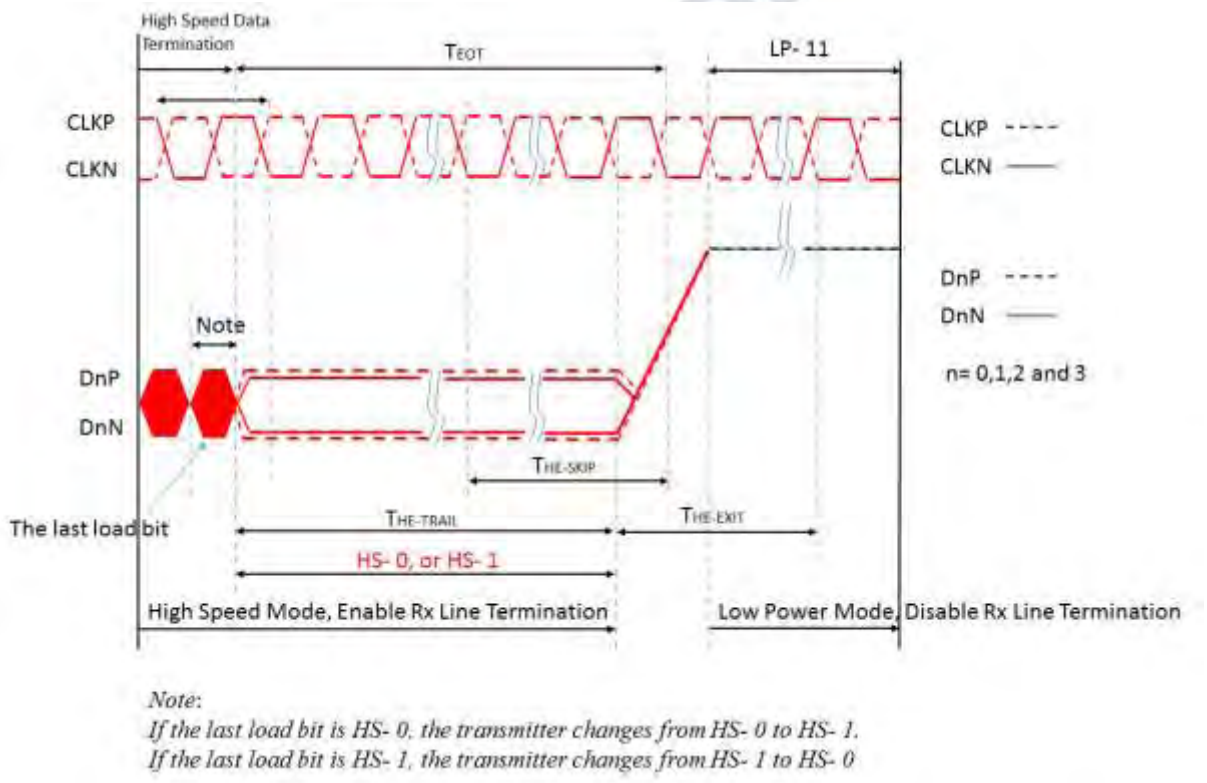


Figure 5.2.8-1: Leaving High- Speed Data Transmission (TEOT of HSDT)

5.2.9 Burst of the High- Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

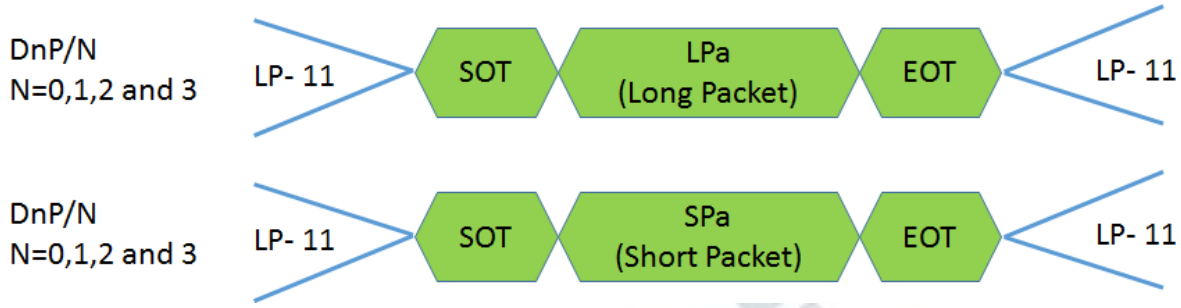


Figure 5.2.9-1: Single Packet in High- Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

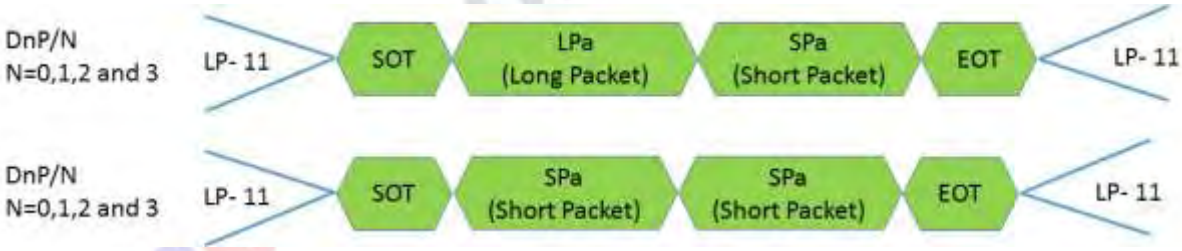


Figure 5.2.9-2: Multiple Packets in High- Speed Data Transmission – Example

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are “1”s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

5.2.10 Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module. The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

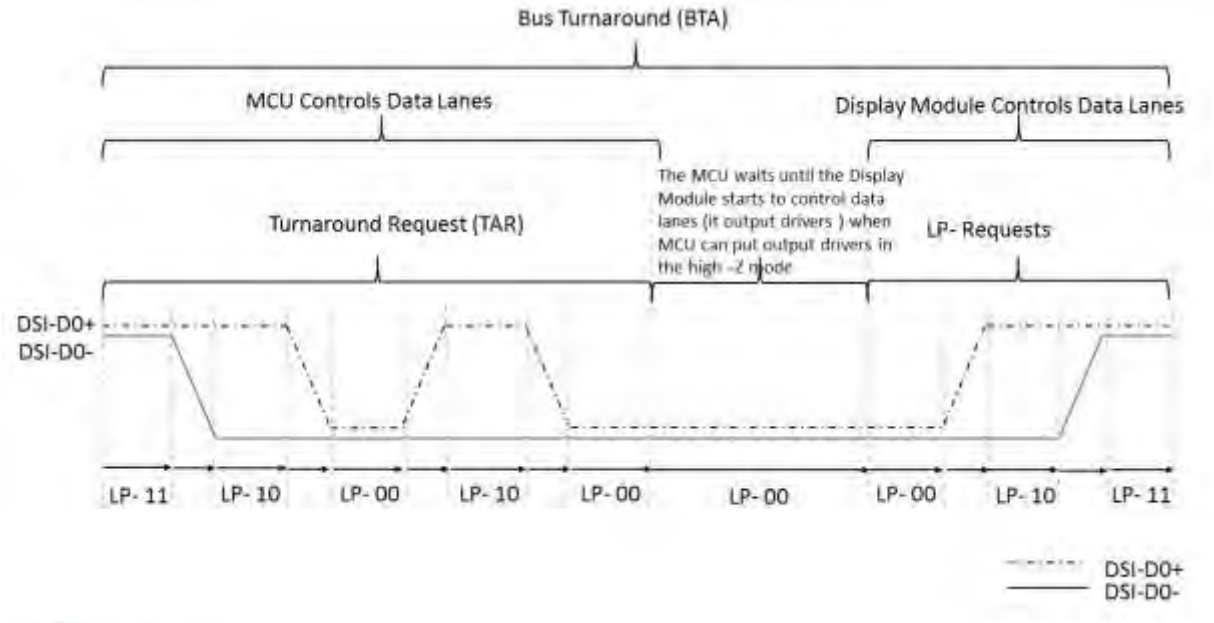


Figure5.2.10-1: Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 5.2.10-1 if the Bus Turnaround (BTA) is from the display module to the MCU.

5.3、Packet Level Communication

5.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

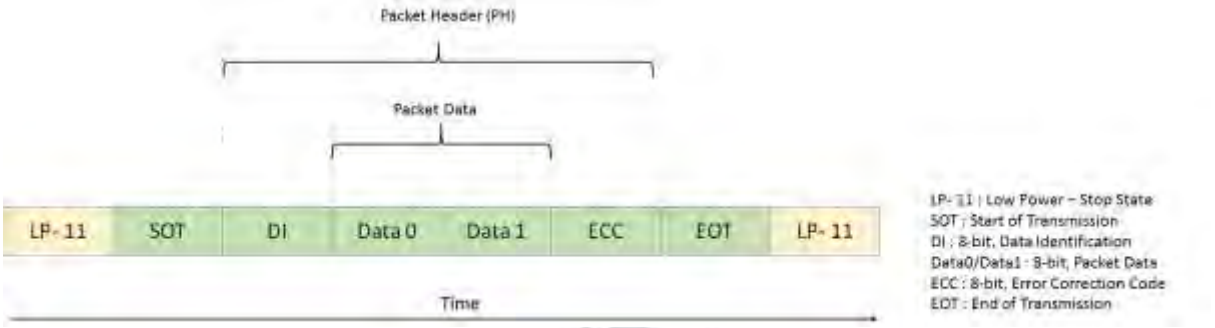


Figure 5.3.1-1: Short Packet (SPa) Structure

Figure 5.3.1-2: Long Packet (LPa) Structure

Notes:

1. Figure 5.4.1-1 and Figure 5.4.1-2 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

2. The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.

LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11

LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11

LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

5.3.2 Bit Order of the Byte on Packet

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

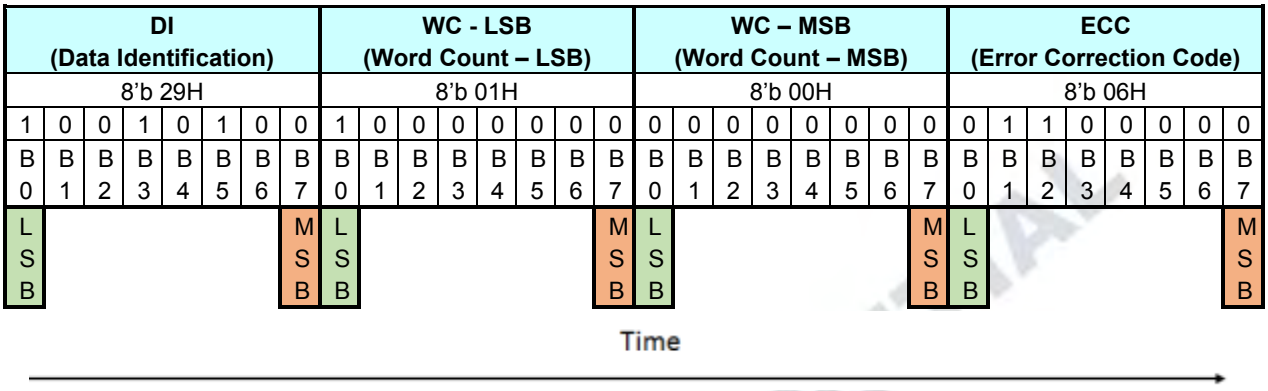


Figure 5.3.2-1: Bit order of the byte on packet

5.3.3 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

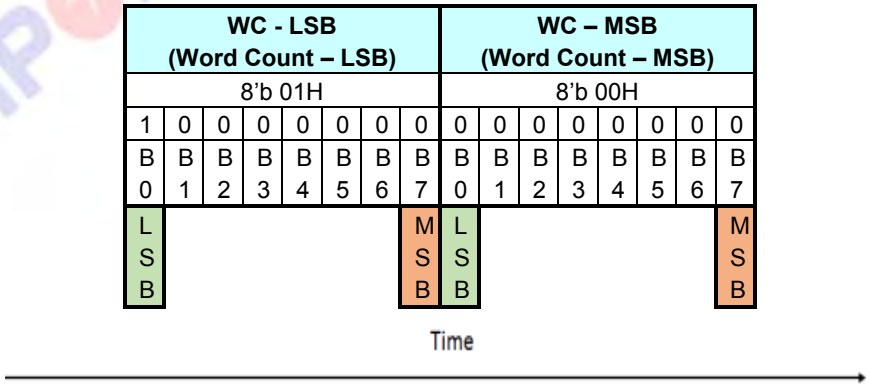


Figure 5.3.3-1: Byte order of the multiple byte information on packets

5.3.4 Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

- Short Packet (SPa)

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 07H								8'b 18H							
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure5.3.4-1: Packet Header (PH) in a Short Packet (SPa)

- Long Packet (LPa)

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure5.3.4-2: Packet Header (PH) in a Long Packet (LPa)

5.3.5 Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated, see the figure below.

DI (Data Identification)							
VC (Virtual Channel Identifier)		DT (Data Type)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure5.3.5-1: Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

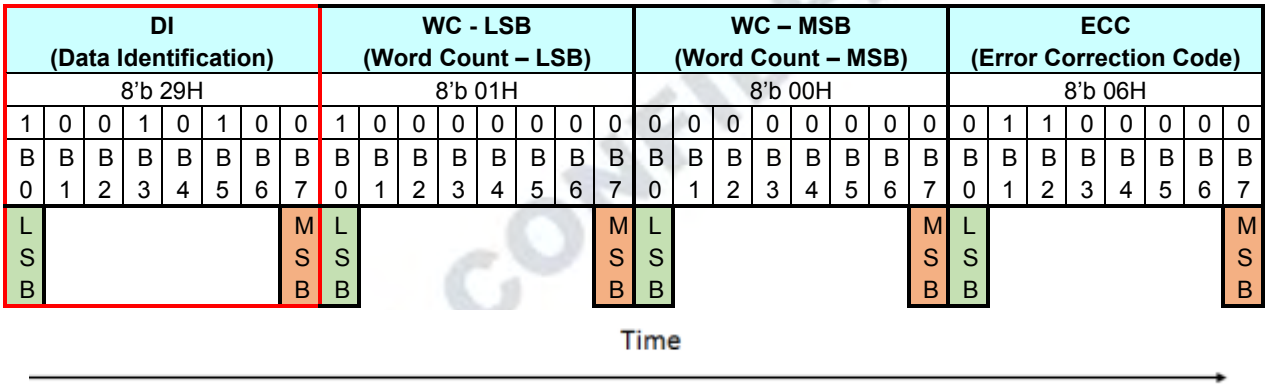


Figure5.3.5-2: Data Identification (DI) on the Packet Header (PH)

5.3.6 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7:6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB						MSB		LSB						MSB		LSB						MSB		LSB							MSB

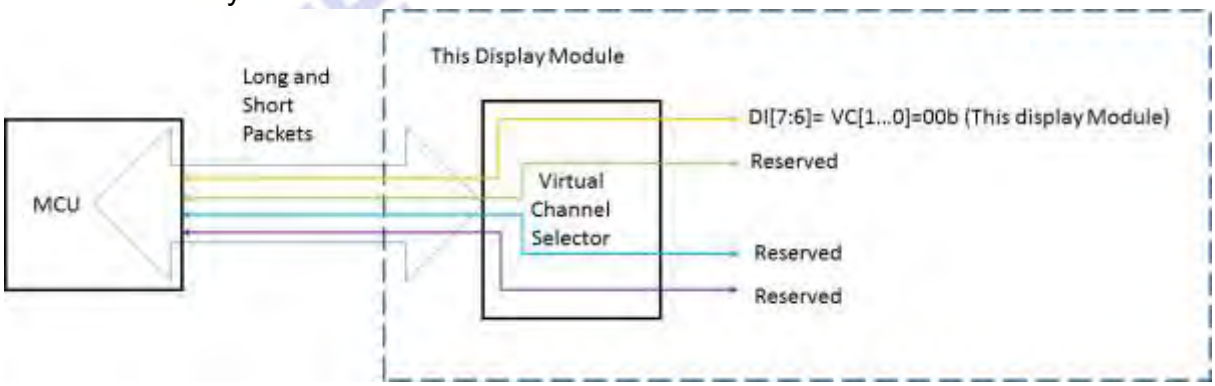
Time

Figure5.3.6-1: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the ICNL9706.
- The ICNL9706 also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) is always 0 (DI [7:6] = VC [1:0] = 00b) when the MCU sends "End of Transmission Packet" to the display module. See the section "End of Transmission Packet (EoTP)". This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1:0]) is 00b for the ICNL9706.

5.3.7 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

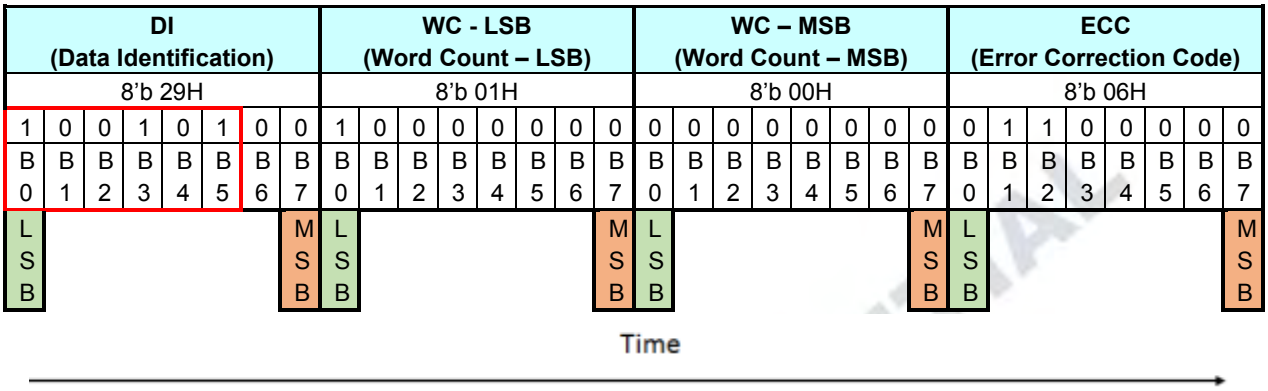


Figure5.3.7-1: Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

From the MCU to the Display Module		
Hex	Description	Short / Long Packet
01	Sync Even, V Sync Start	SPa (Short Packet)
11	Sync Even, V Sync End	SPa (Short Packet)
21	Sync Even, H Sync Start	SPa (Short Packet)
31	Sync Even, H Sync End	SPa (Short Packet)
08	End of Transmission Packet (EOTP) Note1	SPa (Short Packet)
02	Color Mode Off Command	SPa (Short Packet)
12	Color Mode On Command	SPa (Short Packet)
22	Shut Down Peripheral Command	SPa (Short Packet)
32	Turn On Peripheral Command	SPa (Short Packet)
03	Generic Short WRITE, no parameters	SPa (Short Packet)
13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
04	Generic Short READ, no parameters	SPa (Short Packet)
14	Generic Short READ, 1 parameters	SPa (Short Packet)
24	Generic Short READ, 2 parameters	SPa (Short Packet)
05	DCS Write, No Parameter	SPa (Short Packet)
15	DCS Write, 1 Parameter	SPa (Short Packet)
06	DCS Read, No Parameter	SPa (Short Packet)
37	Set Maximum Return Packet Size	SPa (Short Packet)
09	Null Packet, No Data, Note2	LPa (Long Packet)
19	Blanking Packet, no data	LPa (Long Packet)
29	Generic Long Write	LPa (Long Packet)

39	DCS Write Long	LPa (Long Packet)
1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
X0 xF	DO NOT USE All unspecified codes are reserved	

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.

2. This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module to the MCU		
Hex	Description	Short / Long Packet
02h	Acknowledge with Error Report	SPa (Short Packet)
1Ch	DCS Read Long Response	LPa (Long Packet)
21h	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
22h	DCS Read Short Response, 2 byte returned	SPa (Short Packet)
1Ah	Generic Read Long Response	LPa (Long Packet)
11h	Generic Read Short Response, 1 byte returned	SPa (Short Packet)
12h	Generic Read Short Response, 2 byte returned	SPa (Short Packet)

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Note: The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG is set to “0”.

5.3.8 Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

- Packet Data (PD) information:
- Data 0: 26Hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15Hex)
- Data 1: 01Hex (DCS's Parameter)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 26H								8'b 01H								8'b 3EH							
1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure5.3.8-1: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

- Packet Data (PD) information:
- Data 0: 10Hex (DCS without Parameter => DI (Data Type (DT)) = 05Hex)
- Data 1: 00Hex (Null)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure5.3.8-2: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

5.3.9 Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 5.4.9-2. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.9-1: Word Count (WC) in a Long Packet (LPa)

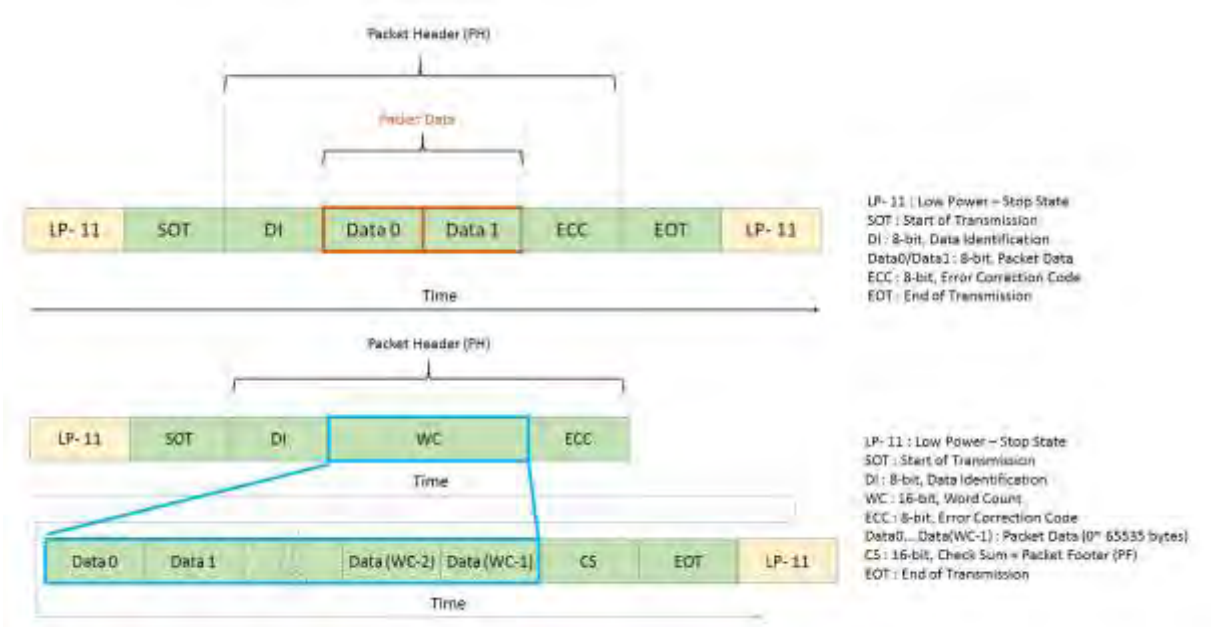


Figure 5.3.9-2: Packet Data in Short and Long Packets

5.3.10 Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors.
The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7]) D [23…0] and P [7…0] are illustrated for reference purposes below.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8’b 05H								8’b 10H								8’b 00H								8’b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.10-1: D [23:0] and D 7:0] in a Short Packet (SPa)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.10-2: D [23:0] and D 7:0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol „^“ presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D0	D1	D2		D4	D5		D7			D10	D11		D13			D16				D20	D21	D22	D23	P0							
D0	D1		D3	D4		D6		D8		D10		D12		D14			D17			D20	D21	D22	D23		P1						
D0		D2	D3		D5	D6			D9		D11	D12			D15			D18		D20	D21	D22				P2					
	D1	D2	D3				D7	D8	D9				D13	D14	D15				D19	D20	D21		D23				P3				
				D4	D5	D6	D7	D8	D9							D16	D17	D18	D19	D20		D22	D23					P4			
										D10	D11	D12	D13	D14	D15	D16	D17	D18	D19		D21	D22	D23						P5		
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.10-3: XOR Function on Short Packet (SPa)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
D0	D1	D2		D4	D5		D7			D10	D11		D13			D16				D20	D21	D22	D23	P0							
D0	D1		D3	D4		D6		D8		D10		D12		D14			D17			D20	D21	D22	D23		P1						
D0		D2	D3		D5	D6			D9		D11	D12			D15			D18		D20	D21	D22				P2					
	D1	D2	D3				D7	D8	D9				D13	D14	D15				D19	D20	D21		D23				P3				
				D4	D5	D6	D7	D8	D9							D16	D17	D18	D19	D20		D22	D23					P4			
										D10	D11	D12	D13	D14	D15	D16	D17	D18	D19		D21	D22	D23						P5		
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.10-4: XOR Function on Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

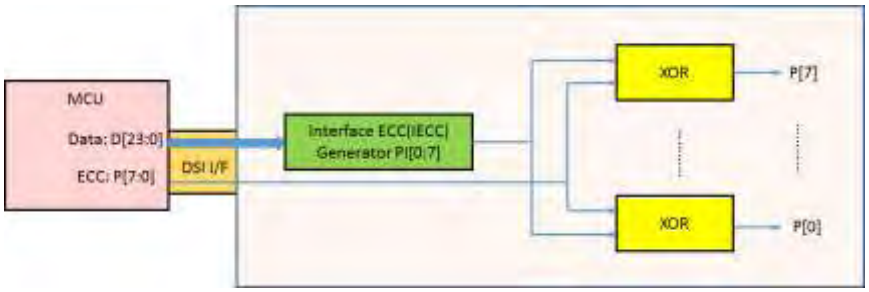


Figure 5.3.10-5: Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h.
The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

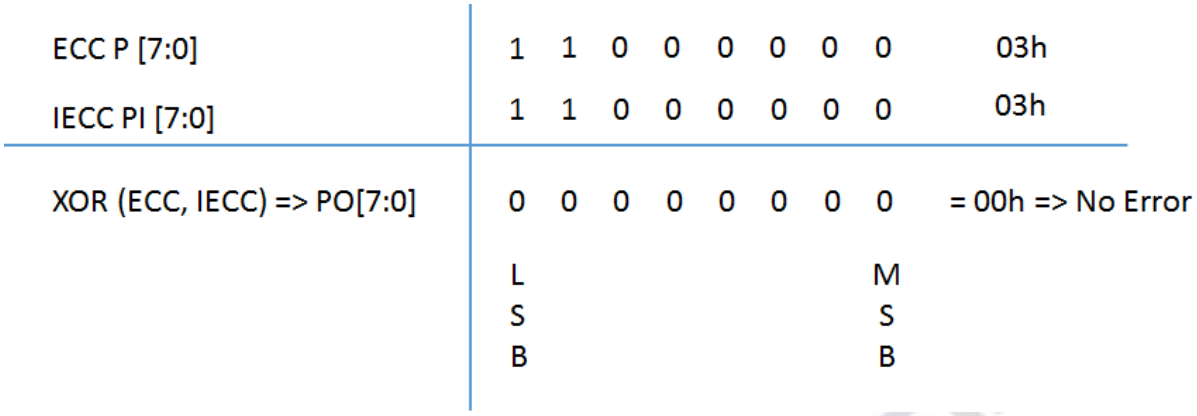


Figure 5.3.10-6: Internal XOR Calculation between ECC and IECC Values – No Error

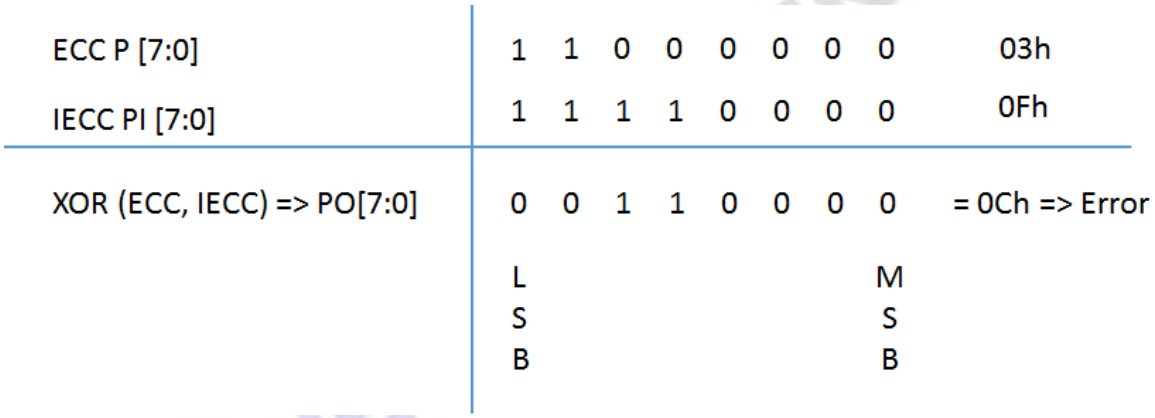


Figure 5.3.10-7: Internal XOR Calculation between ECC and IECC Values – Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h

D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table, and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), that is not correct, is D [3] More than one error is detected if the value of the PO [7…0] is not in Table for example, PO [7…0] = 0Ch.

5.3.11 Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “Word Count (WC) in a Long Packet (LPa)”.

5.3.12 Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

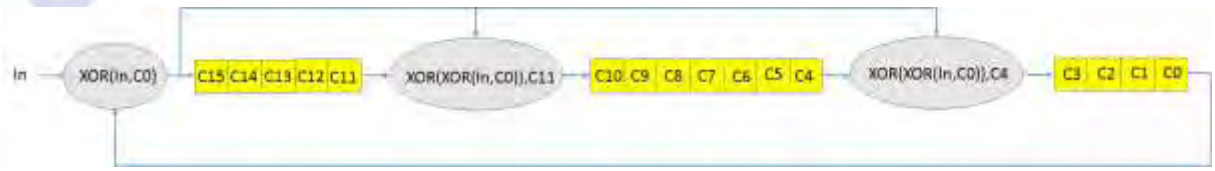


Figure 5.3.12-1: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD)

of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

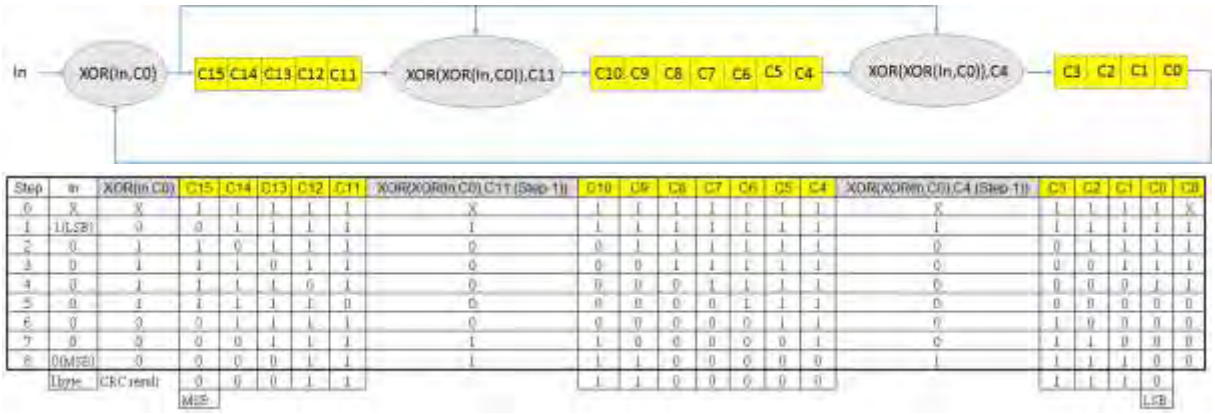


Figure 5.3.12-2: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated below

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 01H								8'b 00H								8'b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8'b 00H								8'b 0EH								8'b 1EH							
0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.3.12-3: Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

5.4、Packet Transmissions

5.4.1 Display Command Set (DCS)

Display Command Set (DCS), defined in the section “Level1 Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

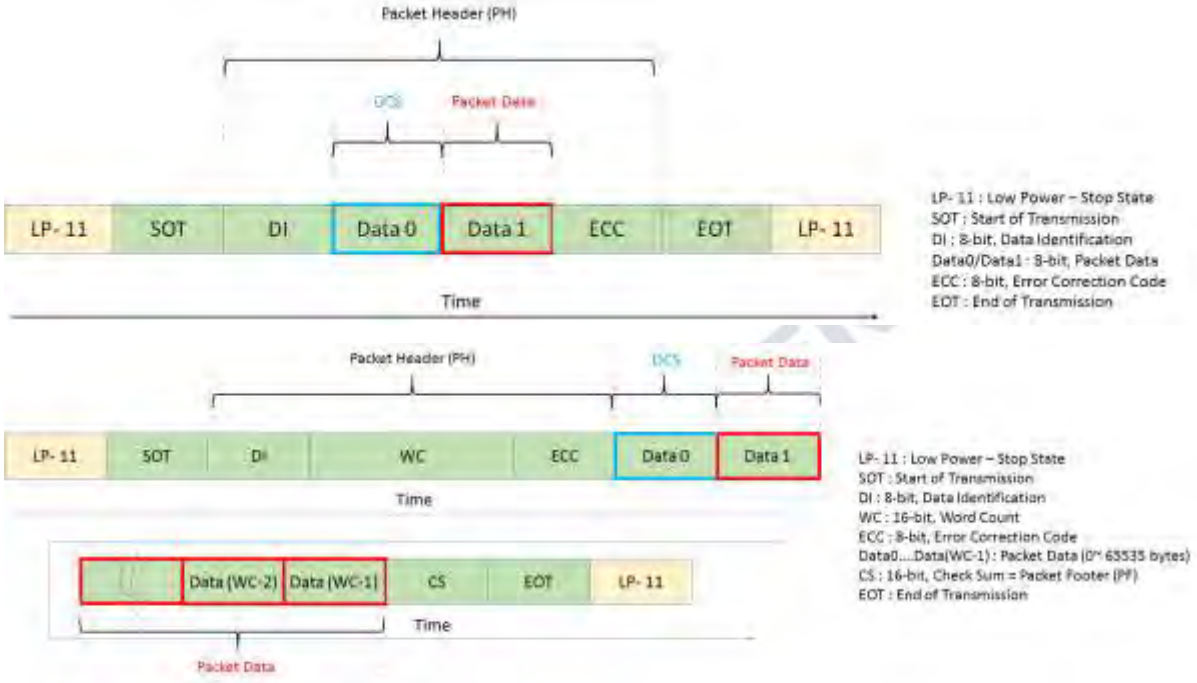


Figure 5.4.1-1: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

5.4.2 Display Command Set (DCS) Write, No Parameter (DSCWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep In (10h)
Sleep Out (11h)
Normal Display Mode On (13h)
INVOff (20h)
INVOn (21h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display On (29h)
Tearing Effect Line Off (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex

Error Correction Code (ECC)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.2-1: Display Command Set (DCS) Write, No Parameter (DCSWN-S) – Example

5.4.3 Display Command Set (DCS) Write, 1 Parameter (DSCW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Command
Gamma Curve Set (26h)
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 01H								8'b 1EH							
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.3-1: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

5.4.4 Display Command Set (DCS) Write, Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Command
NOP (00h) Note 1
Software Reset (01h), Note 1
Sleep In (10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
INVOff (21h) , Note 1
INVOn (22h) , Note 1
All Pixel Off (22h) , Note 1
All Pixel On (23h) , Note 1
GAMSET (26h) , Note 2
Display Off (28h) , Note 1
Display On (29h) , Note 1
Tearing Effect Line Off (34h) , Note 1
Tearing Effect Line On (35h) , Note 2
MADCTR (36h)
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
COLMOD (3Ah) , Note 2
Tearline (44h)
WRDISBV (51h) , Note 2
WRCTRLD (53h)
WRCABC (55h) , Note 2
WRCABCMB (5Eh)

Notes :

1. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, No Parameter.

2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 01H								8'b 00H								8'b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8'b 10H								8'b 06H								8'b 1FH							
0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.4-1: Display Command Set (DCS) Write, Long (DCSWL-S) with DCS Only– Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 02H								8'b 00H								8'b 13H							
1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (DCS)								Data 1 (Parameter)								CRC-LSB								CRC-MSB							
8'b 26H								8'b 01H								8'b D2H								8'b 96H							
0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.4-2: Display Command Set (DCS) Write, Long with DCS and 1 Parameter – Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: "Column Address Set (2Ah)" (For example only), Display Command Set (DCS)
  - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 05H								8'b 00H								8'b 36H							
1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (DCS)								Data 1 (1st Parameter)								Data 2 (2nd Parameter)								Data 3 (3rd Parameter)							
8'b 2AH								8'b 00H								8'b 12H								8'b 01H							
0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4 (4th Parameter)								CRC – LSB								CRC – MSB							
8'b EFH								8'b BDH								8'b 2AH							
1	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1	0	1	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.4-3: Display Command Set (DCS) Write, Long with DCS and 4 Parameter – Example

5.4.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Command
RDDID (04h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
GSL (45h)
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated for reference purposes below.

- Step1

The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)

DI (Data Identification)								MRPS – LSB								MRPS – MSB								ECC (Error Correction Code)							
8'b 37H								8'b 01H								8'b 00H								8'b 1DH							
1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.5-1: Set Maximum Return Packet Size (SMRPS-S) – Example

- Step 2

The MCU wants to receive the value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
  - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

DI (Data Identification)								Data 0 (DCS)								Data 1 (Always 8'b 00H)								ECC (Error Correction Code)							
8'b 06H								8'b DAH								8'b 00H								8'b 1FH							
0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.5-2: Display Command Set (DCS) Read, No Parameter (DCSRN – S) – Example

- Step 3

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section "Acknowledge with Error Report (AwER)".
2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

5.4.6 Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

DI (Data Identification)								**WC – LSB (Word Count – LSB)**								**WC – MSB (Word Count – MSB)**								**ECC (Error Correction Code)**							
8'b 09H								8'b 05H								8'b 00H								8'b 30H							
1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								**Data 1**								**Data 2**								**Data 3**							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4								CRC – LSB								CRC – MSB							
8’b E2H								8’b 59H								8’b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.6-1: Null Packet, No Data (NP- L) – Example

5.4.7 End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before “End of Transmission” (EoT).The MCU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application. The display module does or does not receive “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=> Display Module	Support with and without EoTP	Support with and without EoTP
Display Module => MCU	HS mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code

DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8'b 08H								8'b 0FH								8'b 0FH								8'b 01H							
0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.7-1: End of Transmission Packet (EoTP)

Some examples of the "End of Transmission Packet" (EoTP) are illustrated for reference purposes below.

Figure 5.4.7-2: End of Transmission Packet (EoTP) – Example

5.4.8 Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

DI (Data Identification)								AwER – LSB								AwER – MSB								ECC (Error Correction Code)							
8'b 02H								8'b 00H								8'b 01H								8'b 3AH							
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.8-1: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

Figure 5.4.8-2: Error Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands. The bit D0 of the "Read Display Signal Mode (0Eh)" command will be set to 1 if a received packet includes an error. The amount of packets, which include an ***ECC or CRC*** error, is calculated in the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h and set the bit D0 of the "Read Display Signal Mode (0Eh)" command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

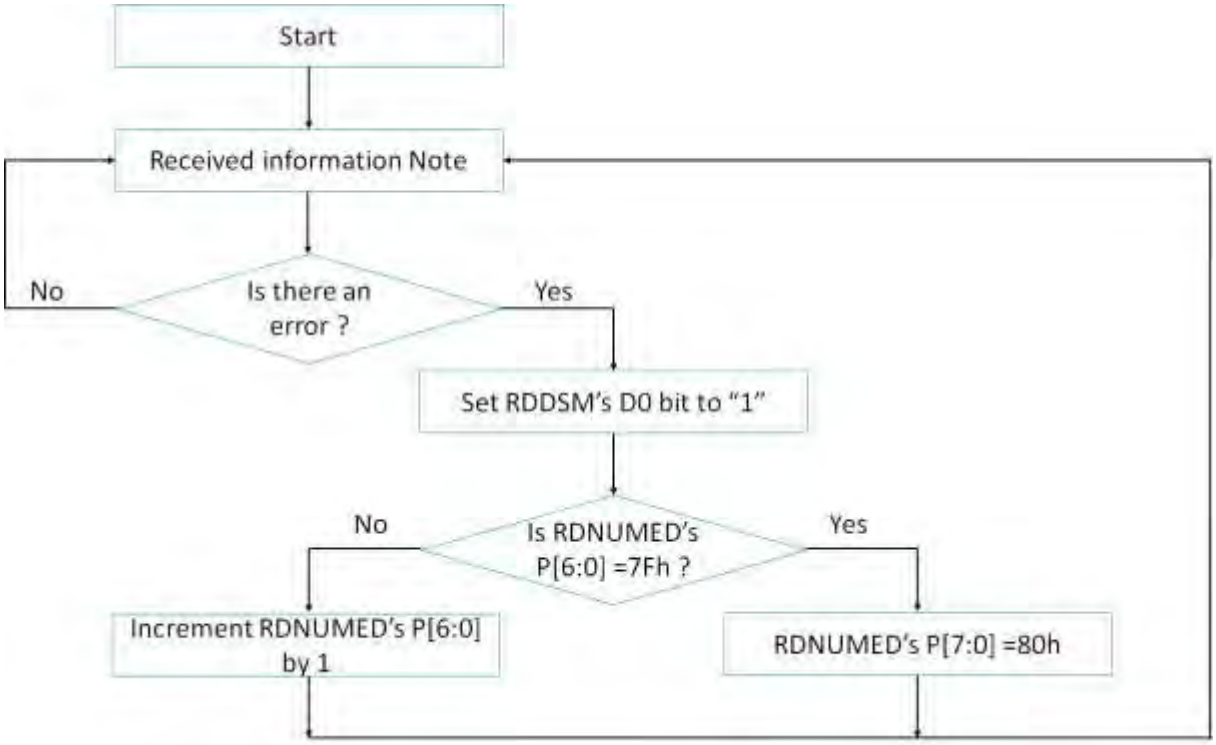


Figure 5.4.8-2: Flow Chart for Errors on DSI

Notes:

1. This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.

2. CRC or ECC error

5.4.9 DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module. A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
- Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: 89hex
- Data 1: 23hex
- Data 2: 12hex
- Data 3: A2hex
- Data 4: E2hex
- Packet Footer (PF)

DI (Data Identification)								**WC – LSB (Word Count – LSB)**								**WC – MSB (Word Count – MSB)**								**ECC (Error Correction Code)**							
8'b 1CH								8'b 05H								8'b 00H								8'b 29H							
0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								**Data1**								**Data2**								**Data3**							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4								CRC – LSB								CRC – MSB							
8'b E2H								8'b 59H								8'b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.9-1: DCS Read Long Response (DCSRR-L) – Example

5.4.10 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 00hex (Always)
- Error Correction Code (ECC)

DI (Data Identification)								**Data0 (Packet Data)**								**Data1 (Always 8'b 00h)**								**ECC (Error Correction Code)**							
8'b 21H								8'b 45H								8'b 00H								8'b 01H							
1	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.10-1: DCS Read Short Response, 1Byte Return (DCSRR1-S) – Example

5.4.11 DCS Read Short Response, 2 Byte Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 32hex
- Error Correction Code (ECC)

DI (Data Identification)								**Data 0 (Packet Data)**								**Data1**								**ECC (Error Correction Code)**							
8'b 22H								8'b 45H								8'b 32H								8'b 0FH							
0	1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5.4.11-1: DCS Read Short Response, 2Byte Returned (DCSRR2-S) – Example

5.5、Communication Sequences

5.5.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “Interface Level Communication” and “Packet Level Communication”. This communication sequence description is for DSI data lanes (D3P/N, D2P/N, D1P/N and D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

5.5.1 Table 1: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra- Low power state
	RAR	Remote application reset
	TEE	Tearing effect event (Not supported)
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

5.5.1 Table 2: Packet level communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.5.2 Sequences –DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used is described on following tables.

Table 5.5.2-1 DCS Write,1 parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5.5.2-2 DCS Write,1 parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5.5.2-3 DCS Write,1 parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	<=	ACK		No error
9		-	<=	LP-11		
10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						

13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.3 Sequences –DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 5.5.3-1 DCS Write, No parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5.5.3-2 DCS Write, No parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5.5.3-3 DCS Write, No parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	<=	ACK		No error
9		-	<=	LP-11		

10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						
13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.4 Sequences –DCS Write, Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 5.5.4-1 DCS Write, Long Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5.5.4-2 DCS Write, Long Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5.5.4-3 DCS Write, Long Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13

7						
8		-	<=	ACK		No error
9		-	<=	LP-11		
10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						
13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.5 Sequences –DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

Table 5.5.5-1 DCS Read, No Parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	

16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>		-	End

5.5.6 Sequences –Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Table 5.5.6-1 Null Packet, No Data Sequence – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>			End of transmission Packet
4	-	LP-11	=>	-	-	End

5.5.7 Sequences –End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

Table 5.5.7-1 End of Transmission Packet – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>			End of transmission Packet
4	-	LP-11	=>	-	-	End

5.6、Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.6.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the

first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.
Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.
Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

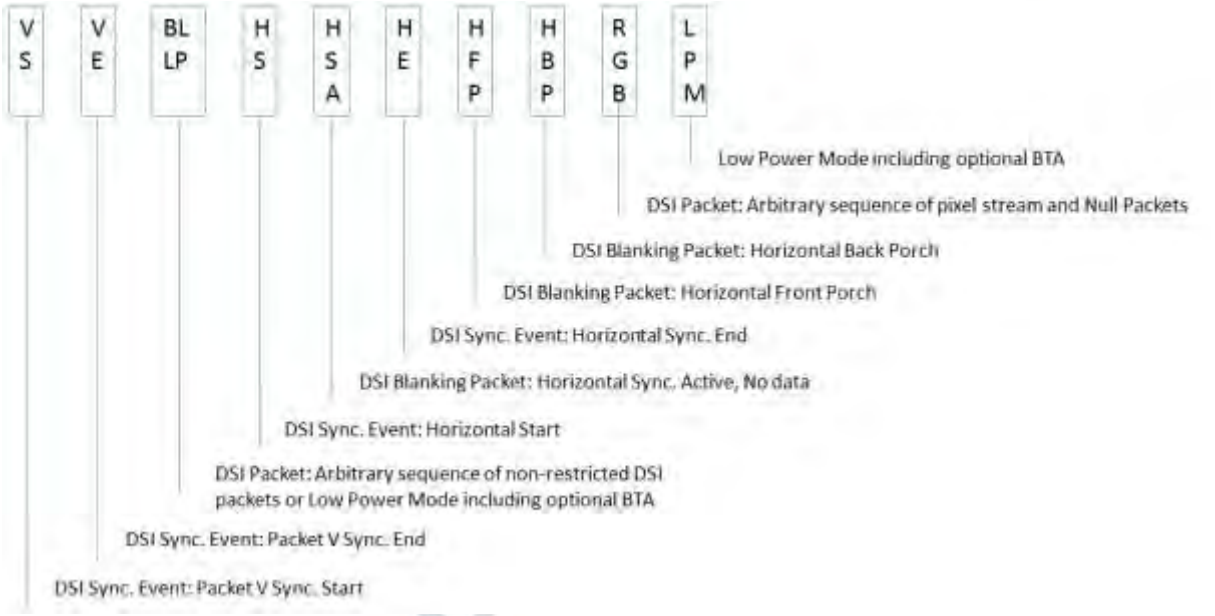


Figure 5.6.1-1: DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.6.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

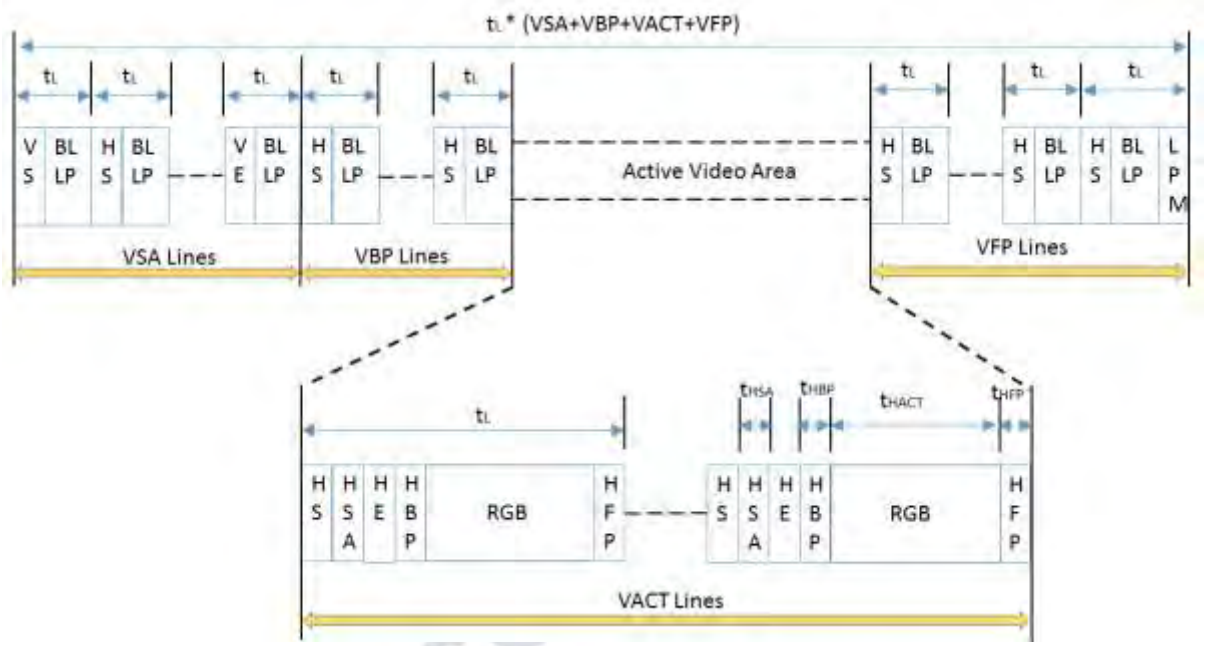


Figure 5.6.2-1: DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.6.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.

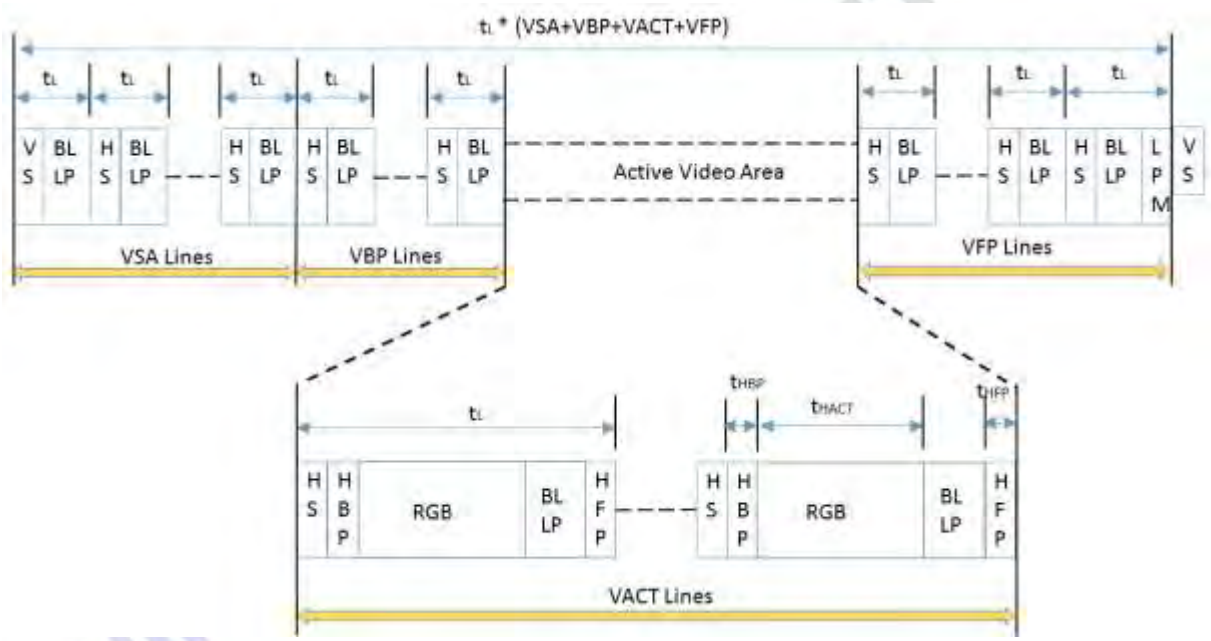


Figure 5.6.2-1: DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.7、Display Data Format

5.7.1 16-bit per Pixel, Long Packet, Data Type 001110 (0Eh)

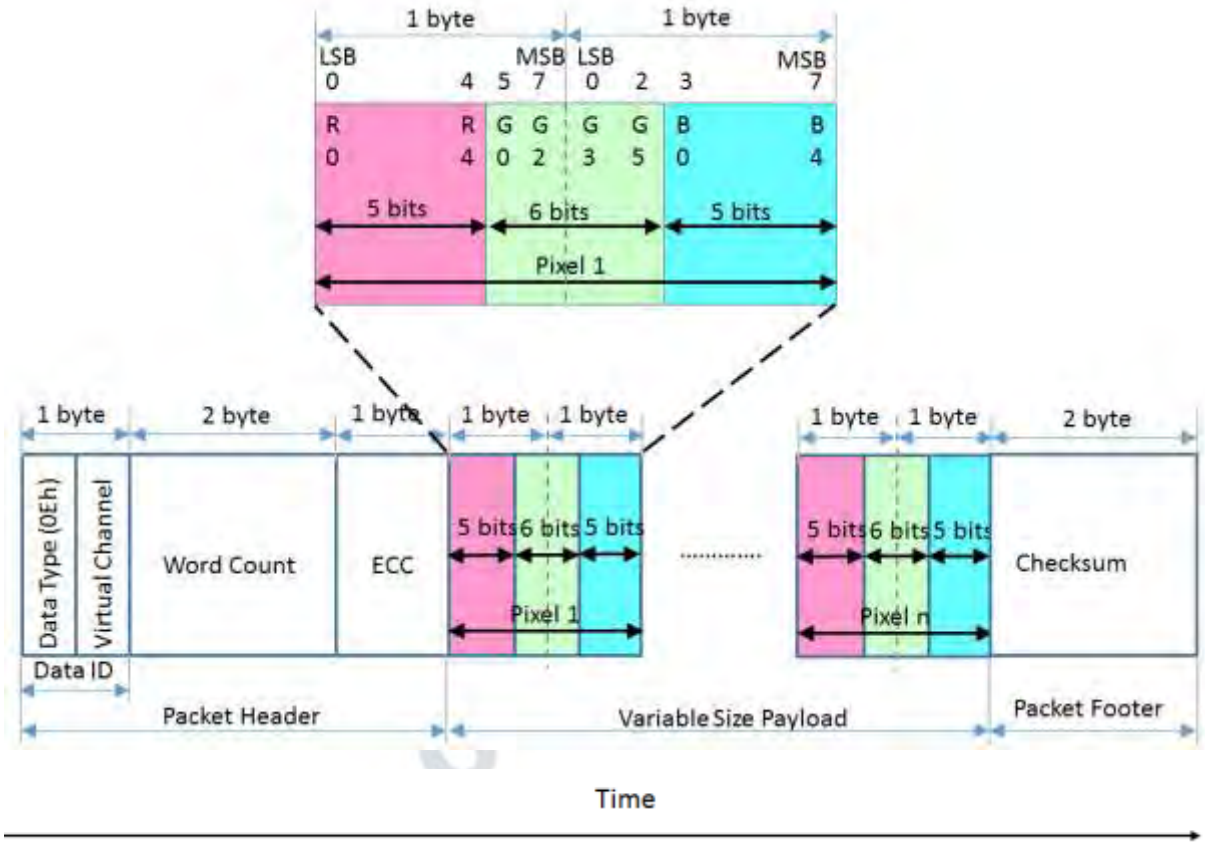


Figure 5.7.1-1: 16-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

5.7.2 18-bit per Pixel, Long Packet, Data Type 011110 (1Eh)

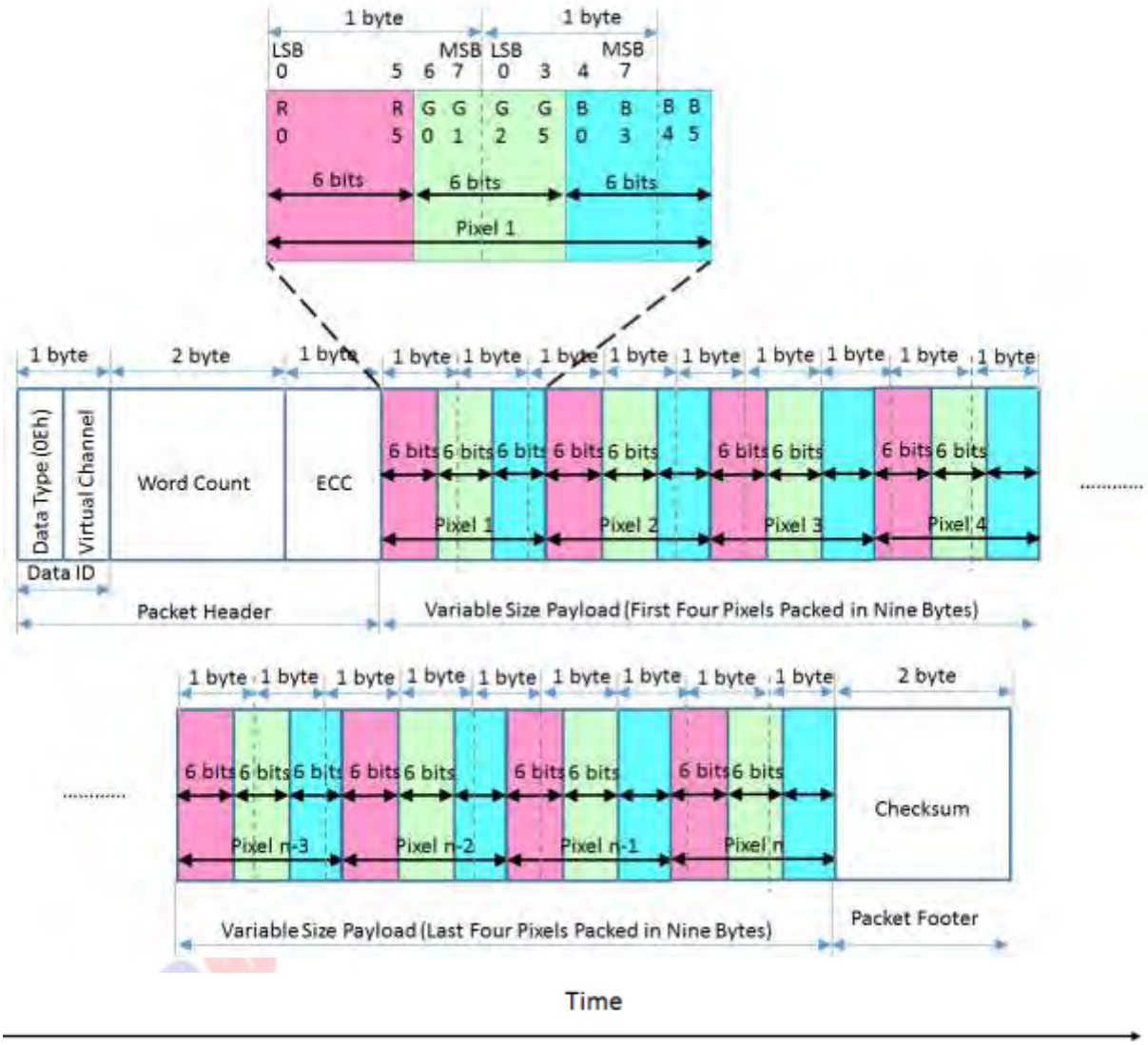


Figure 5.7.2-1: 18-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last. Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the

display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device.
For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.
With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

5.7.3 18-bit per Pixel, Long Packet, Data Type 101110 (2Eh)

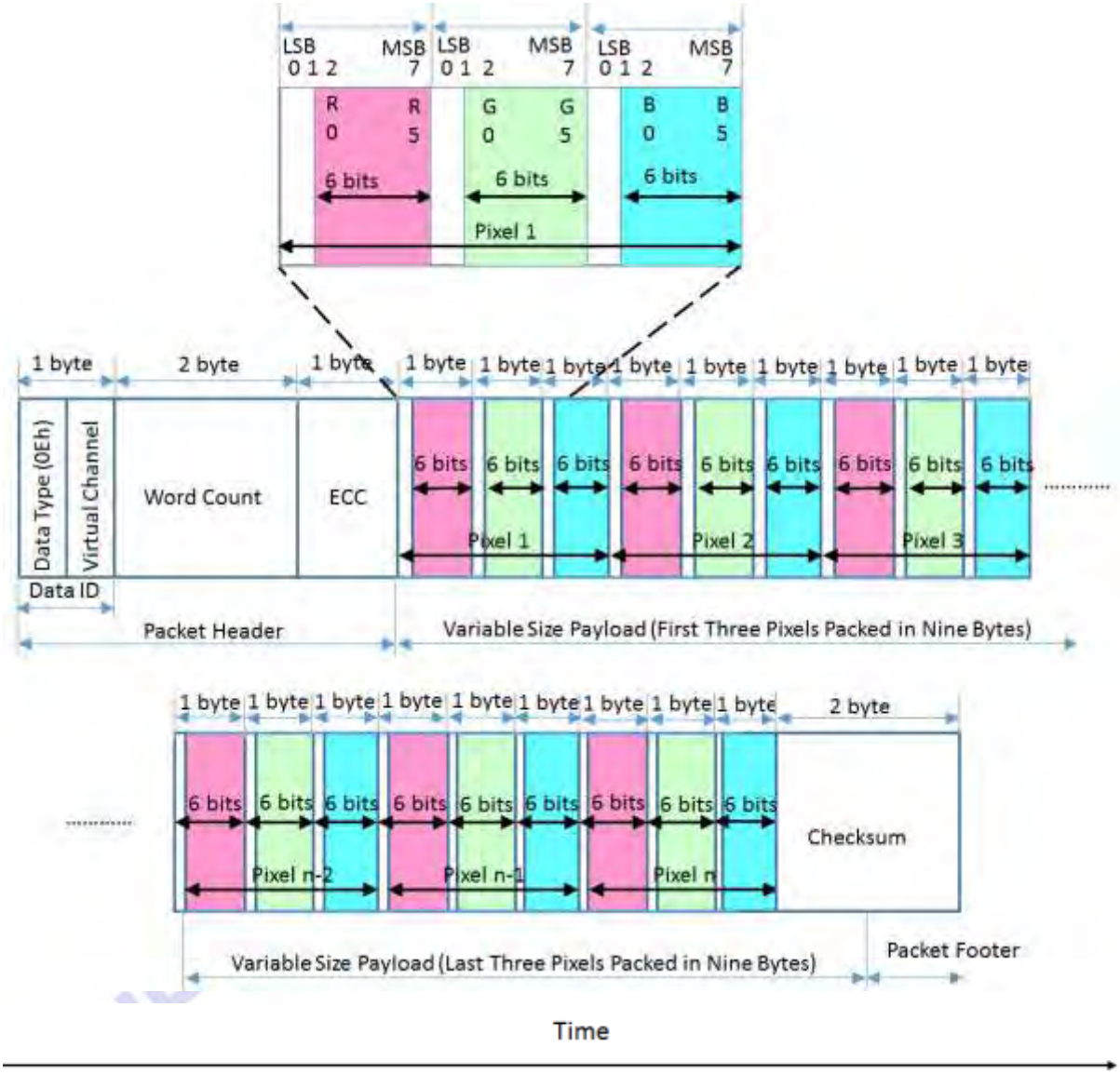


Figure 5.7.3-1: 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum.

The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.7.4 24-bit per Pixel, Long Packet, Data Type 111110 (3Eh)

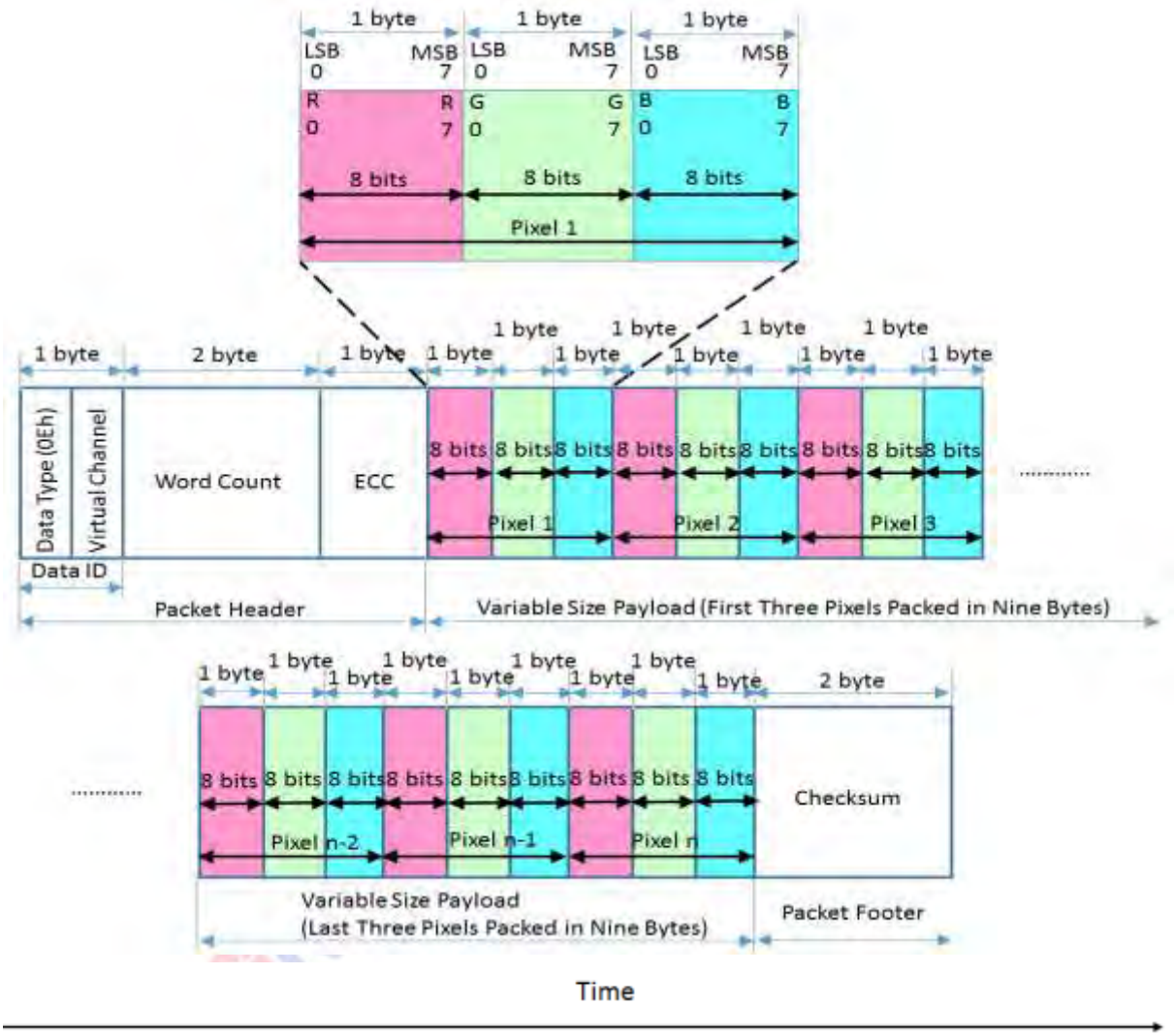


Figure 5.7.4-1: 24-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

6、Functions

6.1、Oscillator

The ICNL9706 can oscillate an internal R-C oscillator with an internal oscillation resistor. The oscillation frequency is changed according to the internal register if needed. The default frequency is 45MHz. The oscillation frequency tolerance is ±5%.

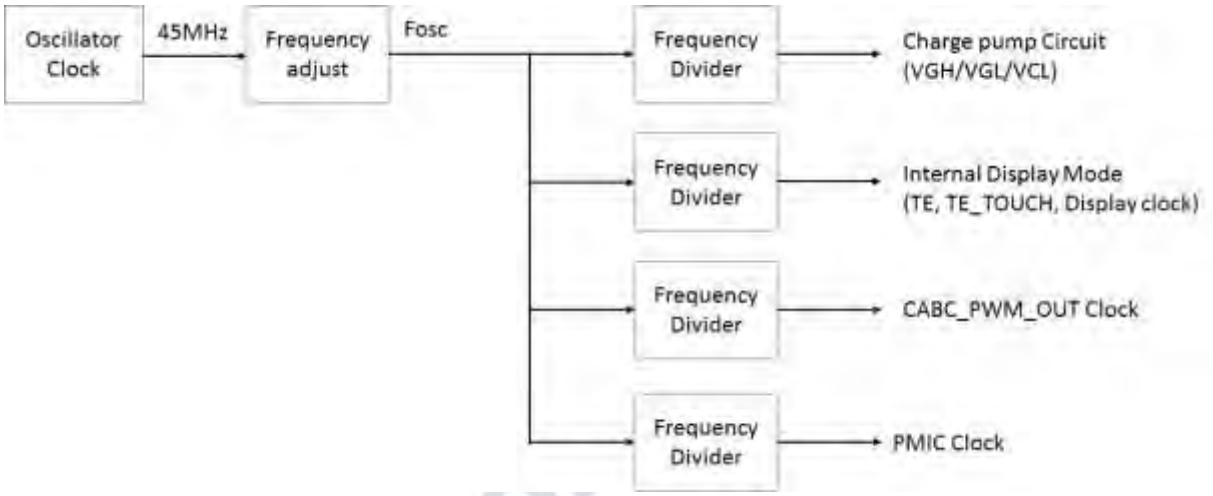


Figure 6.1-1: Oscillator architecture

6.2、Content Adaptive Brightness Control (CABC)

The CABC, a dynamic backlight control function, drastically reduces the power consumption of the luminance source. The ICNL9706 will refer the gray scale content of the display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

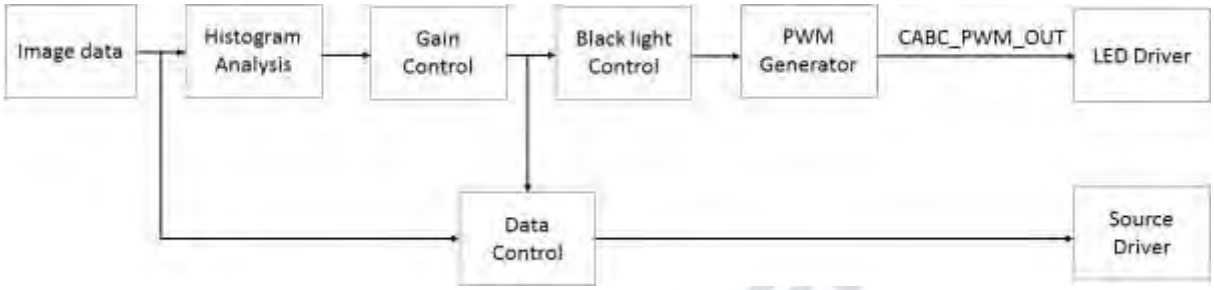


Figure 6.2-1: CABC Block Diagram

The ICNL9706 can calculate the backlight brightness level and send a CABC_PWM_OUT pulse to the LED driver via CABC_PWM_OUT pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{CABC\_PWM\_OUT} = \frac{32MHz}{(PWM\_DIV[7:0]+1)x255}$$

The basic timing diagram which is applied from the ICNL9706 in order to control the LED driver

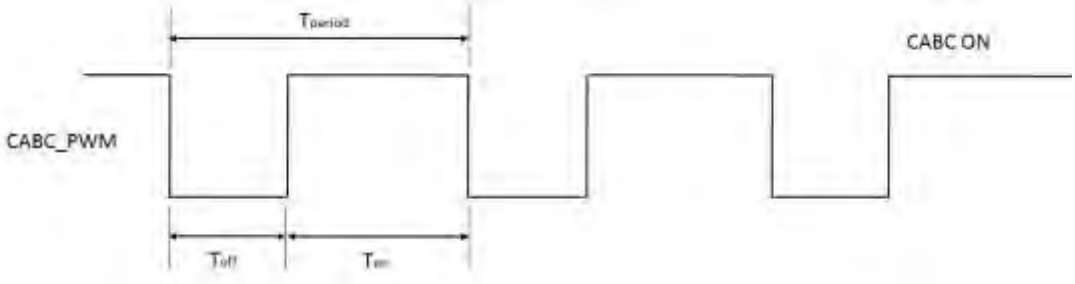


Figure6.2-2: CABC_PWM_OUT On/Off Period

6.3、Gamma Function

The structure of grayscale amplifier is shown as below. The 19 voltage levels between VSPR and VSNR are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro- adjustment register.

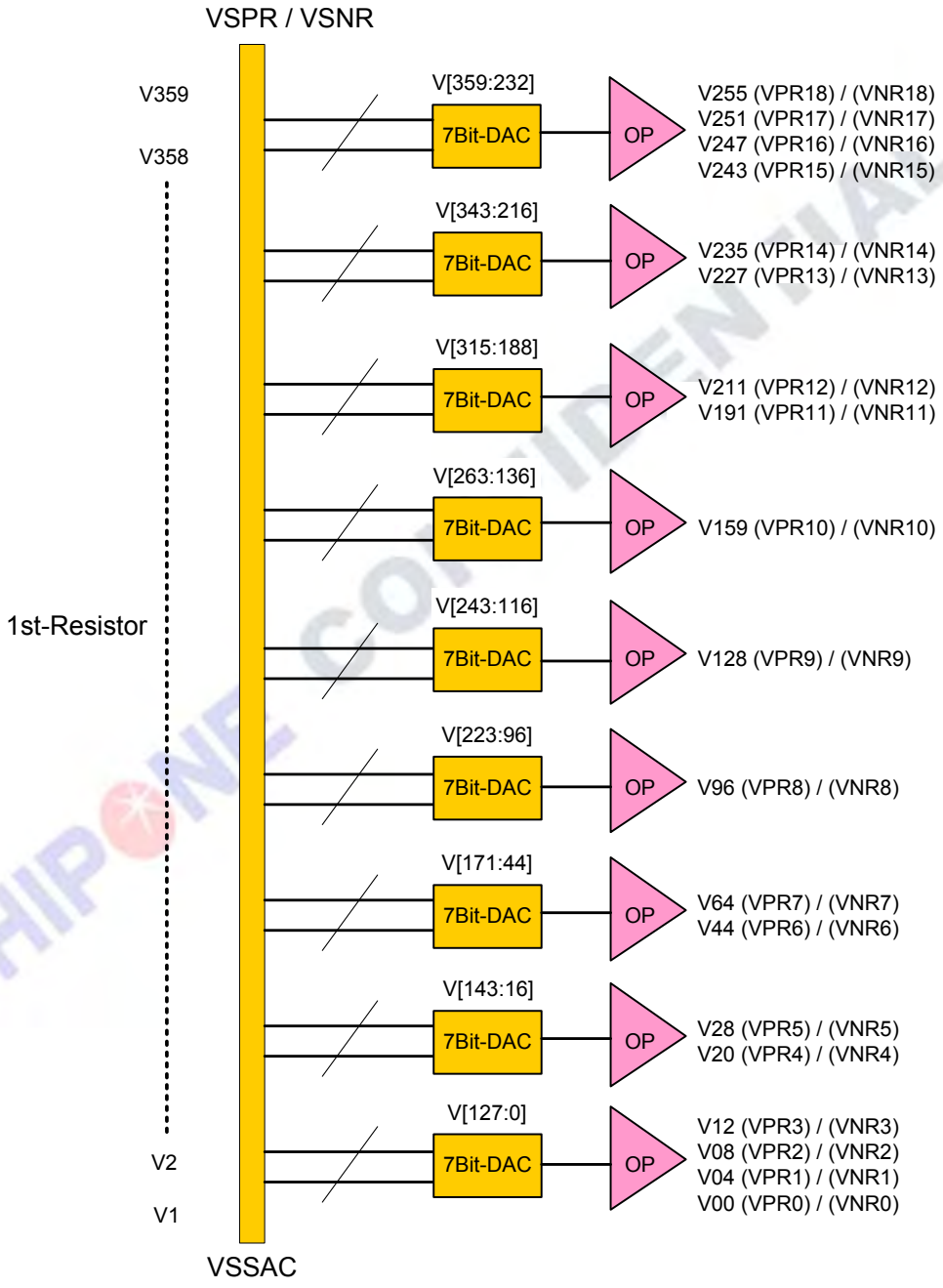


Figure6.3-1: Gamma register stream and Gamma reference voltage

6.4、OTP Programing Flow

6.4.1 Level 2 OTP Programing flow

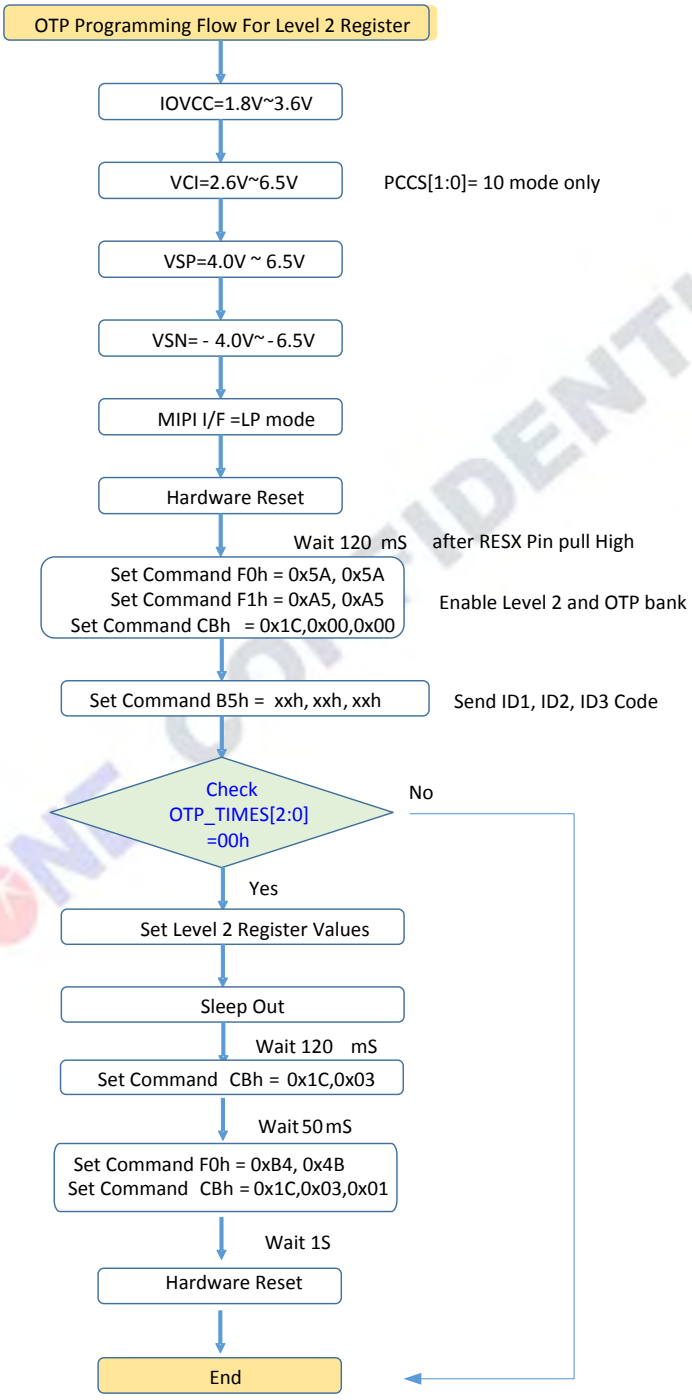


Figure6.4.1-1: Level 2 OTP Programing Flow

6.4.2 ID code and VCOM OTP Programing flow

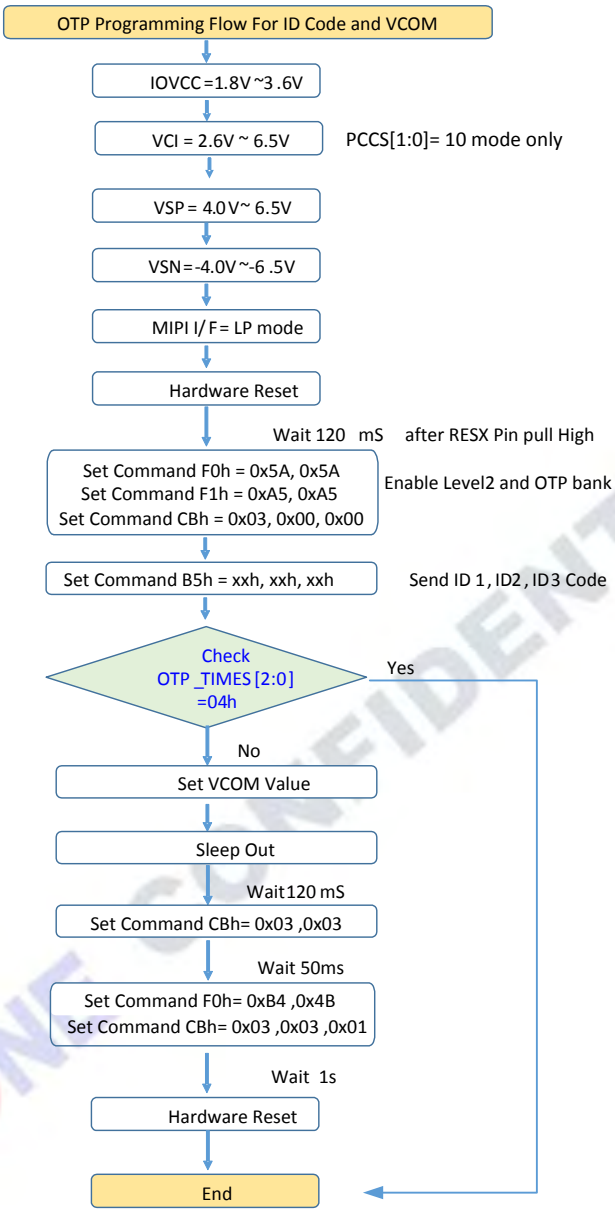


Figure6.4.2-1: ID code and VCOM OTP Programing Flow

6.5、Tearing Effect

6.5.1 Tearing effect output line

The Tearing Effect output line supplies a panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

Figure 6.5-1: Tearing effect output signal mode 1

t_{vdh}= The LCD display is not updated from the Frame Memory

t_{vdl}= The LCD display is updated from the Frame Memory

6.5.2 Tearing effect line timing

The Tearing Effect signal is described below:

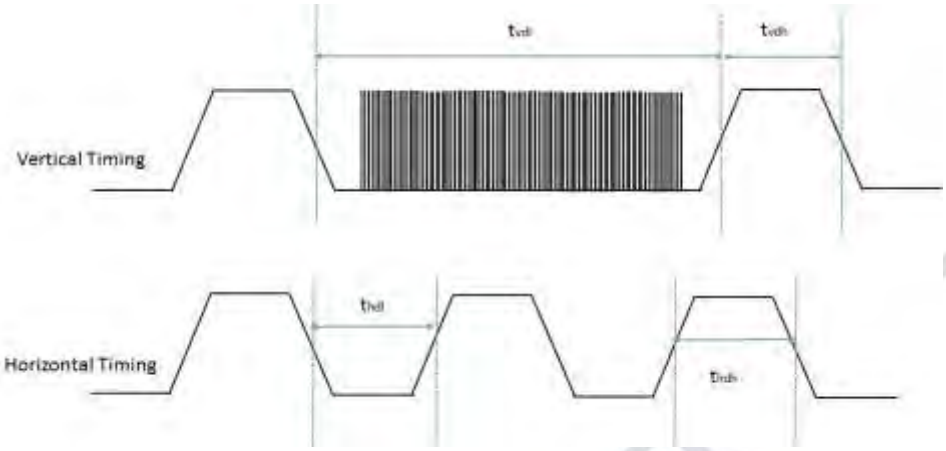


Figure 6.5.2-1: Tearing effect output line – tearing effect line timing

Condition : Idle mode off, Frame Rate =60Hz, Resolution: 800(RGB) *1280

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
TE	t_{vdl}	Vertical Timing Low Duration	15			mS	
TE	t_{vdh}	Vertical Timing High Duration	VFP+VBP+VHP			nS	
TE	Tr	Rise Time			15	nS	
TE	Tf	Fall Time			15	nS	

Note MADCTL ML=0 and ML=1

The signal's rise and fall times (T_r, T_f) are stipulated to be equal to or less than 15nS.

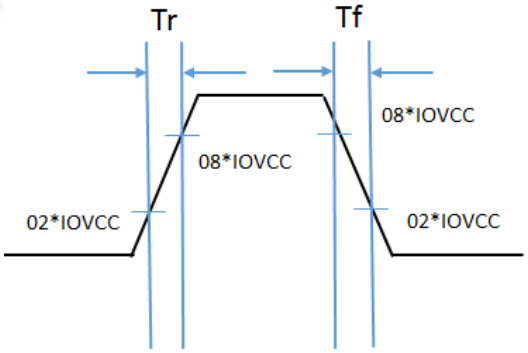


Figure 6.5.2-2: Tearing effect output line –definition of Tr,Tf

6.6、Sleep Out – Command

6.6.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1). The flow chart for this internal function is following:

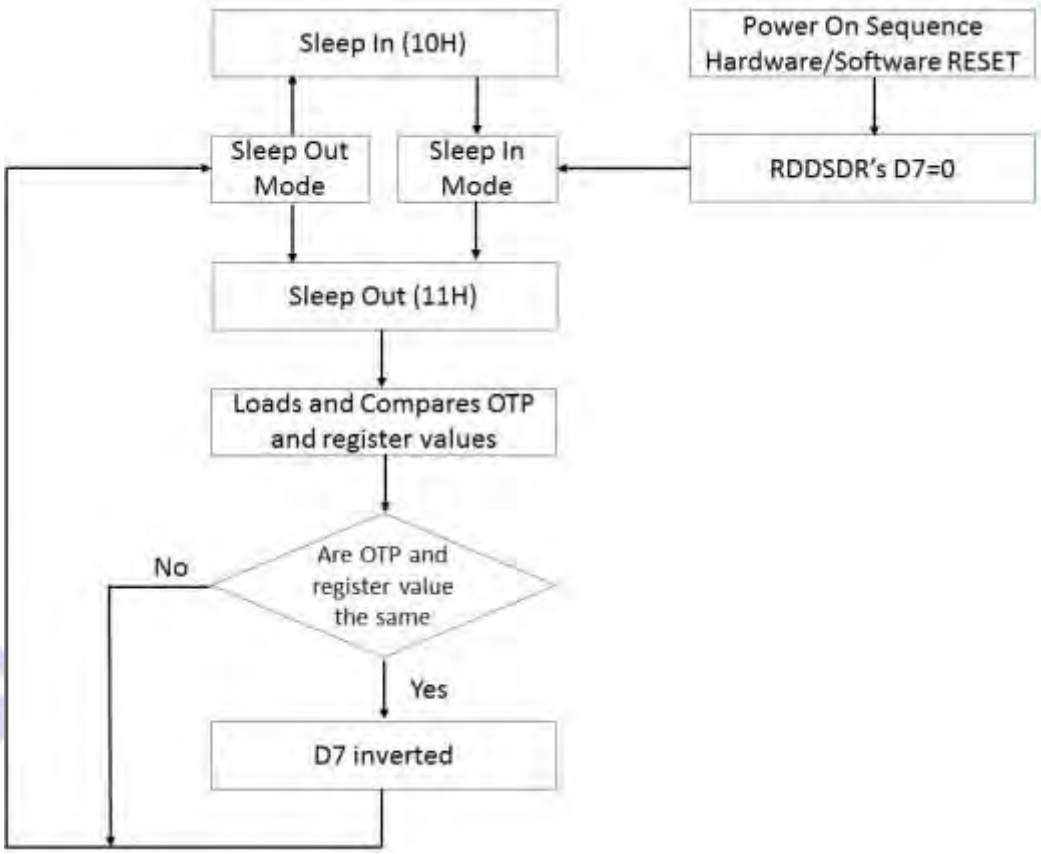


Figure 6.6-1: Sleep out flow chart-command and self-diagnostic functions

6.6.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements. The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.

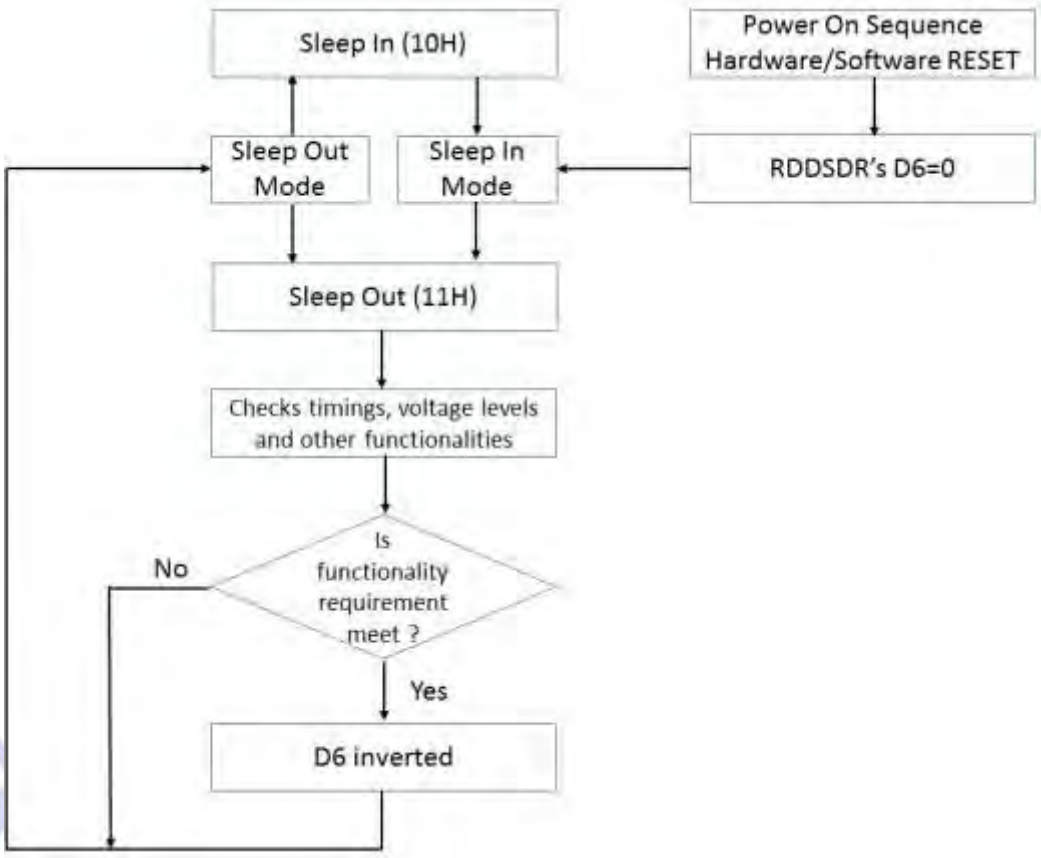


Figure 6.6.2-1: Sleep out flow chart internal function detection

Note: There is needed 120msec. After Sleep Out –command, when there is changing from sleep In –mode to Sleep Out –mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

7、Power On/ OFF Sequence

7.1、Power ON Sequence

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and IOVCC have been applied.

The power on sequence for different power input modes are shown below figures.

Table 7.1-1 Power On Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T_{On1}	0			mS	
T_{On2}	0			mS	
T_{On3}	0			mS	
T_{On4}	0			mS	
T2		No limit		uS	
T3	0			mS	
T4	10			mS	
T5	20			mS	
T6	0		T4	mS	
T7	10			uS	
T8	120			mS	

7.1.1 Power ON-PCCS[1:0]=L,L Mode Sequence

Application Power: IOVCC, VSP, VSN, VGH, VGL

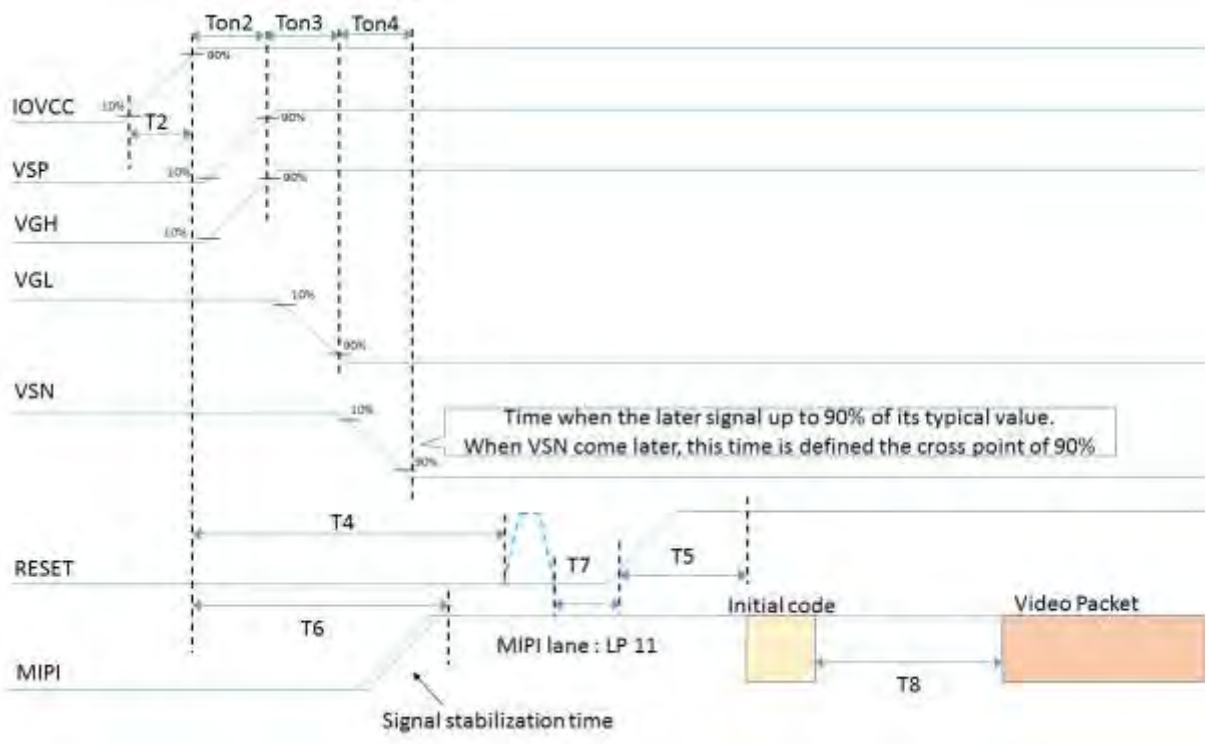


Figure 7.1.1-1: Power On-PCCS[1:0]= L,L mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note2: This power-on sequence is based on adding schottky diode on VGL pin to ground.

Note3: Keep VGH is equal to or larger than VSP during power on sequence.

7.1.2 Power ON- PCCS[1:0] =H,L Mode Sequence

Application Power: IOVCC, VCI

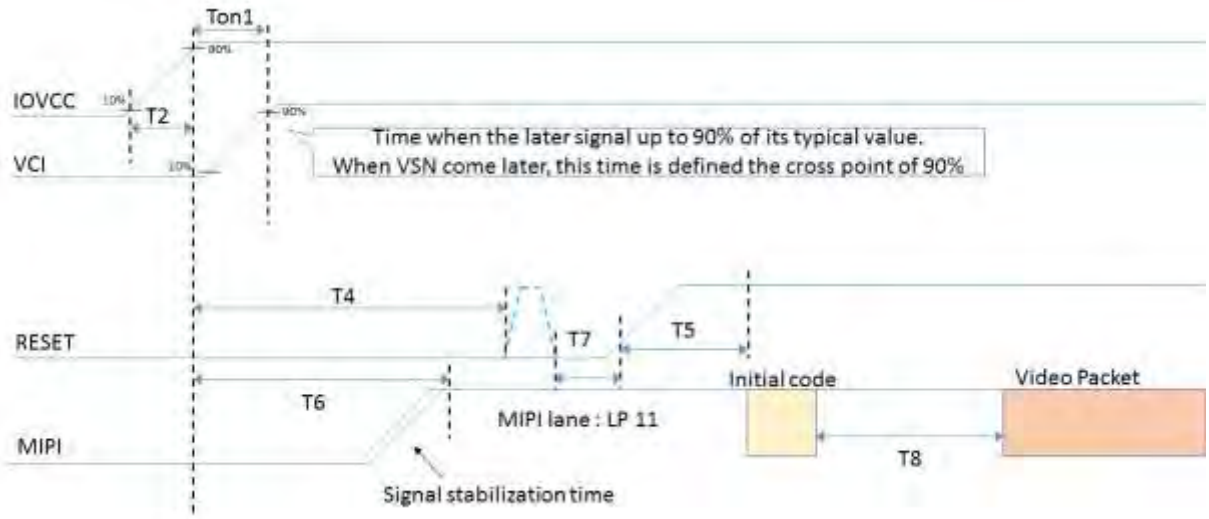


Figure 7.1.2-1: Power On-PCCS[1:0]= H,L mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note2: This power-on sequence is based on adding schottky diode on VGL pin to ground.

7.1.3 Power ON- PCCS[1:0]= H,H Mode Sequence

Application Power: IOVCC, VSP, VSN

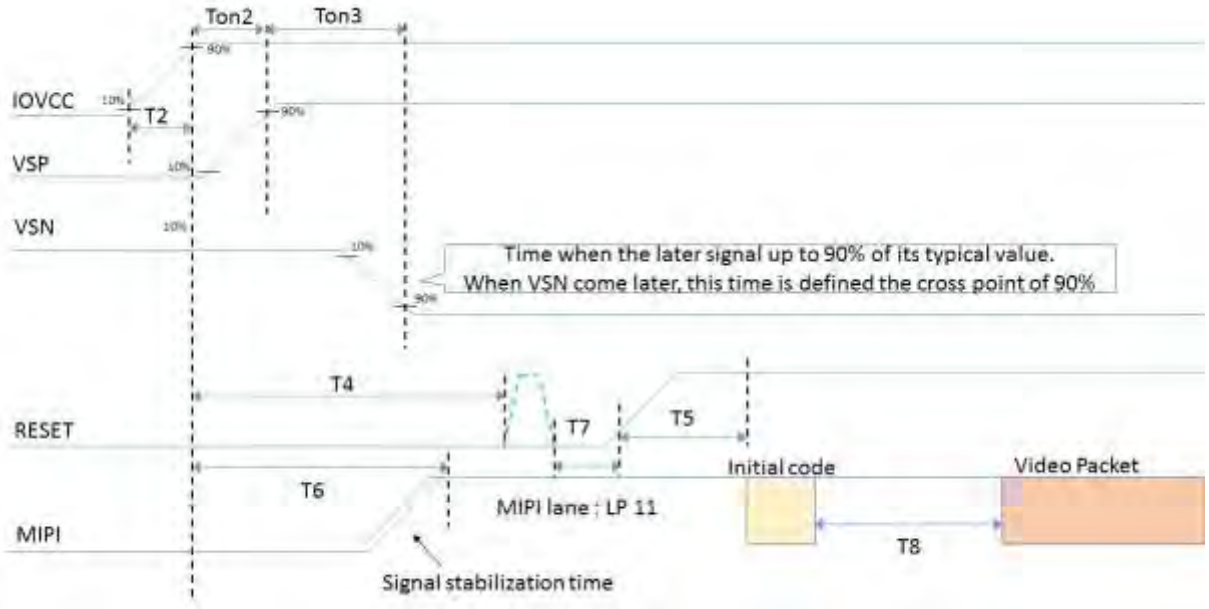


Figure 7.1.3-1: Power On-PCCS[1:0]= H,H mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note2: This power-on sequence is based on adding schottky diode on VGL pin to ground.

7.2、Power OFF Sequence

The power off sequence for different power input modes are shown below figures.

Table 7.2-1 Power Off Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T_{off1}	0			mS	
T_{off2}	0			mS	
T_{off3}	0			mS	
T_{off4}	0			mS	
T9	150			uS	
T12	0			mS	
T13	0			mS	
T14	100			mS	

7.2.1 Power OFF-PCCS[1:0]=L,L Mode Sequence

Application Power: IOVCC, VSP, VSN, VGH, VGL

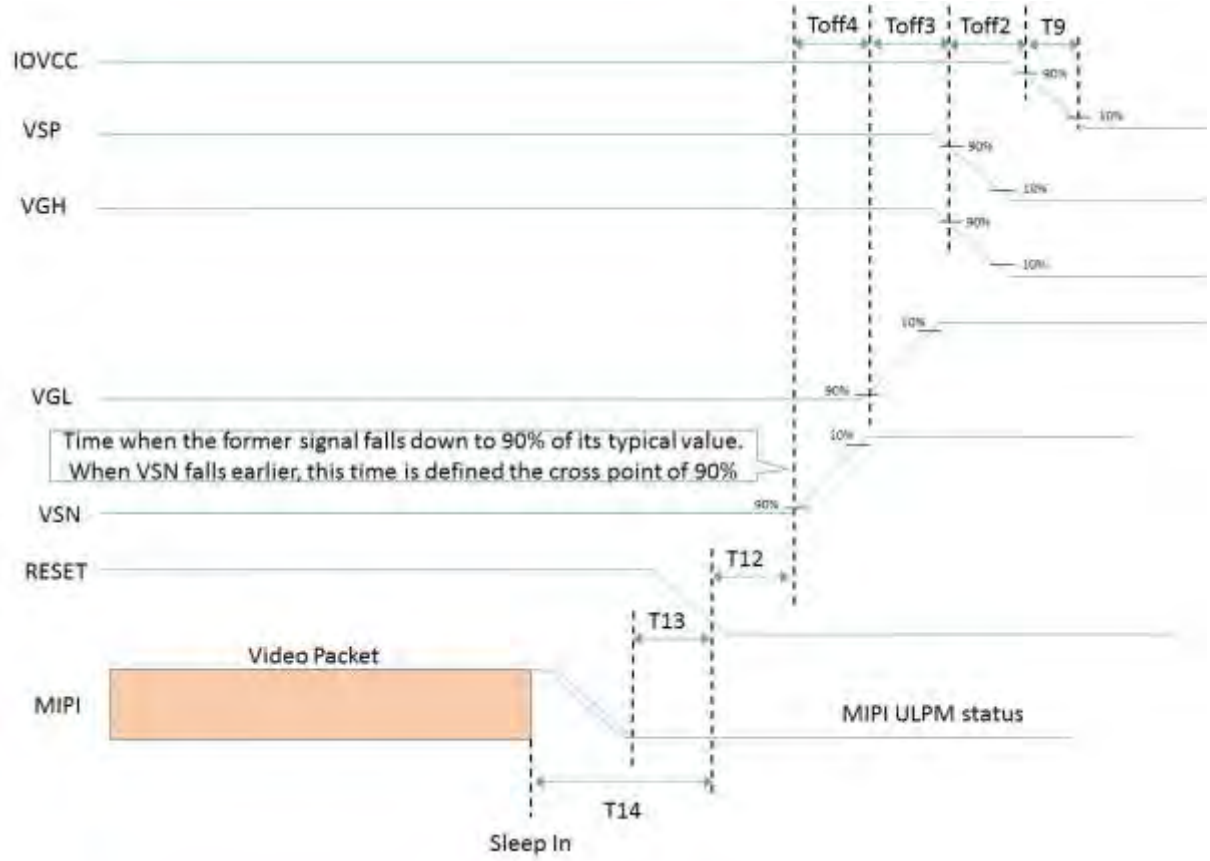


Figure 7.2.1-1: Power OFF- PCCS[1:0]= L,L mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note2: Keep VGH is equal to or larger than VSP during power off sequence.

7.2.2 Power OFF- PCCS[1:0] =H,L Mode Sequence

Application Power: IOVCC, VCI

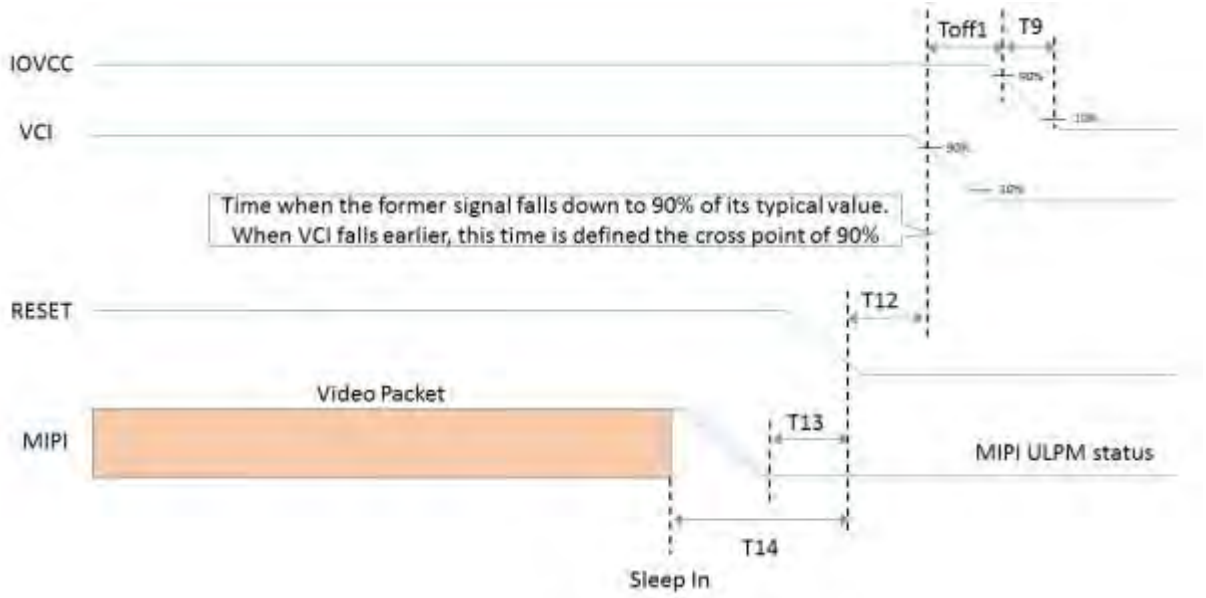


Figure 7.2.2-1: Power OFF- PCCS[1:0]= H,L mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.2.3 Power OFF- PCCS[1:0]= H,H Mode Sequence

Application Power: IOVCC, VSP, VSN

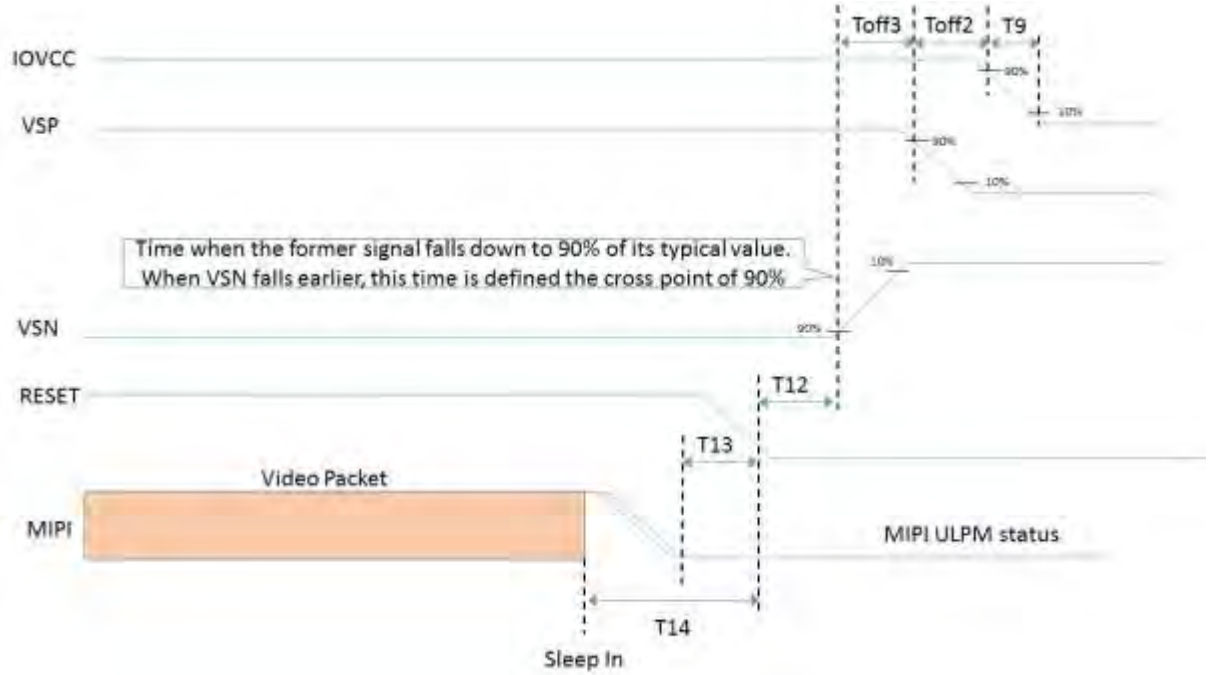


Figure 7.2.3-1: Power OFF- PCCS[1:0]= H,H mode sequence

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

8、Command

8.1、Instruction Code Table

8.1.1 Instruction Code Table → Level 1

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Hex
NOP	00h	0	W	No Parameter								-
SWRESET	01h	0	W	No Parameter								-
RDDID	04h	1	R	ID1[7:0]								00H
		2	R	ID2[7:0]								00H
		3	R	ID3[7:0]								00H
RDNUMED	05h	1	R	P[7:0]								00H
RDDST	09H	1	R	ST[31:24]								00H
		2	R	ST[23:16]								71H
		3	R	ST[15:8]								00H
		4	R	ST[7:0]								00H
RDDPM	0Ah	1	R	D[7:0]								08H
RDDMADCTR	0Bh	1	R	D[7:0]								00H
RDDCOLMOD	0Ch	1	R	D[7:0]								00H
RDDIM	0Dh	1	R	D[7:0]								00H
RDDSM	0Eh	1	R	D[7:0]								00H
RDDSDR	0Fh	1	R	D[7:0]								00H
SLPIN	10h	0	W	No Parameter								-
SLPOUT	11h	0	W	No Parameter								-
NORN	13h	0	W	No Parameter								-
INVOFF	20h	0	W	No Parameter								-
INVON	21h	0	W	No Parameter								-
ALLPOFF	22h	0	W	No Parameter								-
ALLPON	23h	0	W	No Parameter								-
GAMSET	26h	1	W	0	0	0	0	GC[3:0]				01H
DISPOFF	28h	0	W	No Parameter								-
DISPON	29h	0	W	No Parameter								-
TEOFF	34h	0	W	No Parameter								-

TEON	35h	1	W	0	0	0	0	0	0	0	M	00H
MADCTR	36h	1	W	0	0	0	ML	RGB	MH	0	0	00H
IDMOFF	38h	0	W	No Parameter								-
IDMON	39h	0	W	No Parameter								-
COLMOD	3Ah	1	W	0	VPF[2:0]			0	0	0	0	70H
STESL	44h	1	W	N[15:8]								00H
		2	W	N[7:0]								00H
RDSCL	45h	1	R	SLN[15:8]								00H
		2	R	SLN[7:0]								00H
WRDISBV	51h	1	W	DBV[7:0]								00H
RDDISBV	52h	1	R	DBV[7:0]								00H
WRCTRLD	53h	1	W	0	0	BCTL	0	DD	BL	0	0	00H
RDCTRLD	54h	1	R	0	0	BCTL	0	DD	BL	0	0	00H
WRCABC	55h	1	W	0	0	0	0	0	0	CABC [1:0]		00H
RDCABC	56h	1	R	0	0	0	0	0	0	CABC [1:0]		00H
WRCABCMB	5Eh	1	W	CMB[7:0]								00H
RDCABCMB	5Fh	1	R	CMB[7:0]								00H
RDID1	DAh	1	R	ID1[7:0]								00H
RDID2	DBh	1	R	ID2[7:0]								00H
RDID3	DCh	1	R	ID3[7:0]								00H

8.1.2 Instruction Code Table → Level 2

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial (Hex)
GOUTL	B3	1	W	0	0	GOUTL_SEL1[5:0]						03
		2	W	0	0	GOUTL_SEL2[5:0]						03
		3	W	0	0	GOUTL_SEL3[5:0]						03
		4	W	0	0	GOUTL_SEL4[5:0]						03
		5	W	0	0	GOUTL_SEL5[5:0]						03
		6	W	0	0	GOUTL_SEL6[5:0]						03
		7	W	0	0	GOUTL_SEL7[5:0]						03
		8	W	0	0	GOUTL_SEL8[5:0]						03
		9	W	0	0	GOUTL_SEL9[5:0]						03
		10	W	0	0	GOUTL_SEL10[5:0]						03
		11	W	0	0	GOUTL_SEL11[5:0]						03
		12	W	0	0	GOUTL_SEL12[5:0]						03
		13	W	0	0	GOUTL_SEL13[5:0]						03
		14	W	0	0	GOUTL_SEL14[5:0]						03
		15	W	0	0	GOUTL_SEL15[5:0]						03
		16	W	0	0	GOUTL_SEL16[5:0]						03
		17	W	0	0	GOUTL_SEL17[5:0]						03
		18	W	0	0	GOUTL_SEL18[5:0]						03
		19	W	0	0	GOUTL_SEL19[5:0]						03
		20	W	0	0	GOUTL_SEL20[5:0]						03
		21	W	0	0	GOUTL_SEL21[5:0]						03
		22	W	0	0	GOUTL_SEL22[5:0]						03
GOUTR	B4	1	W	0	0	GOUTR_SEL1[5:0]						03
		2	W	0	0	GOUTR_SEL2[5:0]						03
		3	W	0	0	GOUTR_SEL3[5:0]						03
		4	W	0	0	GOUTR_SEL4[5:0]						03

		5	W	0	0	GOUTR_SEL5[5:0]						03
		6	W	0	0	GOUTR_SEL6[5:0]						03
		7	W	0	0	GOUTR_SEL7[5:0]						03
		8	W	0	0	GOUTR_SEL8[5:0]						03
		9	W	0	0	GOUTR_SEL9[5:0]						03
		10	W	0	0	GOUTR_SEL10[5:0]						03
		11	W	0	0	GOUTR_SEL11[5:0]						03
		12	W	0	0	GOUTR_SEL12[5:0]						03
		13	W	0	0	GOUTR_SEL13[5:0]						03
		14	W	0	0	GOUTR_SEL14[5:0]						03
		15	W	0	0	GOUTR_SEL15[5:0]						03
		16	W	0	0	GOUTR_SEL16[5:0]						03
		17	W	0	0	GOUTR_SEL17[5:0]						03
		18	W	0	0	GOUTR_SEL18[5:0]						03
		19	W	0	0	GOUTR_SEL19[5:0]						03
		20	W	0	0	GOUTR_SEL20[5:0]						03
		21	W	0	0	GOUTR_SEL21[5:0]						03
		22	W	0	0	GOUTR_SEL22[5:0]						03
SETID	B5	1	RW	ID1[7:0]								00
		2	RW	ID2[7:0]								00
		3	RW	ID3[7:0]								00
		4	R	0	0	0	0	0	OTP_ID_TIMES[2:0]			00
PWRCON_VCOM	B6	1	RW	VCOM_FWS[7:0]								2F
		2	RW	VCOM_BWS[7:0]								2F
		3	R	0	0	0	0	0	OTP_VCOM_TIMES[2:0]			00
PWRCON_SEQ	B7	1	W	0	0	VSP_DC_H[5:0]						01
		2	W	0	0	VSN_DC_H[5:0]						01
		3	W	0	0	VCL_DC_H[5:0]						09
		4	W	0	0	VGH_DC_H[5:0]						11
		5	W	0	0	VGL_DC_H[5:0]						0D

		6	W	0	0	GAM_DC_H[5:0]								15
		7	W	0	0	VCOM_DC_H[5:0]								19
		8	W	0	0	0	1	1	1	0	1			1D
		9	W	0	0	1	0	0	0	0	1			21
		10	W	0	0	0	1	1	1	0	1			1D
		11	W	VCL_DC_L[3:0]				VSP_DC_L[3:0]						00
		12	W	VCOM_DC_L[3:0]				VGL_DC_L[3:0]						00
		13	W	VGH_DC_L[3:0]				VSN_DC_L[3:0]						20
		14	W	0	0	0	0	GAM_DC_L[3:0]						00
		15	W	0	0	0	0	DISCH_L[3:0]						02
PWRCON_CLK	B8	1	W	0	VGL_RT[2:0]			VGH_RT[3:0]						24
		2	W	0	0	0	0	OTP_VGH_RT[3:0]						01
		3	W	VCOM_EN_S[1:0]		DCDCM[1:0]		VGL_REG_SHT	0	VSP_PMIC[1:0]				30
		4	W	0	VGL_CLK_S[2:0]			0	VCL_CLK_S[2:0]					34
		5	W	0	PWRIC_CLK_S[2:0]			0	VGH_CLK_S[2:0]					53
PWRCON_BTA	B9	1	W	1	0	1	0	0	0	0	1			A1
		2	W	0	0	1	0	0	0	0	0			20
		3	W	1	1	1	1	1	1	1	1			FF
		4	W	GAS_EN	GAS_IO_S[2:0]			GAS_VCI_S[3:0]						C4
PWRCON_MODE	BA	1	W	VCSW2_HZ	VCSW2_S[2:0]			VCSW1_HZ	VCSW1_S[2:0]					27
		2	W	0	1	1	0	0	0	1	1			63
PWRCON_REG	BD	1	W	0	1	0	VSP_S[4:0]							4E
		2	W	VCL_S[2:0]			VSN_S[4:0]							0E
		3	W	VGMP_S[7:0]										4B
		4	W	VGMN_S[7:0]										4B
		5	W	0	0	VGH_S[5:0]								20
		6	W	0	0	VGL_S[5:0]								14
		7	W	0	0	OTP_VGH_S[5:0]								00
		8	W	0	0	VGL_REG_S[5:0]								14

		9	W	0	1	0	0	0	0	1	1	43
		10	W	0	0	0	0	0	0	1	1	03
BIST	C0	1	W	0	0	0	1	0	0	0	BIST_ON	10
		2	W	1	1	1	1	1	1	1	1	FF
		3	W	1	1	1	1	1	1	1	1	FF
TCON	C1	1	W	VBP[7:0]								0C
		2	W	VFP[7:0]								10
		3	W	VSA[7:0]								04
		4	W	HBP[7:0]								0C
		5	W	HFP[7:0]								10
		6	W	HSA[7:0]								04
TCON_2	C2	1	W	NL_FIX	0	0	NL[8]	0	0	RSO[1:0]		82
		2	W	NL[7:0]								10
TCON_3	C3	1	W	0	I2O_BLKF_S[2:0]			BLK_KP	O2I_BLKF_S[2:0]			22
		2	W	REV_EOR	B4_EOR	B3_EOR	B2_EOR	0	0	0	1	01
		3	W	0	0	0	0	0	1	0	0	04
DSTB	C4	1	W	0	0	0	0	0	0	0	DSTB	00
SRC_TIM	C6	1	W	SD1[7:0]								08
		2	W	SD2[7:0]								10
		3	W	SD3[7:0]								68
		4	W	OP_ON1[7:0]								08
		5	W	0	0	0	1	0	1	1	0	16
		6	W	OP_OFF1[7:0]								60
		7	W	0	0	1	1	0	1	1	0	36
		8	W	0	0	0	0	0	0	0	0	00
SRCCON	C7	1	W	0	0	Z_SHIFT	Z_LINE	0	INV_SEL[2:0]			05
		2	W	0	0	1	0	OPDR[3:0]				23
		3	W	0	SMEQOFF	1	0	1	0	1	1	2B
		4	W	0	1	0	0	0	0	0	1	41
		5	W	PORCH_HIZ	PORCH_GND	SDSW_DATA	SDPORCH_DATA	0	NEQSTOP	0	0	00

SET_GAMMA	C8	1	W	0	VPR18[6:0]	7C
		2	W	0	VPR17[6:0]	6D
		3	W	0	VPR16[6:0]	63
		4	W	0	VPR 15[6:0]	59
		5	W	0	VPR 14[6:0]	57
		6	W	0	VPR 13[6:0]	4A
		7	W	0	VPR 12[6:0]	51
		8	W	0	VPR 11[6:0]	3A
		9	W	0	VPR 10[6:0]	55
		10	W	0	VPR 9[6:0]	53
		11	W	0	VPR 8[6:0]	55
		12	W	0	VPR 7[6:0]	7A
		13	W	0	VPR 6[6:0]	6F
		14	W	0	VPR 5[6:0]	7F
		15	W	0	VPR 4[6:0]	75
		16	W	0	VPR 3[6:0]	72
		17	W	0	VPR 2[6:0]	62
		18	W	0	VPR 1[6:0]	2D
		19	W	0	VPR 0[6:0]	06
		20	W	0	VNR18[6:0]	7C
		21	W	0	VNR 17[6:0]	6D
		22	W	0	VNR 16[6:0]	63
		23	W	0	VNR 15[6:0]	59
		24	W	0	VNR 14[6:0]	57
		25	W	0	VNR 13[6:0]	4A
		26	W	0	VNR 12[6:0]	51
		27	W	0	VNR 11[6:0]	3A
		28	W	0	VNR 10[6:0]	55
		29	W	0	VNR 9[6:0]	53
		30	W	0	VNR 8[6:0]	55

		31	W	0	VNR 7[6:0]							7A
		32	W	0	VNR 6[6:0]							6F
		33	W	0	VNR 5[6:0]							7F
		34	W	0	VNR 4[6:0]							75
		35	W	0	VNR 3[6:0]							72
		36	W	0	VNR 2[6:0]							62
		37	W	0	VNR 1[6:0]							2D
		38	W	0	VNR 0[6:0]							06
CE_CTL	CA	1	RW	0	0	0	0	0	0	0	0	00
		2	RW	0	0	0	0	0	0	0	CE_CTL	00
		3	RW	0	0	0	0	0	0	0	0	00
OTP_AUTO_PROG	CB	1	W	0	0	0	0	OTP_PROG_BANK 3	OTP_PROG_BANK 2	OTP_PROG_BANK 1	OTP_PROG_BANK 0	03
		2	W	0	0	0	0	0	0	0	OTP_INT_VPP	00
		3	W	0	0	0	0	0	0	0	OTP_AUTO_PROG	00
ABON_CTR	D0	1	W	0	0	0	0	0	FS_BLK	1	FS_EN	07
		2	W	FS_DETECT[7:0]								10
		3	W	BATON_CNT[7:0]								00
PWM_CTR	E0	1	W	0	0	1	0	PWM_POL	0	PWM_EN	0	22
		2	W	BCFRQSEL[7:0]								03
		3	W	0	0	1	0	0	0	0	0	20
		4	W	0	0	0	0	0	0	0	0	00
		5	W	0	0	0	0	0	0	0	0	FF
DGC_CTRL	E3	1	W	0	0	0	0	0	0	DTR_EN	DGC_EN	00
DGC_R	E4	1	W	DGC_R_V255[9:2]								FF
		2	W	DGC_R_V254[9:2]								FE
		3	W	DGC_R_V252[9:2]								FC
		4	W	DGC_R_V250[9:2]								FA
		5	W	DGC_R_V248[9:2]								F8

		6	W	DGC_R_V244[9:2]	F4
		7	W	DGC_R_V240[9:2]	F0
		8	W	DGC_R_V232[9:2]	E8
		9	W	DGC_R_V224[9:2]	E0
		10	W	DGC_R_V208[9:2]	D0
		11	W	DGC_R_V192[9:2]	C0
		12	W	DGC_R_V160[9:2]	A0
		13	W	DGC_R_V128[9:2]	80
		14	W	DGC_R_V127[9:2]	7F
		15	W	DGC_R_V95[9:2]	5F
		16	W	DGC_R_V63[9:2]	3F
		17	W	DGC_R_V47[9:2]	2F
		18	W	DGC_R_V31[9:2]	1F
		19	W	DGC_R_V23[9:2]	17
		20	W	DGC_R_V15[9:2]	0F
		21	W	DGC_R_V11[9:2]	0B
		22	W	DGC_R_V7[9:2]	07
		23	W	DGC_R_V5[9:2]	05
		24	W	DGC_R_V3[9:2]	03
		25	W	DGC_R_V1[9:2]	01
		26	W	DGC_R_V0[9:2]	00
DGC_G	E5	1	W	DGC_G_V255[9:2]	FF
		2	W	DGC_G_V254[9:2]	FE
		3	W	DGC_G_V252[9:2]	FC
		4	W	DGC_G_V250[9:2]	FA
		5	W	DGC_G_V248[9:2]	F8
		6	W	DGC_G_V244[9:2]	F4
		7	W	DGC_G_V240[9:2]	F0
		8	W	DGC_G_V232[9:2]	E8
		9	W	DGC_G_V224[9:2]	E0

		10	W	DGC_G_V208[9:2]	D0
		11	W	DGC_G_V192[9:2]	C0
		12	W	DGC_G_V160[9:2]	A0
		13	W	DGC_G_V128[9:2]	80
		14	W	DGC_G_V127[9:2]	7F
		15	W	DGC_G_V95[9:2]	5F
		16	W	DGC_G_V63[9:2]	3F
		17	W	DGC_G_V47[9:2]	2F
		18	W	DGC_G_V31[9:2]	1F
		19	W	DGC_G_V23[9:2]	17
		20	W	DGC_G_V15[9:2]	0F
		21	W	DGC_G_V11[9:2]	0B
		22	W	DGC_G_V7[9:2]	07
		23	W	DGC_G_V5[9:2]	05
		24	W	DGC_G_V3[9:2]	03
		25	W	DGC_G_V1[9:2]	01
		26	W	DGC_G_V0[9:2]	00
DGC_B	E6	1	W	DGC_B_V255[9:2]	FF
		2	W	DGC_B_V254[9:2]	FE
		3	W	DGC_B_V252[9:2]	FC
		4	W	DGC_B_V250[9:2]	FA
		5	W	DGC_B_V248[9:2]	F8
		6	W	DGC_B_V244[9:2]	F4
		7	W	DGC_B_V240[9:2]	F0
		8	W	DGC_B_V232[9:2]	E8
		9	W	DGC_B_V224[9:2]	E0
		10	W	DGC_B_V208[9:2]	D0
		11	W	DGC_B_V192[9:2]	C0
		12	W	DGC_B_V160[9:2]	A0
		13	W	DGC_B_V128[9:2]	80

		14	W	DGC_B_V127[9:2]				7F
		15	W	DGC_B_V95[9:2]				5F
		16	W	DGC_B_V63[9:2]				3F
		17	W	DGC_B_V47[9:2]				2F
		18	W	DGC_B_V31[9:2]				1F
		19	W	DGC_B_V23[9:2]				17
		20	W	DGC_B_V15[9:2]				0F
		21	W	DGC_B_V11[9:2]				0B
		22	W	DGC_B_V7[9:2]				07
		23	W	DGC_B_V5[9:2]				05
		24	W	DGC_B_V3[9:2]				03
		25	W	DGC_B_V1[9:2]				01
		26	W	DGC_B_V0[9:2]				00
DGC_R_L	E7	1	W	DGC_R_V255[1:0]	DGC_R_V254[1:0]	DGC_R_V252[1:0]	DGC_R_V250[1:0]	00
		2	W	DGC_R_V248[1:0]	DGC_R_V244[1:0]	DGC_R_V240[1:0]	DGC_R_V232[1:0]	00
		3	W	DGC_R_V224[1:0]	DGC_R_V208[1:0]	DGC_R_V192[1:0]	DGC_R_V160[1:0]	00
		4	W	DGC_R_V128[1:0]	DGC_R_V127[1:0]	DGC_R_V95[1:0]	DGC_R_V63[1:0]	00
		5	W	DGC_R_V47[1:0]	DGC_R_V31[1:0]	DGC_R_V23[1:0]	DGC_R_V15[1:0]	00
		6	W	DGC_R_V11[1:0]	DGC_R_V7[1:0]	DGC_R_V5[1:0]	DGC_R_V3[1:0]	00
		7	W	DGC_R_V1[1:0]	DGC_R_V0[1:0]	0 0	0 0	00
DGC_G_L	E8	1	W	DGC_G_V255[1:0]	DGC_G_V254[1:0]	DGC_G_V252[1:0]	DGC_G_V250[1:0]	00
		2	W	DGC_G_V248[1:0]	DGC_G_V244[1:0]	DGC_G_V240[1:0]	DGC_G_V232[1:0]	00
		3	W	DGC_G_V224[1:0]	DGC_G_V208[1:0]	DGC_G_V192[1:0]	DGC_G_V160[1:0]	00
		4	W	DGC_G_V128[1:0]	DGC_G_V127[1:0]	DGC_G_V95[1:0]	DGC_G_V63[1:0]	00
		5	W	DGC_G_V47[1:0]	DGC_G_V31[1:0]	DGC_G_V23[1:0]	DGC_G_V15[1:0]	00
		6	W	DGC_G_V11[1:0]	DGC_G_V7[1:0]	DGC_G_V5[1:0]	DGC_G_V3[1:0]	00
		7	W	DGC_G_V1[1:0]	DGC_G_V0[1:0]	0 0	0 0	00
DGC_B_L	E9	1	W	DGC_B_V255[1:0]	DGC_B_V254[1:0]	DGC_B_V252[1:0]	DGC_B_V250[1:0]	00
		2	W	DGC_B_V248[1:0]	DGC_B_V244[1:0]	DGC_B_V240[1:0]	DGC_B_V232[1:0]	00
		3	W	DGC_B_V224[1:0]	DGC_B_V208[1:0]	DGC_B_V192[1:0]	DGC_B_V160[1:0]	00

		4	W	DGC_B_V128[1:0]	DGC_B_V127[1:0]	DGC_B_V95[1:0]		DGC_B_V63[1:0]		00
		5	W	DGC_B_V47[1:0]	DGC_B_V31[1:0]	DGC_B_V23[1:0]		DGC_B_V15[1:0]		00
		6	W	DGC_B_V11[1:0]	DGC_B_V7[1:0]	DGC_B_V5[1:0]		DGC_B_V3[1:0]		00
		7	W	DGC_B_V1[1:0]	DGC_B_V0[1:0]	0	0	0	0	00
PASSWORD1	F0	1	W	PASSWORD1[7:0]						A5
		2	W	PASSWORD1[7:0]						A5
PASSWRD2	F1	1	W	PASSWORD1[7:0]						5A
		2	W	PASSWORD1[7:0]						5A

8.2、Level 1 Command Description

8.2.1 NOP: NOP (00h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	W	0	0	0	0	0	0	0	0	00h
Parameter	-	No Parameter								

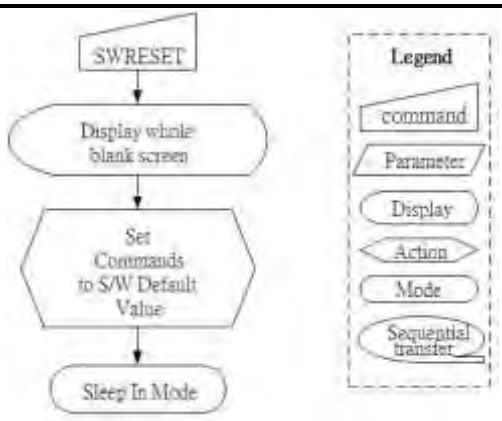
NOTE: "-"Don't care

Description	This command is empty command. It does not have effect on the display module.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A
Flow Chart	-

8.2.2 SWRESET: Software Reset (01h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	W	0	0	0	0	0	0	0	1	01h
Parameter		No Parameter								

NOTE: "-"Don't care

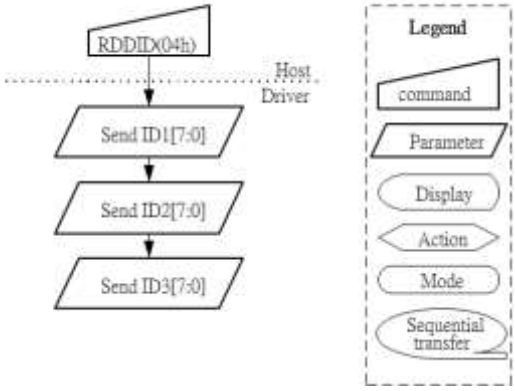
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to GND (display off).
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: N/A Status: S/W Reset — Default Value: N/A Status: H/W Reset — Default Value: N/A
Flow Chart	

8.2.3 RDDID: Read Display ID (04h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDID	R	0	0	0	0	0	1	0	0	04h
Parameter	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
Parameter	2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Parameter	3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-"Don't care

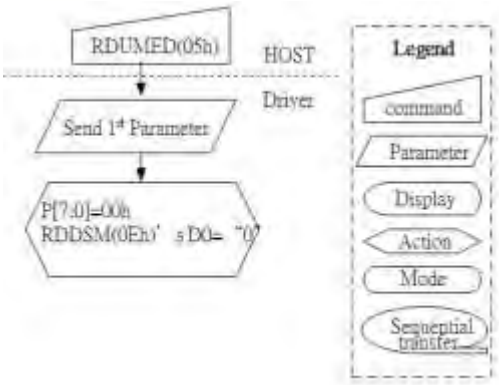
<table>
<tr><td>Description</td><td>This read byte returns 24-bit display identification information.
The 1st (ID17 to ID10): LCD module's manufacturer ID.
The 2nd parameter (ID27 to ID20): LCD module/driver version ID.
The 3rd parameter (ID37 to UD30): LCD module/driver ID.
NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1, 2 and 3 of the command 04h, respectively.</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>If ID1/ID2/ID3 OTP are not yet programmed:
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>ID1</th><th>ID2</th><th>ID3</th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>80h</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>80h</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>80h</td><td>00h</td></tr>
</table>
If ID1/ID2/ID3 OTP were programmed:
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>ID1</th><th>ID2</th><th>ID3</th></tr>
<tr><td>Power On Sequence</td><td>(OTP value)</td><td>(OTP value)</td><td>(OTP value)</td></tr>
<tr><td>S/W Reset</td><td>(OTP value)</td><td>(OTP value)</td><td>(OTP value)</td></tr>
<tr><td>H/W Reset</td><td>(OTP value)</td><td>(OTP value)</td><td>(OTP value)</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

8.2.4 RDNUMED: Read Number of Errors on DSI (05h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDNUMED	R	0	0	0	0	0	1	0	1	05h
Parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00h

NOTE: "-"Don't care

Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to "1" if there is overflow with P[6..0] bits. P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed). See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / 00h S/W Reset / No Changed H/W Reset / 00h
Flow Chart	

8.2.5 RDDST: Read Display Status (09h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	R	0	0	0	0	1	0	0	1	09h
Parameter	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	00h
Parameter	2	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	71h
Parameter	3	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	00h
Parameter	4	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	40h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Not Used	"0"
ST29	Not Used	"0"
ST28	Not Used	"0"
ST27	Vertical refresh Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Horizontal refresh Order (MH)	"1"=Decrement, "0"=Increment
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22-20	Interface Color Pixel Format Definition	"110" = 18-bit / pixel, "111" = 24-bit / pixel
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Not Used	"0"
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display
ST15	Not Used	"0"
ST14	Not Used	"0"
ST13	Inversion Status	"0" = Off
ST12	All Pixels On	"1" = All Pixels On, "0" = All Pixels Off
ST11	All Pixels Off	"0"
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8-6	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" = GC4 "101" to "111" = Not defined
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

Restriction

-

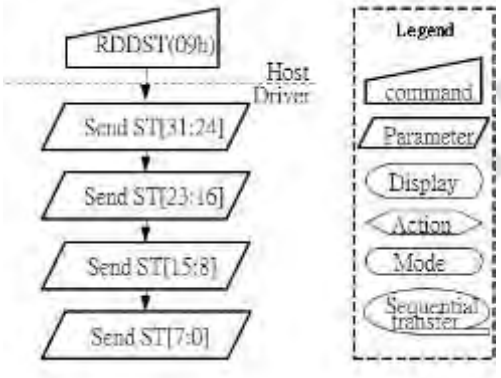
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h,71h,00h,00h
S/W Reset	00h,71h,00h,00h
H/W Reset	00h,71h,00h,00h

Flow Chart



8.2.6 RDDPM: Read Display Power Mode (0Ah)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDPM	R	0	0	0	0	1	0	1	0	0Ah
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	08h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1" = Booster on, "0" = Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
D5	Not Used	"0"
D4	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display On, "0" = Normal Display Off
D2	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

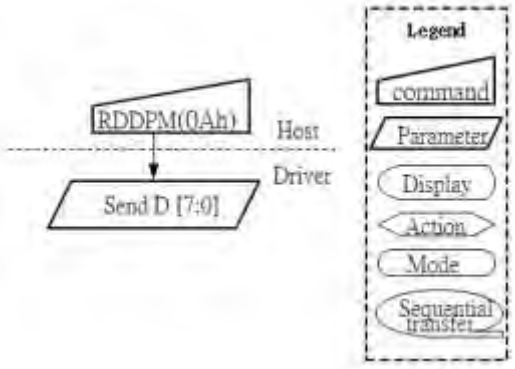
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



8.2.7 RDDMADCTR: Read Display MADCTR (0Bh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDMADCTR	R	0	0	0	0	1	0	1	1	0Bh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Not Used	"0"
D4	Vertical fresh Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Horizontal fresh Order (MH)	"1"=Decrement, "0"=Increment
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

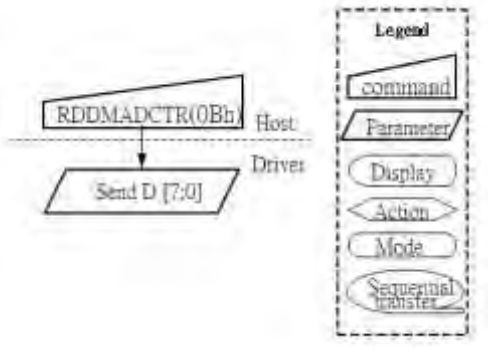
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.8 RDDCOLMOD: Read Display Pixel Format (0Ch)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDCOLMOD	R	0	0	0	0	1	1	0	0	0Ch
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	70h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6 – 4	Control Interface Color Format	"110"=18 bit/pixel "111"=24 bit/pixel The others are not defined
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

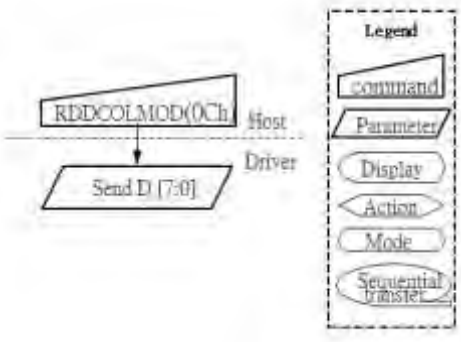
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



8.2.9 RDDIM: Read Display Image Mode (0Dh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDIM	R	0	0	0	0	1	1	0	1	0Dh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Inversion On/Off	"0" = Inversion is Off
D4	All Pixels On	"1" = All Pixels On
D3	All Pixels Off	"1" = All Pixels Off
D2 -0	Gamma Curve Selection	"000" = GC0 ,"001" = GC1,"010" = GC2,"011" = GC3 ,"100" = GC4, "101" to "111" = Not defined

Restriction

-

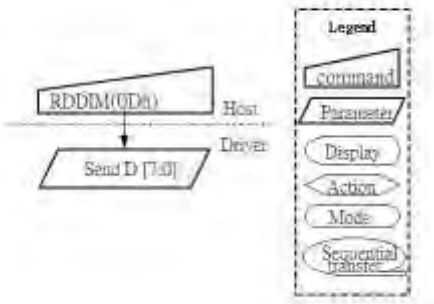
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.10 RDDIM: Read Display Signal Mode (0Eh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSM	R	0	0	0	0	1	1	1	0	0Eh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing effect line mode	"0" = mode1,"1" = mode2
D5	Not Used	"0"
D4	Not Used	"0"
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Error on DSI	"1" = Error, "0" = No Error

Restriction

-

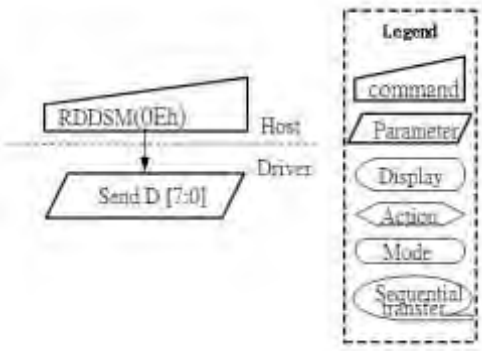
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.11 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSDR	R	0	0	0	0	1	1	1	1	0Fh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

NOTE: "-"Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section 6.7
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

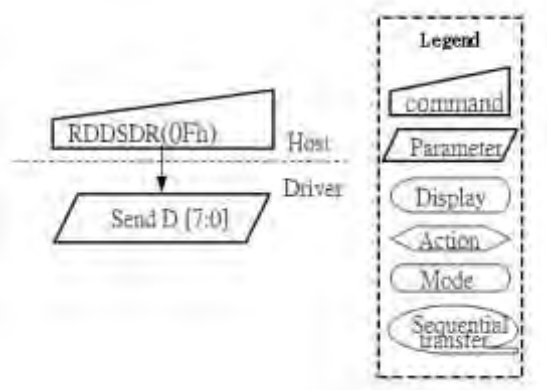
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

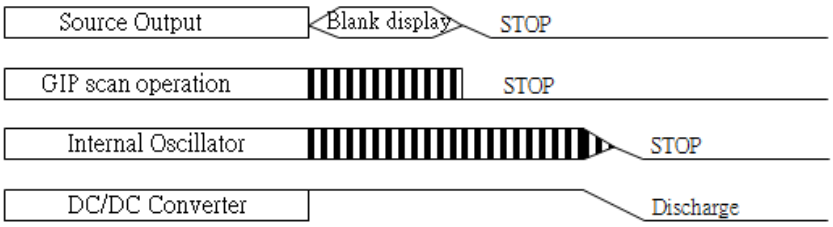
Flow Chart

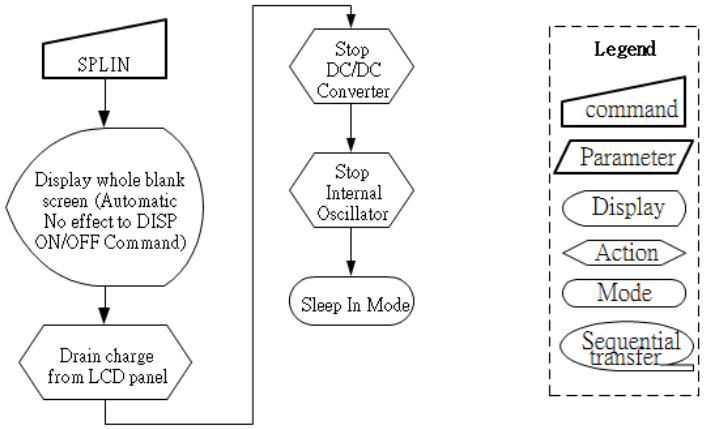


8.2.12 SLPIN: Sleep In (10h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	W	0	0	0	1	0	0	0	0	10h
Parameter	-	No Parameter								

NOTE: "-"Don't care

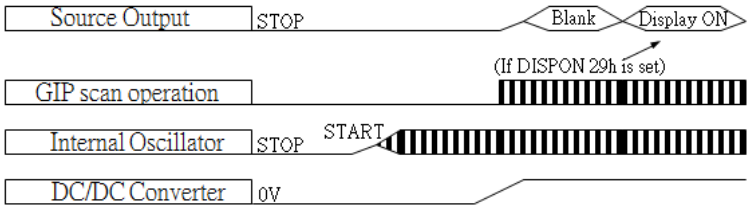
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. 
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes
Default	Status / Default Value: Power On Sequence — Sleep In mode S/W Reset — Sleep In mode H/W Reset — Sleep In mode

Flow Chart	It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit 31. 

8.2.13 SLPOUT: Sleep Out (11h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	W	0	0	0	1	0	0	0	1	11h
Parameter	-	No Parameter								

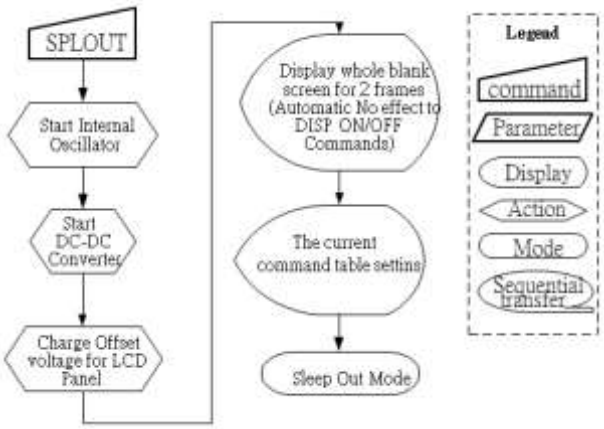
NOTE: "-"Don't care

Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. 
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. ICNL9706 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the ICNL9706 is already Sleep Out –mode. ICNL9706 is doing self-diagnostic functions during this 5msec. See also section 6.7. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit 31. 

8.2.14 NORON: Normal Display Mode ON (13h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	W	0	0	0	1	0	0	1	1	13h
Parameter	-	No Parameter								

NOTE: "-"Don't care

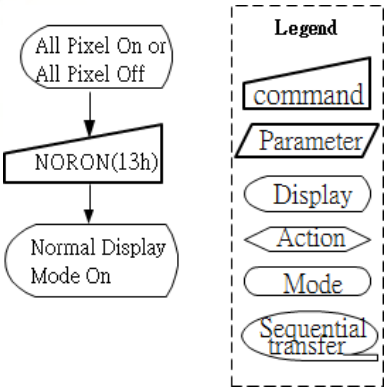
Description	This command returns the display to normal mode. Normal display mode on. Exit from NORON by the All Pixels On or All Pixels Off command. There is no abnormal visual effect during mode change.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart



8.2.15 INVOFF: Display Inversion OFF (20h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	W	0	0	1	0	0	0	0	0	20h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)

Restriction

This command has no effect when module is already inversion off mode.

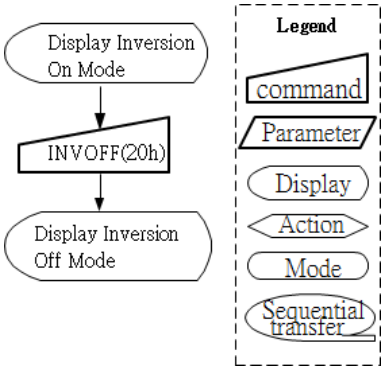
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



8.2.16 INVON: Display Inversion ON (21h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVON	W	0	0	1	0	0	0	0	1	21h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description

This command is used to enter display inversion mode.

This command makes no change of contents of frame memory.

This command does not change any other status.

To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)

Restriction

This command has no effect when module is already inversion On mode.

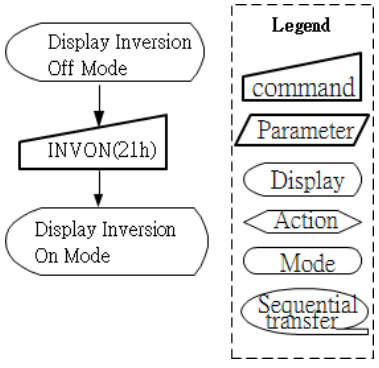
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

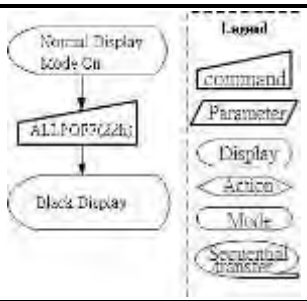
Flow Chart



8.2.17 ALLPOFF: All Pixel OFF (22h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ALLPOFF	W	0	0	1	0	0	0	1	0	22h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example)  "All Pixels On", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.
Restriction	This command has no effect when module is already in All Pixel Off mode.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: All Pixels Off S/W Reset: All Pixels Off H/W Reset: All Pixels Off
Flow Chart	

8.2.18 ALLPON: All Pixel ON (23h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ALLPON	W	0	0	1	0	0	0	1	1	23h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description

This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)

"All Pixels OFF", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.

Restriction

This command has no effect when module is already in All Pixel On mode.

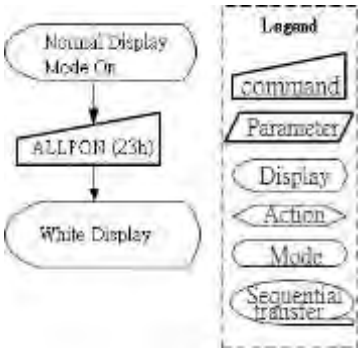
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All Pixels Off
S/W Reset	All Pixels Off
H/W Reset	All Pixels Off

Flow Chart



8.2.19 GAMSET: Gamma Set (26h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GAMSET	W	0	0	1	0	0	1	1	0	26h
Parameter	1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

NOTE: "-"Don't care

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (Gamma=2.2 Set)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.

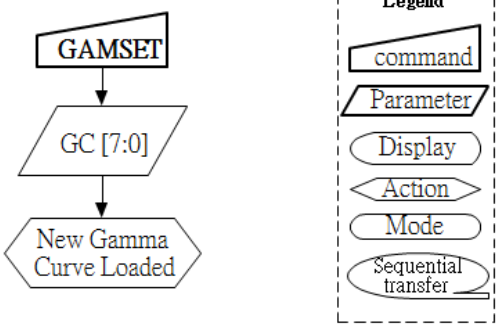
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.20 DISPOFF: Display OFF (28h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	W	0	0	1	0	1	0	0	0	28h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) 
Restriction	This command has no effect when module is already in Display Off mode.

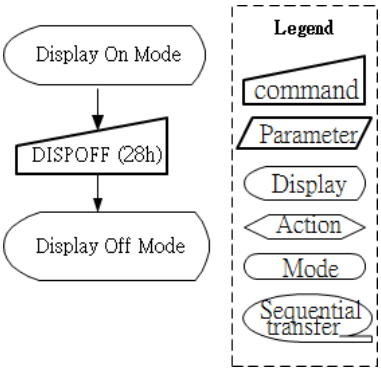
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



8.2.21 DISPON: Display ON (29h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	W	0	0	1	0	1	0	0	1	29h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description

This command is used to recover from DISPLAY OFF mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)

Restriction

This command has no effect when module is already in Display On mode.

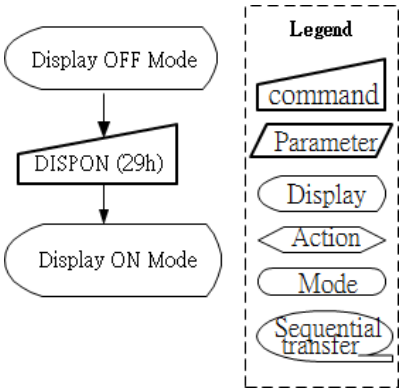
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



8.2.22 TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEOFF	W	0	0	1	1	0	1	0	0	34h
Parameter	-	No Parameter								

NOTE: "-"Don't care

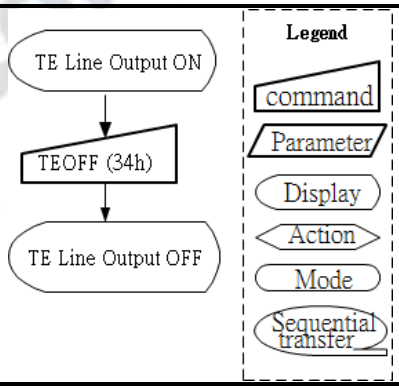
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



8.2.23 TEON: Tearing Effect Line ON (35h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEON	W	0	0	1	1	0	1	0	1	35h
Parameter	1	-	-	-	-	-	-	-	M	00h

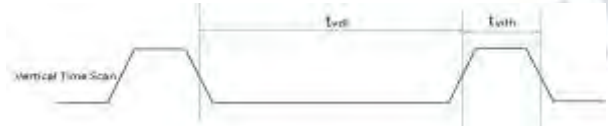
NOTE: "-"Don't care

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

When M = "0": The Tearing Effect Output line consists of V-Blanking information only.



When M = "1": The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

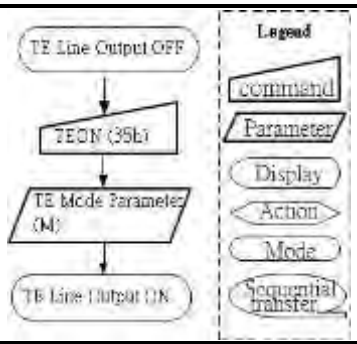
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



8.2.24 MADCTL: Memory Data Access Control (36h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTL	W	0	0	1	1	0	1	1	0	36h
Parameter	1	-	-	-	ML	RGB	MH	-	-	00h

NOTE: "-"Don't care

Description

This command defines display direction of image.

This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
ML	Vertical refresh ORDER	LCD Vertical refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal refresh ORDER	LCD Horizontal refresh direction control

Restriction

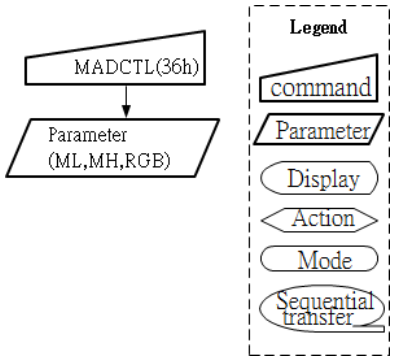
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

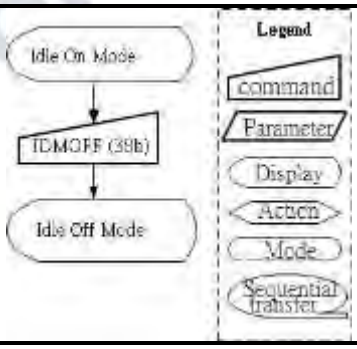
Flow Chart



8.2.25 IDMOFF: Idle mode OFF (38h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMOFF	W	0	0	1	1	1	0	0	0	38h
Parameter	-	No Parameter								

NOTE: "-"Don't care

Description	This command is used to recover from Idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.
Restriction	This command has no effect when module is already in Idle Off mode.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Idle mode Off Status: S/W Reset — Default Value: Idle mode Off Status: H/W Reset — Default Value: Idle mode Off
Flow Chart	

8.2.26 IDMON: Idle mode ON (39h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMON	W	0	0	1	1	1	0	0	1	39h
Parameter	-	No Parameter								

NOTE: "-"Don't care

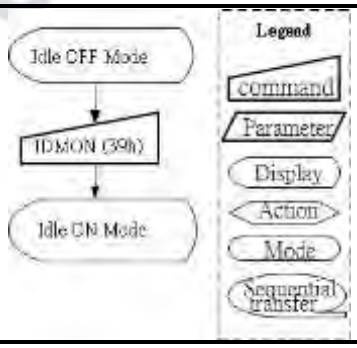
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The display color is determined by MSB of R, G, and B.
Restriction	This command has no effect when module is already in Idle On mode
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode Off
S/W Reset	Idle mode Off
H/W Reset	Idle mode Off

Flow Chart



8.2.27 COLMOD: Interface Pixel Format (3Ah)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	W	0	0	1	1	1	0	1	0	3Ah
Parameter	1	-	VIPF[2:0]			-	-	-	-	70h

NOTE: "-"Don't care

Description

This command is used to define the format of RGB picture data.

The formats are shown in the table:

Bit	NAME	DESCRIPTION
VIPF[2:0]	Pixel Format for RGB.	"110" = 18-bit/pixel "111" = 24-bit/pixel The others = not defined

Restriction

There is no visible effect until the Frame Memory is written to.

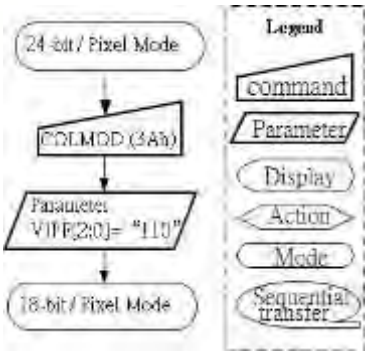
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



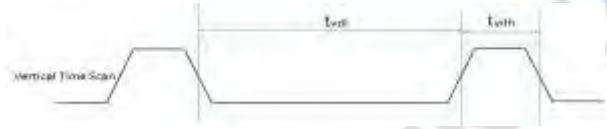
8.2.28 STESL: Set Tearing Effect Scan Line (44h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
STESL	W	0	1	0	0	0	1	0	0	44h
Parameter	1	N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter	1	N7	N6	N5	N4	N3	N2	N1	N0	00h

NOTE: "-"Don't care

Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.



*Note that STESL with N[15:0]="000h" is equivalent to TEON with M="0"*The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.

This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.

Restriction

Parameter range 0 _ N[15:0] _ 1280+Porch Line

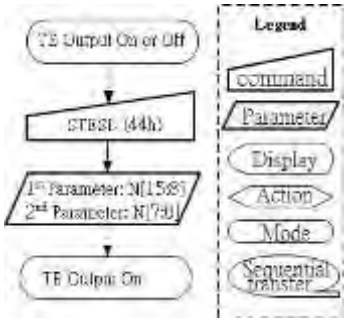
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



8.2.29 GSL: Get Scan Line (45h)

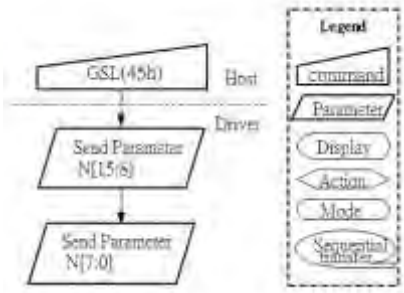
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GSL	R	0	1	0	0	0	1	0	1	45h
Parameter	1	N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter	1	N7	N6	N5	N4	N3	N2	N1	N0	00h

NOTE: "-"Don't care

Description	This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as Vdisplay + Vporch. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.
Restriction	-
Register Availability	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h



8.2.30 WRDISBV: Write Display Brightness (51h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRDISBV	W	0	1	0	1	0	0	0	1	51h
Parameter	1	BV[7]	BV[6]	BV[5]	BV[4]	BV[3]	BV[2]	BV[1]	BV[0]	00h

NOTE: "-"Don't care

Description

This command is used to adjust brightness value.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

BV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0 %
01h	2/256	0.78 %
……	……	……
FEh	255/256	99.6%
FFh	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

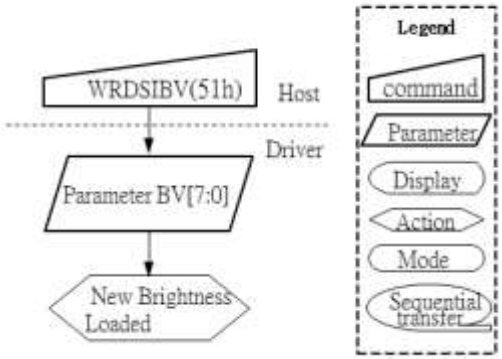
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.31 RDDISBV: Read Display Brightness (52h)

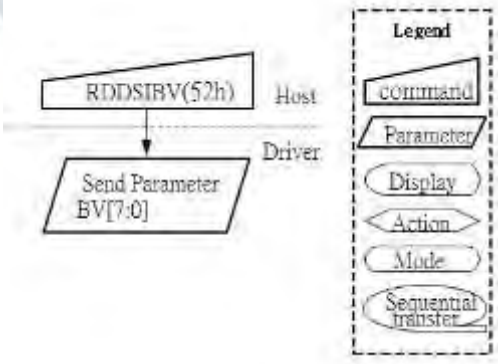
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDISBV	R	0	1	0	1	0	0	1	0	52h
Parameter	1	BV[7]	BV[6]	BV[5]	BV[4]	BV[3]	BV[2]	BV[1]	BV[0]	00h

NOTE: "-"Don't care

Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
Restriction	-
Register Availability	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

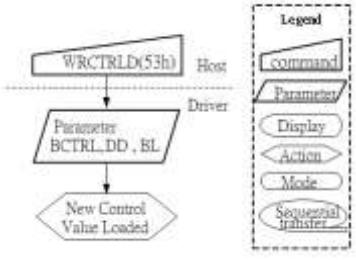
Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h



8.2.32 WRCTRLD: Write CTRL Display (53h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCTRLD	W	0	1	0	1	0	0	1	1	53h
Parameter	1	-	-	BCTRL	-	DD	BL	-	-	00h

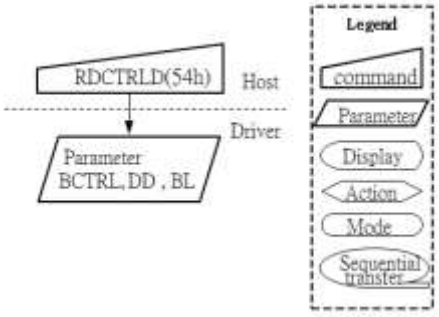
NOTE: "-"Don't care

Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit). BCTRL =0, BV[7:0] value disable. BCTRL =1, BV[7:0] value enable. DD: Display Dimming Control On/Off. DD= 0, Display dimming is off. DD=1, Display dimming is on. BL: Backlight Control On/Off without Dimming Effect When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected. BL =0, Off. BL =1, On The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0. *Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.*
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / 00h S/W Reset / 00h H/W Reset / 00h
Flow Chart	

8.2.33 RDCTRLD: Read CTRL Display (54h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCTRLD	R	0	1	0	1	0	1	0	0	54h
Parameter	1	-	-	BCTRL	-	DD	BL	-	-	00h

NOTE: "-"Don't care

Description	This command returns the display brightness. BCTRL: Brightness Control Block On/Off The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit). BCTRL =0, BV[7:0] value disable. BCTRL =1, BV[7:0] value enable. DD: Display Dimming Control On/Off. DD= 0, Display dimming is off. DD=1, Display dimming is on. BL: Backlight Control On/Off without Dimming Effect When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected. BL =0, Off. BL =1, On The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0.
Restriction	-
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h
Flow Chart	

8.2.34 WRCABC: Write Content Adaptive Brightness Control (55h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCABC	W	0	1	0	1	0	1	0	1	55h
Parameter	1	-	-	-	CABC_OFF	-	-	CBAC_CON[1:0]		10h

NOTE: "-"Don't care

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_CON[1]	CABC_CON[0]	Function
0	0	Off
0	1	User Interface Image
1	0	Still picture
1	1	Moving Image

CABC_OFF : 1: Disable CABC Function

0: Enable CABC Function

Restriction

-

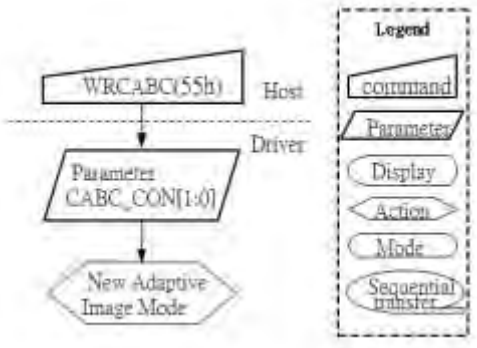
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

Flow Chart



8.2.35 RDCABC: Read Content Adaptive Brightness Control (56h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCABC	R	0	1	0	1	0	1	1	0	56h
Parameter	1	-	-	-	CABC_OFF	-	-	CBAC_CON[1:0]		00h

NOTE: "-"Don't care

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_CON[1]	CABC_CON[0]	Function
0	0	Off
0	1	User Interface Image
1	0	Still picture
1	1	Moving Image

CABC_OFF : 1: Disable CABC Function

0: Enable CABC Function

Restriction

-

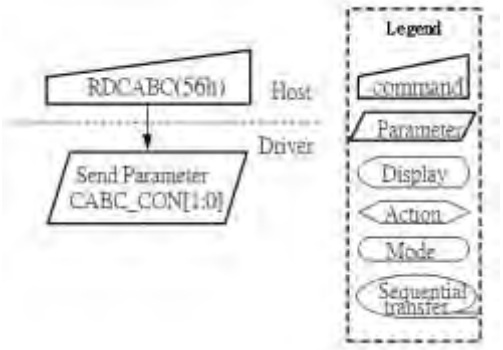
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

Flow Chart



8.2.36 WRCABCMB: Write CABC minimum brightness (5Eh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCABCMB	W	0	1	0	1	1	1	1	0	5Eh
Parameter	1	MB[7]	MB[6]	MB[5]	MB[4]	MB[3]	MB[2]	MB[1]	MB[0]	00h

NOTE: "-"Don't care

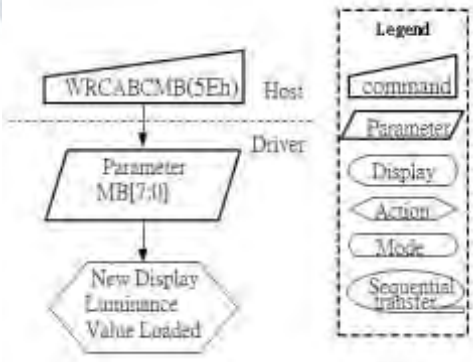
Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.37 RDCABCMB: Read CABC minimum brightness (5Fh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCABCMB	R	0	1	0	1	1	1	1	1	5Fh
Parameter	1	MB[7]	MB[6]	MB[5]	MB[4]	MB[3]	MB[2]	MB[1]	MB[0]	00h

NOTE: "-"Don't care

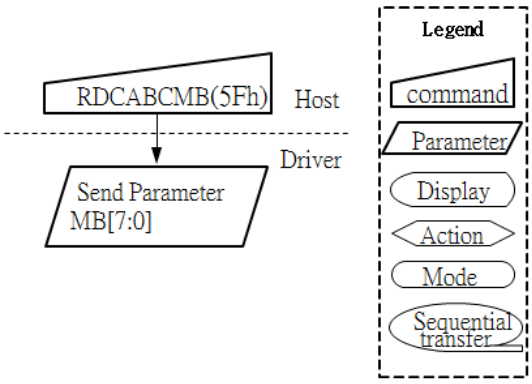
Description	This command return the minimum brightness value of CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. MB[7:0] is the minimum brightness for CABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.38 RDID1: Read ID1 Value (DAh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	R	1	1	0	1	1	0	1	0	DAh
Parameter	1	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	00h

NOTE: "-"Don't care

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-

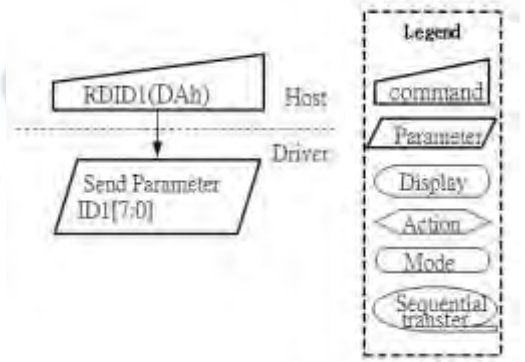
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.39 RDID2: Read ID2 Value (DBh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID2	R	1	1	0	1	1	0	1	1	DBh
Parameter	1	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	00h

NOTE: "-"Don't care

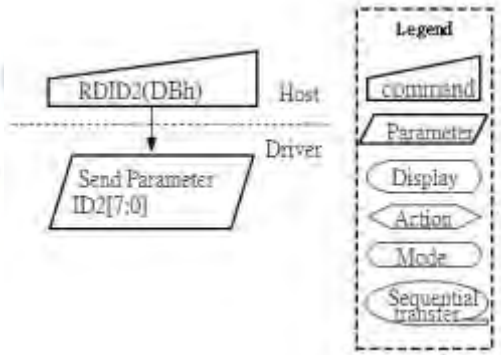
Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

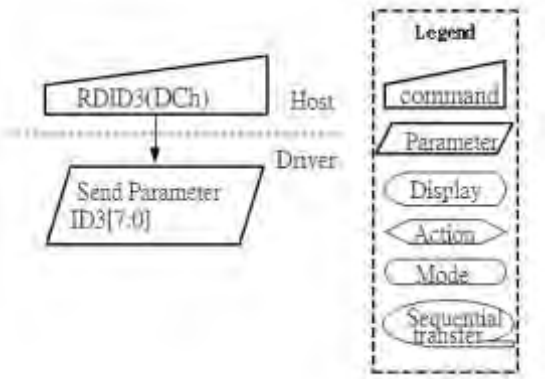
Flow Chart



8.2.40 RDID3: Read ID3 Value (DCh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID3	R	1	1	0	1	1	1	0	0	DCh
Parameter	1	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	00h

NOTE: "-"Don't care

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h
Flow Chart	

8.3、Level 2 Command Description

8.3.1 CGOUTL Control

This command is used to set the assignment of ASG output signals.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GOUTL	W	1	0	1	1	0	0	1	1	B3h
Parameter	1	0	0	GOUTL_SEL1[5:0]						03h
Parameter	2	0	0	GOUTL_SEL2[5:0]						03h
Parameter	3	0	0	GOUTL_SEL3[5:0]						03h
Parameter	4	0	0	GOUTL_SEL4[5:0]						03h
Parameter	5	0	0	GOUTL_SEL5[5:0]						03h
Parameter	6	0	0	GOUTL_SEL6[5:0]						03h
Parameter	7	0	0	GOUTL_SEL7[5:0]						03h
Parameter	8	0	0	GOUTL_SEL8[5:0]						03h
Parameter	9	0	0	GOUTL_SEL9[5:0]						03h
Parameter	10	0	0	GOUTL_SEL10[5:0]						03h
Parameter	11	0	0	GOUTL_SEL11[5:0]						03h
Parameter	12	0	0	GOUTL_SEL12[5:0]						03h
Parameter	13	0	0	GOUTL_SEL13[5:0]						03h
Parameter	14	0	0	GOUTL_SEL14[5:0]						03h
Parameter	15	0	0	GOUTL_SEL15[5:0]						03h
Parameter	16	0	0	GOUTL_SEL16[5:0]						03h
Parameter	17	0	0	GOUTL_SEL17[5:0]						03h
Parameter	18	0	0	GOUTL_SEL18[5:0]						03h
Parameter	19	0	0	GOUTL_SEL19[5:0]						03h
Parameter	20	0	0	GOUTL_SEL20[5:0]						03h
Parameter	21	0	0	GOUTL_SEL21[5:0]						03h
Parameter	22	0	0	GOUTL_SEL22[5:0]						03h

Note : Refer 8.3.2 CGOUTR Control

8.3.2 CGOUTR Control

This command is used to set the assignment of ASG output signals.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GOUTR	W	1	0	1	1	0	1	0	0	B4h
Parameter	1	0	0	GOUTR_SEL1[5:0]						03h
Parameter	2	0	0	GOUTR_SEL2[5:0]						03h
Parameter	3	0	0	GOUTR_SEL3[5:0]						03h
Parameter	4	0	0	GOUTR_SEL4[5:0]						03h
Parameter	5	0	0	GOUTR_SEL5[5:0]						03h
Parameter	6	0	0	GOUTR_SEL6[5:0]						03h
Parameter	7	0	0	GOUTR_SEL7[5:0]						03h
Parameter	8	0	0	GOUTR_SEL8[5:0]						03h
Parameter	9	0	0	GOUTR_SEL9[5:0]						03h
Parameter	10	0	0	GOUTR_SEL10[5:0]						03h
Parameter	11	0	0	GOUTR_SEL11[5:0]						03h
Parameter	12	0	0	GOUTR_SEL12[5:0]						03h
Parameter	13	0	0	GOUTR_SEL13[5:0]						03h
Parameter	14	0	0	GOUTR_SEL14[5:0]						03h
Parameter	15	0	0	GOUTR_SEL15[5:0]						03h
Parameter	16	0	0	GOUTR_SEL16[5:0]						03h
Parameter	17	0	0	GOUTR_SEL17[5:0]						03h
Parameter	18	0	0	GOUTR_SEL18[5:0]						03h
Parameter	19	0	0	GOUTR_SEL19[5:0]						03h
Parameter	20	0	0	GOUTR_SEL20[5:0]						03h
Parameter	21	0	0	GOUTR_SEL21[5:0]						03h
Parameter	22	0	0	GOUTR_SEL22[5:0]						03h

8.3.2.1: CGOUTL(n)[5:0], CGOUTR(n)[5:0]

These registers are used to set the mapping of the ASG signals.

CGOUTL(n)[5:0], CGOUTR(n)[5:0]	Function	CGOUTL(n)[5:0], CGOUTR(n)[5:0]	Function
00h	VGL	13h	GCK8
01h	VGH	14h	GCK9
02h	HZ	15h	GCK10
03h	GND	16h	GCK11
04h	GSP1	17h	GCK12
05h	GSP2	18h	GCK13
06h	GSP3	19h	GCK14
07h	GSP4	1Ah	GCK15
08h	GSP5	1Bh	GCK16
09h	GSP6	1Ch	DIR
0Ah	GSP7	1Dh	DIRB
0Bh	GSP8	1Eh	ECLK_AC
0Ch	GCK1	1Fh	ECLK_ACB
0Dh	GCK2	20h	ECLK_AC2
0Eh	GCK3	21h	ECLK_AC2B
0Fh	GCK4	22h	GCH
10h	GCK5	23h	GCL
11h	GCK6	24h	XDON
12h	GCK7	25h	XDONB

Hardware RESET	Default
CGOUTL(n)[5:0], CGOUTR(n)[5:0]	03h

8.3.3 SETID

This command is used to set ID1, ID2, ID3

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SETID	RW	1	0	1	1	0	1	0	1	B5h
Parameter	1	ID1[7:0]								00h
Parameter	2	ID2[7:0]								00h
Parameter	3	ID3[7:0]								00h
Parameter	4	0	0	0	0	0	OTP_TIMES[2:0]			00h

8.3.3.1: ID1[7:0], ID2[7:0], ID3[7:0]

These registers are used to write otp ID1, ID2, ID3.

Hardware RESET	Default
ID1[7:0], ID2[7:0], ID3[7:0]	00H

8.3.3.2: OTP_TIMES [2:0]

These registers are used to show the remaining program times status.

Hardware RESET	Default
OTP_TIMES[2:0]	00H

8.3.4 PWRCON_VCOM

This command is used to set VCOM voltage.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_VCOM	RW	1	0	1	1	0	1	1	0	B6h
Parameter	1	VCOM_FW[7:0]								2Fh
Parameter	2	VCOM_BW[7:0]								2Fh
Parameter	3	0	0	0	0	0	OTP_VCOM_TIMES[2:0]			00h

8.3.4.1: VCOM_FW[7:0]

These registers are used to set forward scan VCOM voltage. Register Step 15mV.

8.3.4.2: VCOM_BW[7:0]

These registers are used to set backward scan VCOM voltage. Register Step 15mV.

8.3.4.3: OTP_VCOM_TIMES[2:0]

These registers are used to set show the VCOM program times status.

VCOM_FW[7:0], VCOM_BW[7:0]	VCOM (V)
00h	-0.3V
01h	-0.315V
02h	-0.33V
……	……
2Eh	-0.99V
2Fh	-1.005V
……	……
7Eh	-2.19V
7Fh	-2.205V
80h	VCL
81h	Disable

Hardware RESET	Default
VCOM_FW[7:0], VCOM_BW[7:0]	2FH
OTP_VCOM_TIMES[2:0]	00H

8.3.5 PWRCON_SEQ

This command is used to set power sequence.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_SEQ	W	1	0	1	1	0	1	1	1	B7h
Parameter	1	0	0	VSP_DC_H[5:0]						01h
Parameter	2	0	0	VSN_DC_H[5:0]						01h
Parameter	3	0	0	VCL_DC_H[5:0]						09h
Parameter	4	0	0	VGH_DC_H[5:0]						11h
Parameter	5	0	0	VGL_DC_H[5:0]						0Dh
Parameter	6	0	0	GAM_DC_H[5:0]						15h
Parameter	7	0	0	VCOM_DC_H[5:0]						19h
Parameter	8	0	0	0	1	1	1	0	1	1Dh
Parameter	9	0	0	1	0	0	0	0	1	21h
Parameter	10	0	0	0	1	1	1	0	1	1Dh
Parameter	11	VCL_DC_L[3:0]				VSP_DC_L[3:0]				00h
Parameter	12	VCOM_DC_L[3:0]				VGL_DC_L[3:0]				00h
Parameter	13	VGH_DC_L[3:0]				VSN_DC_L[3:0]				20h
Parameter	14	0	0	0	0	GAM_DC_L[3:0]				00h
Parameter	15	0	0	0	0	DISCH_DC_L[3:0]				02h

8.3.5.1: VSP_DC_H[5:0], VSN_DC_H[5:0], VCL_DC_H[5:0], VGH_DC_H[5:0], VGL_DC_H[5:0], GAM_DC_H[5:0], VCOM_DC_H[5:0]

VSP_DC_H[5:0]: These registers are used to set VSP sequence. Register step 2mS
VSN_DC_H[5:0]: These registers are used to set VSN sequence. Register step 2mS
VCL_DC_H[5:0]: These registers are used to set VCL sequence. Register step 2mS
VGH_DC_H[5:0]: These registers are used to set VGH sequence. Register step 2mS
VGL_DC_H[5:0]: These registers are used to set VGL sequence. Register step 2mS
VGAM_DC_H[5:0]: These registers are used to set VGAM sequence. Register step 2mS
VCOM_DC_H[5:0]: These registers are used to set VCOM sequence. Register step 2mS

VSP_DC_H[5:0], VSN_DC_H[5:0], VCL_DC_H[5:0], VGH_DC_H[5:0], VGL_DC_H[5:0], GAM_DC_H[5:0], VCOM_DC_H[5:0]	Time (mS)
00h	0mS
01h	2mS
02h	4mS
……	……
20h	64mS
21h	66mS
22h	68mS
……	……
3Dh	122mS
3Eh	124mS
3Fh	126mS

8.3.5.2: VSP_DC_L[3:0], VSN_DC_L[3:0], VCL_DC_L[3:0], VGH_DC_L[3:0], VGL_DC_L[3:0], GAM_DC_L[3:0], VCOM_DC_L[3:0], DISCH_L[3:0]

VSP_DC_L[3:0]: These registers are used to set VSP sequence. Register step 2mS
VSN_DC_L[3:0]: These registers are used to set VSN sequence. Register step 2mS
VCL_DC_L[3:0]: These registers are used to set VCL sequence. Register step 2mS
VGH_DC_L[3:0]: These registers are used to set VGH sequence. Register step 2mS
VGL_DC_L[3:0]: These registers are used to set VGL sequence. Register step 2mS
VGAM_DC_L[3:0]: These registers are used to set VGAM sequence. Register step 2mS
VCOM_DC_L[3:0]: These registers are used to set VCOM sequence. Register step 2mS
DISCH_L[3:0]: These registers are used to set discharge circuit sequence. Register step 2mS

VSP_DC_L[3:0], VSN_DC_L[3:0], VCL_DC_L[3:0], VGH_DC_L[3:0], VGL_DC_L[3:0], GAM_DC_L[3:0], VCOM_DC_L[3:0], DISCH_L[3:0]	Time (mS)
00h	0mS
01h	2mS
02h	4mS
……	……
20h	64mS
21h	66mS
22h	68mS
……	……
3Dh	122mS
3Eh	124mS
3Fh	126mS

Hardware RESET	Default
VSP_DC_H[5:0]	01H
VSN_DC_H[5:0]	01H
VCL_DC_H[5:0]	09H
VGH_DC_H[5:0]	11H
VGL_DC_H[5:0]	0DH
VGAM_DC_H[5:0]	15H
VCOM_DC_H[5:0]	19H
VSP_DC_L[3:0]	0H
VSN_DC_L[3:0]	0H
VCL_DC_L[3:0]	0H
VGH_DC_L[3:0]	2H
VGL_DC_L[3:0]	0H
VGAM_DC_L[3:0]	0H
VCOM_DC_L[3:0]	0H
DISCH_L[3:0]	2H

8.3.6 PWRCON_CLK

This command is used to set power mode and charge pump circuit.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_CLK	W	1	0	1	1	1	0	0	0	B8h
Parameter	1	0	VGL_RT[2:0]			VGH_RT[3:0]				24h
Parameter	2	0	0	0	0	OTP_VGH_RT[3:0]				01h
Parameter	3	VCOM_EN_S[1:0]		DCDCM[1:0]		VGL_REG_SHT	0	VSP_PMIC[1:0]		30h
Parameter	4	0	VGL_CLK[2:0]			0	VCL_CLK[2:0]			34h
Parameter	5	0	PWRIC_CLK[2:0]			0	VGH_CLK[2:0]			53h

8.3.6.1: VGL_RT[2:0]

These registers are used to set VGL charge pump circuit.

VGL_RT[2:0]	VGL (V)
00h	VSN – VCI
01h	VSN – VSP
02h	2 * VSN – VCI
03h	2 * VSN – VSP
04h	Inhibited
05h	Inhibited
06h	Inhibited
07h	Inhibited

8.3.6.2: VGH_RT[3:0] , OTP_VGH_RT[3:0]

VGH_RT[3:0] : These registers are used to set VGH charge pump circuit for VGH.

OTP_VGH_RT[3:0] : These registers are used to set VGH charge pump circuit for OTP.

VGH_RT[3:0], OTP_VGH_RT[3:0]	VGH (V)
00h	VSP + VCI
01h	2 * VSP
02h	VSP – VSN + VCI
03h	2 * VSP – VSN
04h	2 * VSP – VSN + VCI
05h	3 * VSP – VSN
06h	2 * VSP – 2 * VSN + VCI
07h	3 * VSP – 2 * VSN
08h	Inhibited
0Ah	Inhibited
0Ch	Inhibited
0Eh	Inhibited

8.3.6.3: VCOM_EN_S[1:0]

These registers are used to set VCOM output status.

VCOM_EN_S[1:0]	VCOM Output
00h	Follow VCOM_DC_H[5:0]
01h	Sleep Out Command
02h	Display On Command
03h	Inhibited

8.3.6.4: DCDCM[1:0]

These registers are used to set power mode.

DCDCM[1:0]	VSP/VSN
00h	Inhibited
01h	Inhibited
02h	PMIC 0
03h	PMIC 1

8.3.6.5: VGL_REG_SHT

It is used to set VGL_REG power.

VGL_REG_SHT	VGL_REG
0h	Follow VGL_REG_S[5:0]
1h	VGL

8.3.6.6: VSP_PMIC[1:0]

These registers are used to set PMIC clock for VSP / VSN.

VSP_PMIC[1:0]	VSP / VSN
00h	PMIC 1
01h	PMIC 0
02h	Inhibited
03h	Inhibited

8.3.6.7: VGL_CLK[2:0], VCL_CLK[2:0], VGH_CLK[2:0]

VGL_CLK[2:0] : These registers are used to set VGL charge pump clock.

VCL_CLK[2:0] : These registers are used to set VCL charge pump clock.

VGH_CLK[2:0] : These registers are used to set VGH charge pump clock.

VGL_CLK[2:0], VCL_CLK[2:0], VGH_CLK[2:0]	CLOCK (HS)
00h	16HS
01h	8HS
02h	4HS
03h	2HS
04h	1HS
05h	1/2HS
06h	1/4HS
07h	1/8HS

8.3.6.8: PWRIC_CLK[2:0]

These registers are used to set IC pads VCSW1/ 2 pin output clock status.

PWRIC_CLK [2:0]	CLOCK (HS)
00h	8HS
01h	4HS
02h	2HS
03h	1HS
04h	1/2HS
05h	1/4HS
06h	1/6HS
07h	1/8HS

Hardware RESET	Default
VGL_RT[2:0]	2H
VGH_RT[3:0]	4H
OTP_VGH_RT[3:0]	1H
VCOM_EN_S[1:0]	0H
DCDCM[1:0]	3H
VGL_REG_SHT	0H
VSP_PMIC[1:0]	0H
VGL_CLK[2:0]	3H
VCL_CLK[2:0]	4H
PWRIC_CLK[2:0]	5H
VGH_CLK[2:0]	3H

8.3.7 PWRCON_BAT

This command is used to set abnormal power off.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_BAT	W	1	0	1	1	1	0	0	1	B9h
Parameter	1	1	0	1	0	0	0	1	0	A1h
Parameter	2	0	0	1	0	0	0	0	0	20h
Parameter	3	1	1	1	1	1	1	1	1	FFh
Parameter	4	GAS_ EN	GAS_IO_S[2:0]			GAS_VCI_S[3:0]				C4h

8.3.7.1: GAS_EN

It is used to set abnormal power off function.

GAS_EN	Function
0h	Disable
1h	Enable

8.3.7.2: VGS_IO_S[2:0]

VGS_IO_S[2:0] : These registers are used to set IOVCC power. Register Step 100mV

VGS_IO_S[2:0]	Voltage
0h	0.9V
1h	1.0V
2h	1.1V
3h	1.2V
4h	1.3V
5h	1.4V
6h	1.5V
7h	1.6V

8.3.7.3: VGS_VCI_S[3:0]

VGS_VCI_S[3:0]: These registers are used to detect VCI power. Register step =100mV

VGS_VCI_S[3:0]	Voltage
0h	1.7V
1h	1.8V
2h	1.9V
3h	2.0V
4h	2.1V
5h	2.2V
6h	2.3V
7h	2.4V
8h	2.8V
9h	3.0V
Ah	3.2V
Bh	3.4V
Ch	3.6V
Dh	3.8V
Eh	4.0V
Fh	4.2V

Hardware RESET	Default
GAS_EN	1H
GAS_IO_S[2:0]	4H
GAS_VCI_S[3:0]	4H

8.3.8 PWRCON_MODE

This command is used to set IC pads VCSW1/2 output mode for PMIC Clock.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_MODE	W	1	0	1	1	1	0	1	0	BAh
Parameter	1	VCSW 2_HZ	VCSW2_S[2:0]			VCSW 1_HZ	VCSW1_S[2:0]			27h
Parameter	2	0	1	1	0	0	0	1	1	63h

8.3.8.1: VCSW2_HZ, VCSW1_HZ

VCSW2_HZ: It is used to set IC pads VCSW2 floating.

VCSW1_HZ: It is used to set IC pads VCSW1 floating.

8.3.8.2: VCSW2_S[2:0], VCSW1_S[2:0]

These registers are used to set IC pads VCSW1/2 output status.

VCSW2_S[2:0] VCSW1_S[2:0]	Status
0h	VCI
1h	GND
2h	PWRIC_CLK
3h	PMIC_CLK1
4h	PMIC_CLK2
5h	Inhibited
6h	Inhibited
7h	IOVCC_DC

Hardware RESET	Default
VCSW2_HZ	0H
VCSW1_HZ	0H
VCSW2_S[2:0]	2H
VCSW1_S[2:0]	7H

8.3.9 PWRCON_REG

This command is used to set regulator power.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWRCON_REG	W	1	0	1	1	1	1	0	1	BDh
Parameter	1	0	1	0	VSP_S[4:0]					4Eh
Parameter	2	VCL_S[2:0]			VSN_S[4:0]					0Eh
Parameter	3	VSPR_S[7:0]								4Bh
Parameter	4	VSNR_S[7:0]								4Bh
Parameter	5	0	0	VGH_S[5:0]						20h
Parameter	6	0	0	VGL_S[5:0]						14h
Parameter	7	0	0	OTP_VGH_S[5:0]						00h
Parameter	8	0	0	VGL_REG_S[5:0]						14h
Parameter	9	0	1	0	0	0	0	1	1	43h
Parameter	10	0	0	0	0	0	0	1	1	03h

8.3.9.1: VSP_S[4:0]

These registers are used to set VSP output voltage. Register step 150mV.

VSP_S[4:0]	Voltage
00h	3V
01h	3.15V
02h	3.3V
……	……
0Dh	4.95V
0Eh	5.1V
0Fh	5.25V
……	……
15h	6.15V
16h	6.3V
17h	6.45V

8.3.9.2: VCL_S[2:0]

These registers are used to set VCL output voltage. Register step -100mV

VCL_S[2:0]	Voltage
0h	-2.5V
1h	-2.6V
2h	-2.7V
3h	-2.8V
4h	-2.9V
5h	-3.0V
6h	-3.1V
7h	-3.2V

8.3.9.3: VSN_S[4:0]

These registers are used to set VSN output voltage. Register step -150mV

VSN_S[4:0]	Voltage
00h	-3V
01h	-3.15V
02h	-3.3V
……	……
0Dh	-4.95V
0Eh	-5.1V
0Fh	-5.25V
……	……
15h	-6.15V
16h	-6.3V
17h	-6.45V

8.3.9.4: VSPR_S[7:0]

These registers are used to set VSPR output voltage for Positive Gamma. Register step 20mV.

VSPR_S[7:0]	Voltage
00h	3.0V
01h	3.02V
02h	3.04V
……	…..
0Dh	3.26V
0Eh	3.28V
0Fh	3.3V
……	……
3Bh	4.18V
3Ch	4.2V
3Dh	4.22V
……	…….
4Bh	4.5V
4Ch	4.52V
4Dh	4.54V
……	……
94h	5.96V
95h	5.98V
96h	6.0V

8.3.9.5: VSNR_S[7:0]

These registers are used to set VSNR output voltage for Negative Gamma. Register step -20mV.

VSNR_S[7:0]	Voltage
00h	-3.0V
01h	-3.02V
02h	-3.04V
……	…..
0Dh	-3.26V
0Eh	-3.28V
0Fh	-3.3V
……	
3Bh	-4.18V
3Ch	-4.2V
3Dh	-4.22V
……	…….
4Bh	-4.5V
4Ch	-4.52V
4Dh	-4.54V
……	……
94h	-5.96V
95h	-5.98V
96h	-6.0V

8.3.9.6: VGH_S[5:0], OTP_VGH_S[5:0]

VGH_S[5:0] : These registers are used to set VGH output voltage. Register step 200mV.

OTP_VGH_S[5:0]: These registers are used to set VGH power for OTP cell.

VGH_S[5:0]	Voltage
00h	8.6V
01h	8.8V
02h	9V
……	……
0Dh	11.2V
0Eh	11.4V
0Fh	11.6V
……	……
1Fh	14.8V
20h	15V
21h	15.2V
……	……
37h	19.6V
38h	19.8V
39h	20V

8.3.9.7: VGL_S[5:0]

These registers are used to set VGL output voltage. Register step -200mV.

VGL_S[5:0]	Voltage
00h	-6V
01h	-6.2V
02h	-6.4V
……	……
13h	-9.8V
14h	-10V
15h	-10.2V
……	……
1Dh	-11.8V
1Eh	-12V
1Fh	-12.2V
……	……
2Eh	-15.2V
2Fh	-15.4V
30h	-15.6V

8.3.9.8: VGL_REG_S[5:0]

These registers are used to set VGL_REG output voltage. Register step -200mV

VGL_S[5:0]	Voltage
00h	-5V
01h	-5.2V
02h	-5.4V
……	……
13h	-8.8V
14h	-9V
15h	-9.2V
……	……
1Dh	-10.8V
1Eh	-11V
1Fh	-11.2V
……	……
2Eh	-14.2V
2Fh	-14.4V
30h	-14.6V

Hardware RESET	Default
VSP_S[4:0]	0Eh
VCL_S[2:0]	00h
VSN_S[4:0]	0Eh
VSPR_S[7:0]	4Bh
VSNR_S[7:0]	4Bh
VGH_S[5:0]	20h
VGL_S[5:0]	14h
OTP_VGH_S[5:0]	00h
VGL_REG_S[5:0]	14h

8.3.10 BIST

This command is used to enable BIST function.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BIST	W	1	1	0	0	0	0	0	0	C0h
Parameter	1	0	0	0	1	0	0	0	BIST _ON	10h
Parameter	2	1	1	1	1	1	1	1	1	FFh
Parameter	3	1	1	1	1	1	1	1	1	FFh

8.3.10.1: BIST_ON

BIST_ON	Status
0h	Disable
1h	Enable

Hardware RESET	Default
BIST_ON	0h

8.3.11 TCON

This command is used to sets Vertical / Horizontal back porch / vertical front porch.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TCON	W	1	1	0	0	0	0	0	1	C1h
Parameter	1	VBP[7:0]								0Ch
Parameter	2	VFP[7:0]								10h
Parameter	3	VSW[7:0]								04h
Parameter	4	HBP[7:0]								0Ch
Parameter	5	HFP[7:0]								10h
Parameter	6	HSW[7:0]								04h

8.3.11.1: VBP[7:0], VFP[7:0],VSW[7:0]

VBP[7:0] : These registers are used to set Vertical back porch.

VFP[7:0] : These registers are used to set Vertical front porch.

VSW[7:0] : These registers are used to set Vertical low pulse width.

VBP[7:0] **VFP[7:0]** **VSW[7:0]**	**Line (HS)**
00h	Disable
01h	Disable
02h	2 HS
……	……
0Bh	11 HS
0Ch	12 HS
0Dh	13 HS
……	……
FDh	253 HS
FEh	254 HS
FFh	255 HS

8.3.11.2: HBP[7:0], HFP[7:0],HSW[7:0]

HBP[7:0] : These registers are used to set Horizontal back porch.

HFP[7:0] : These registers are used to set Horizontal front porch.

HSW[7:0] : These registers are used to set Horizontal low pulse width.

HBP[7:0] HFP[7:0] HSW[7:0]	Clock (DOTCLK)
00h	Disable
……	……
0Fh	Disable
10h	16 Clock
11h	17 Clock
……	……
FDh	253 Clock
FEh	254 Clock
FFh	255 Clock

Hardware RESET	Default
VBP[7:0]	0Ch
VFP[7:0]	10h
VSW[7:0]	04h
HBP[7:0]	0Ch
HFP[7:0]	10h
HSW[7:0]	04h

8.3.12 TCON2

This command is used to set Display resolution

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TCON2	W	1	1	0	0	0	0	1	0	C2h
Parameter	1	NL_ FIX	0	0	NL[8]	0	0	RSO[1:0]		82h
Parameter	2	NL[7:0]								10h

8.3.12.1: NL_FIX

It is used to set display resolution.

NL_FIX	Stauts
0h	NL[8:0]
1h	RSO[1:0]

8.3.12.2: NL[8:0]

These registers are used to set display resolution. Register step 4 HS.

NL[8:0]	Display Line (HS)
00h	Disable
01h	4 HS
10h	8 HS
……	……
A0h	640 HS
A1h	644HS
……	……
13Fh	1276 HS
140h	1280 HS

8.3.12.3: RSO[1:0]

RSO[1:0]	Display Line (HS)
00h	Disable
01h	600 HS
02h	720 HS
03h	800 HS

Hardware RESET	Default
NL_FIX	1h
NL[8:0]	10h
RSO[1:0]	1h

8.3.13 TCON3

This command is used to set TCON of display data and blanking frame.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TCON3	W	1	1	0	0	0	0	1	1	C3h
Parameter	1	0	I2O_BLKF_S[2:0]			BLK_KP	O2I_BLKF_S[2:0]			22h
Parameter	2	REV_EOR	B4_EOR	B3_EOR	B2_EOR	0	0	0	1	01h
Parameter	3	0	0	0	0	0	1	0	0	04h

8.3.13.1: I2O_BLKF_S[2:0], O2I_BLKF_S[2:0]

I2O_BLKF_S[2:0] : These registers are used to set SPIN to SPOUT blanking display frame number.

O2I_BLKF_S[2:0] :These registers are used to set SPOUT to SPIN blanking display frame number.

I2O_BLKF_S[2:0] O2I_BLKF_S[2:0]	Blanking (Frame)
0h	Disable Blanking
1h	1 Frame
2h	2 Frame
3h	3 Frame
4h	4 Frame
5h	5 Frame
6h	6 Frame
7h	7 Frame

8.3.13.2: BLK_KP

It is used to keep blanking display in display off status.

BLK_KP	Blanking
0	Stop
1	Keep

8.3.13.3: REV_EOR

REV_EOR : It is used to set exclusive OR command INVON.

REV_EOR	INVON	Display
0	0	Normal Display
0	1	Inversion Display

1	0	Inversion Display
1	1	Normal Display

8.3.13.4: B4_EOR

B4_EOR : It is used to set exclusive OR command MADTCL D4 function.

B4_EOR	MADTCL D4 (ML)	Display
0	0	Top → Bottom
0	1	Bottom → Top
1	0	Bottom → Top
1	1	Top → Bottom

8.3.13.5: B3_EOR

B3_EOR : It is used to set exclusive OR command MADTCL D3 function.

B3_EOR	MADTCL D3 (RGB)	Display
0	0	RGB order
0	1	BGR order
1	0	BGR order
1	1	RGB order

8.3.13.6: B2_EOR

B2_EOR : It is used to set exclusive OR command MADTCL D2 function.

B2_EOR	MADTCL D2 (MH)	Display
0	0	Left → Right
0	1	Right → Left
1	0	Right → Left
1	1	Left → Right

Hardware RESET	Default
I2O_BLKF_S[2:0]	2h
O2I_BLKF_S[2:0]	2h
BLK_KP	0h
REV_EOR	0h
B4_EOR	0h
B3_EOR	0h
B2_EOR	0h

8.3.14 DSTB

This is used to set deep standby mode.

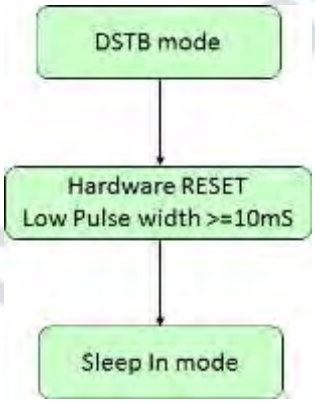
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DSTB	W	1	1	0	0	0	1	0	0	C4h
Parameter	1	0	0	0	0	0	0	0	DSTB	01h

8.3.14.1: DSTB

It is used to set deep standby mode.

DSTB	Status
0h	Deep Standby mode OFF
1h	Deep Standby mode ON

8.3.14.2: Exit DSTB Sequence



Hardware RESET	Default
DSTB	0h

8.3.15 SRC_TIM

This command is used to set source timing.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SRC_TIM	W	1	1	0	0	0	1	1	0	C6h
Parameter	1	SD1[7:0]								08h
Parameter	2	SD2[7:0]								10h
Parameter	3	SD3[7:0]								68h
Parameter	4	OP_ON[7:0]								08h
Parameter	5	0	0	0	1	0	1	1	0	16h
Parameter	6	OP_OFF[7:0]								60h
Parameter	7	0	0	1	1	0	1	1	0	36h
Parameter	8	0	0	0	0	0	0	0	0	00h

8.3.15.1: SD1[7:0], SD2[7:0], SD3[7:0], OP_ON[7:0], OP_OFF[7:0]

SD1[7:0] : These registers are used to set EQ pull gnd time. Register Step 4 x Osc clock.

SD2[7:0] : These registers are used to set EQ pre-charge to VCI/ IOVCC/ VCL time. Register Step 4 x Osc clock.

SD3[7:0]: These registers are used to set source Data + / Data- output time. Register Step 4 x Osc clock.

OP_ON[7:0] : These registers are used to set source OP enable time. Register Step 4 x Osc clock.

OP_OFF[7:0]: These registers are used to set source OP disable time. Register Step 4 x Osc clock.

SD1[7:0], SD2[7:0], SD3[7:0], OP_ON[7:0] ,OP_OFF[7:0]	Clock (Oscillator)
0h	0 Clock
1h	4 Clock
2h	8 Clock
……	……
1Fh	124 Clock
20h	128 Clock
21h	132 Clock
……	……
FDh	1012 Clock
FEh	1016 Clock
FFh	1020 Clock

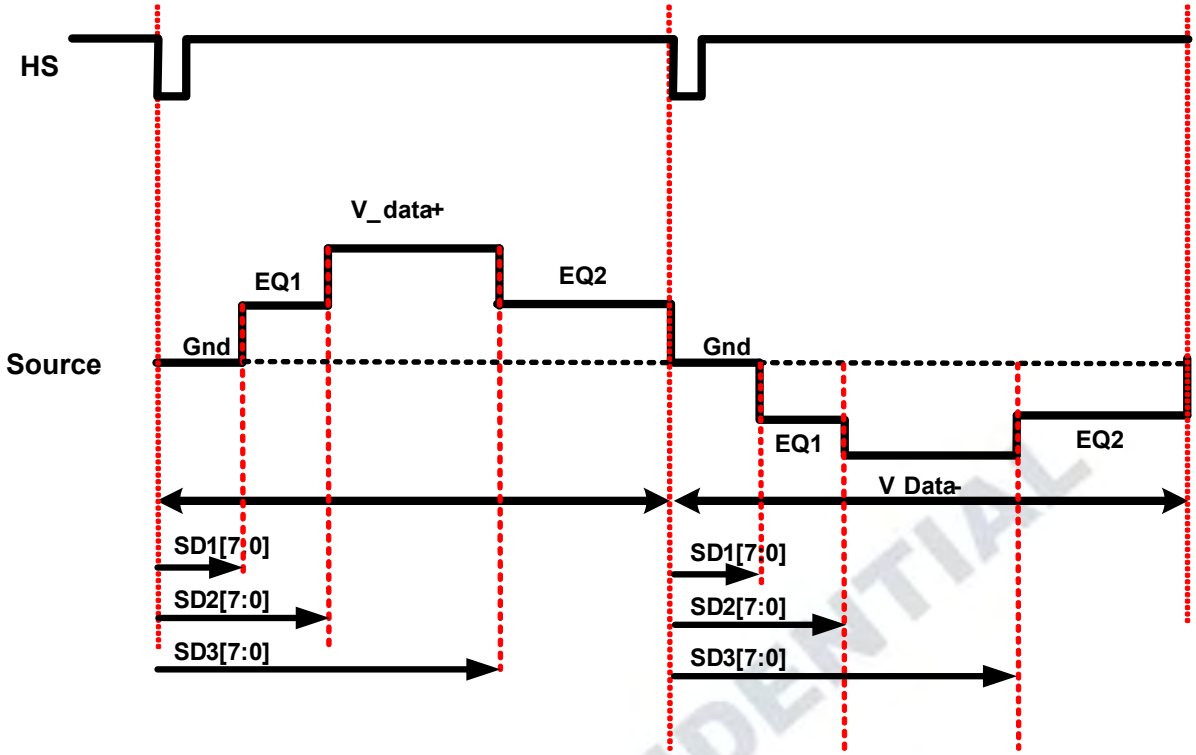


Figure 8.3.15-1: Source / EQ relationship

Note 1: Oscillator = 45MHz.
Note2: EQ2 time = 1HS – SD3[7:0].
Note3: OP_ON[7:0] value = SD1[7:0] value.
Note4 : OP_OFF[7:0] value = SD3[7:0] value.

Hardware RESET	Default
SD1[7:0]	08h
SD2[7:0]	10h
SD3[7:0]	68h
OP_ON[7:0]	08h
OP_OFF[7:0]	60h

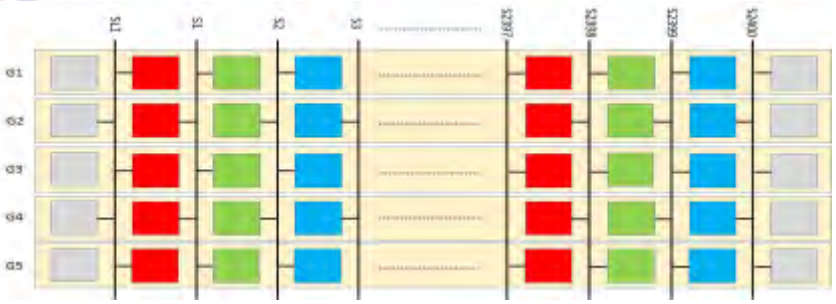
8.3.16 SRCCON

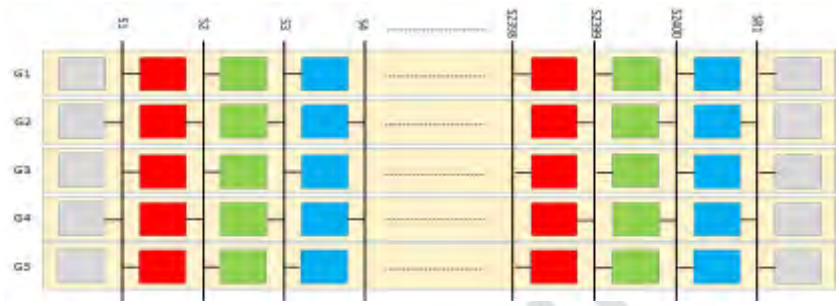
This command is used to control source.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SRCCON	W	1	1	0	0	0	1	1	1	C7h
Parameter	1	0	0	Z_SHIFT	Z_LINE	0	INV_SEL[2:0]			05h
Parameter	2	0	0	1	0	0	0	1	1	23h
Parameter	3	0	SMEOFF	1	0	1	0	1	1	2Bh
Parameter	4	0	1	0	0	0	0	0	1	41h
Parameter	5	PORCH_HIZ	PORCH_GND	SDSW_DATA	SDPORCH_DATA	0	NEQSTOP	0	0	00h

8.3.16.1: Z_SHIFT, Z_LINE:

It is used to set Zig-Zag Panel Type

Z_SHIFT	Z_LINE	Zig-Zag Panel Type
0	0	
0	1	

1	0	
1	1	

8.3.16.2: INV_SEL[2:0]

These registers are used to set the inversion type.

INV_SEL[2:0]	Status
0h	1 dot inversion
1h	1+2 dot inversion
2h	2 dot inversion
3h	4 dot inversion
4h	8 dot inversion
5h	Column inversion
6h	Zig- Zag inversion
7h	Disable

8.3.16.3: SMEOFF

It is used to set smart EQ control.

SMEOFF	SMART EQ
0h	Disable
1h	Enable

8.3.16.4: PORCH_HIZ

It is used to set Non display area source state.

PORCH_HZ	Status
0h	GND / V0 / V255
1h	HZ / GND

8.3.16.5: PORCH_GND

It is used to set Non display area source state.

PORCH_GND	Status
0h	Hiz / V0 / V255
1h	GND

8.3.16.6: SDPORCH_DATA

It is used to set Non display area source state.

SDPORCH_DATA	Status
0h	V0
1h	V255

8.3.16.7: SDSW_DATA

It is used to set Blanking frame source state.

SDSW_DATA	Status
0h	V0
1h	V255

8.3.16.8: NEQSTOP

It is used to set negative EQ ON / OFF.

NEQSTOP	Status
0h	Enable
1h	Disable

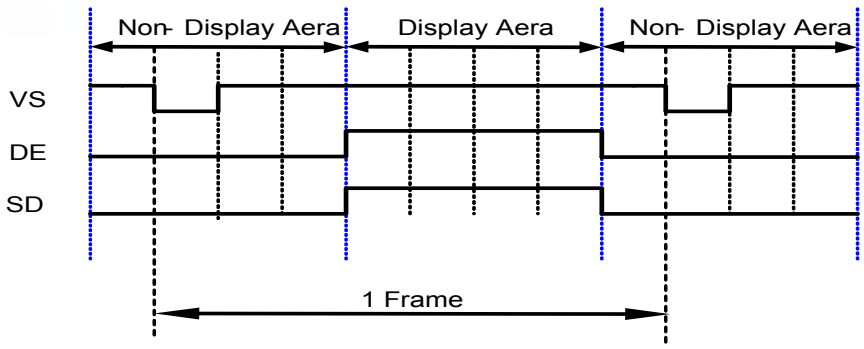


Figure 8.3.16-1: Non-Display Area and Display Area relationship.

Hardware RESET	Default
Z_SHIFT	0h
Z_LINE	0h
INV_SEL[2:0]	5h
SMEQOFF	0h
PORCH_HIZ	0h
PORCH_GND	0h
SDSW_DATA	0h
SDPORCH_DATA	0h
NEQSTOP	0h

8.3.17 SET_GAMMA

This command is used to set analog gamma for display quality.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SET_GAMMA	W	1	1	0	0	1	0	0	0	C8h
Parameter	1	0	VPR18[6:0]							7Ch
Parameter	2	0	VPR17[6:0]							6Dh
Parameter	3	0	VPR16[6:0]							63h
Parameter	4	0	VPR15[6:0]							59h
Parameter	5	0	VPR14[6:0]							57h
Parameter	6	0	VPR13[6:0]							4Ah
Parameter	7	0	VPR12[6:0]							51h
Parameter	8	0	VPR11[6:0]							3Ah
Parameter	9	0	VPR10[6:0]							55h
Parameter	10	0	VPR9[6:0]							53h
Parameter	11	0	VPR8[6:0]							55h
Parameter	12	0	VPR7[6:0]							7Ah
Parameter	13	0	VPR6[6:0]							6Fh
Parameter	14	0	VPR5[6:0]							7Fh
Parameter	15	0	VPR4[6:0]							75h
Parameter	16	0	VPR3[6:0]							72h
Parameter	17	0	VPR2[6:0]							62h
Parameter	18	0	VPR1[6:0]							2Dh
Parameter	19	0	VPR0[6:0]							06h
Parameter	20	0	VNR18[6:0]							7Ch
Parameter	21	0	VNR17[6:0]							6Dh
Parameter	22	0	VNR16[6:0]							63h
Parameter	23	0	VNR15[6:0]							59h
Parameter	24	0	VNR14[6:0]							57h
Parameter	25	0	VNR13[6:0]							4Ah
Parameter	26	0	VNR12[6:0]							51h
Parameter	27	0	VNR11[6:0]							3Ah
Parameter	28	0	VNR10[6:0]							55h
Parameter	29	0	VNR9[6:0]							53h
Parameter	30	0	VNR8[6:0]							55h
Parameter	31	0	VNR7[6:0]							7Ah
Parameter	32	0	VNR6[6:0]							6Fh

Parameter	33	0	VNR5[6:0]	7Fh
Parameter	34	0	VNR4[6:0]	75h
Parameter	35	0	VNR3[6:0]	72h
Parameter	36	0	VNR2[6:0]	62h
Parameter	37	0	VNR1[6:0]	2Dh
Parameter	38	0	VNR0[6:0]	06h

8.3.17.1: VPR(n)[6:0]:

These registers are used to set positive gamma.

	VPR(n) [6:0]	Gray	
		Normal Black Panel	Normal White Panel
Positive	18	255	0
	17	251	4
	16	247	8
	15	243	12
	14	235	20
	13	227	28
	12	211	44
	11	191	64
	10	159	96
	9	128	128
	8	96	159
	7	64	191
	6	44	211
	5	28	227
	4	20	235
	3	12	243
	2	8	247
	1	4	251
	0	0	255

8.3.17.2: VNR(n)[6:0]:

These registers are used to set negative gamma.

	VNR(n) [6:0]	Gray	
		Normal Black Panel	Normal White Panel
Negative	18	255	0
	17	251	4
	16	247	8
	15	243	12
	14	235	20
	13	227	28
	12	211	44
	11	191	64
	10	159	96
	9	128	128
	8	96	159
	7	64	191
	6	44	211
	5	28	227
	4	20	235
	3	12	243
	2	8	247
	1	4	251
	0	0	255

8.3.18 CE_CTR

This command is used to set color enhancement

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CE_CTR	W	1	1	0	0	1	0	1	0	CAh
Parameter	1	0	0	0	0	0	0	0	0	00h
Parameter	2	0	0	0	0	0	0	0	CE_ CTR	00h
Parameter	3	0	0	0	0	0	0	0	0	00h

8.3.18.1: CE_CTR

It is used to set color enhancement.

CE_CTR	Status
0h	Disable
1h	Enable

Hardware RESET	Default
CE_CTR	0h

8.3.19 OTP_AUTO_PROG

This command is used to set OTP Programming.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SRC_TIM	W	1	1	0	0	1	0	1	1	CBh
Parameter	1	0	0	0	OTP_BANK 4	OTP_BANK 3	OTP_BANK 2	OTP_BANK 1	OTP_BANK 0	03h
Parameter	2	0	0	0	0	0	0	0	OTP_INT_VPP	00h
Parameter	3	0	0	0	0	0	0	0	OTP_AUTO_PROG	00h

8.3.19.1: OTP_BANK 4, OTP_BANK 3, OTP_BANK 2, OTP_BANK 1, OTP_BANK 0

These registers are used to set OTP bank.

OTP_BANK	Status
Bank 0	ID Code
Bank 1	VCOM
Bank 2	Level 2
Bank 3	Level 2
Bank 4	Level 2

8.3.19.2: OTP_INT_VPP

It is used to set OTP power.

OTP_INT_VPP	Status
0h	External Power (VPP pad (8.5V))
1h	Internal Power (OTP_VGH_RT[3:0])

8.3.19.2: OTP_AUTO_PROG

It is used to set OTP cell.

OTP_AUTO_PROG	Status
0h	Disable
1h	Enable

Hardware RESET	Default
OTP_BANK 4	0h
OTP_BANK 3	0h
OTP_BANK 2	0h
OTP_BANK 1	1h
OTP_BANK 0	1h
OTP_INT_VPP	0h
OTP_AUTO_PROG	0h

8.3.20 ABNO_CTR

This command is used to set MIPI abnormal state.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ABNO_CTR	W	1	1	0	1	0	0	0	0	D0h
Parameter	1	0	0	0	0	0	FS_BLK	1	FS_EN	07h
Parameter	2	FS_DETECT[7:0]								10h
Parameter	3	BATON_CNT[7:0]								00h

8.3.20.1: FS_BLK

It is used to set MIPI abnormal display state.

FS_BLK	Status
0h	GND
1h	Blanking display

8.3.20.2: FS_EN

It is used to set MIPI abnormal function.

FS_EN	Status
0h	Disable
1h	Enable

8.3.20.3: FS_DETECT[7:0]

These registers are used to set timing of MIPI abnormal. Register step 22uS

FS_DETECT[7:0]	Time (uS)
0h	0uS
1h	22uS
2h	44uS
……	……
0Fh	330uS
10h	352uS
……	……
FEh	5588 uS
FFh	5610 uS

8.3.20.3: BATON_CON[7:0]

These registers used to set timing of power abnormal. Register step 0.088uS

BATON_CON[7:0]	Time (uS)
0h	0uS
1h	0.088uS
2h	0.176uS
……	……
0Fh	1.32uS
10h	1.408uS
……	……
FEh	22.352uS
FFh	22.44uS

Hardware RESET	Default
FS_BLK	1h
FS_EN	1h
FS_DETECT[7:0]	10h
BATON_CON[7:0]	00h

8.3.21 PWM_CTR

This command is used to set PWM clock.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWM_CTR	W	1	1	1	0	0	0	0	0	E0h
Parameter	1	0	0	1	1	PWM_POL	0	PWM_EN	0	32h
Parameter	2	PWM[7:0]								03h
Parameter	3	0	0	1	0	0	0	0	0	20h
Parameter	4	0	0	0	0	0	0	0	0	00h
Parameter	5	1	1	1	1	1	1	1	1	FFh

8.3.21.1: PWM_POL

It is used to set inverse CABC_PWM_OUT output

PWM_POL	CABC_PWM_OUT
0h	Original
1h	Inversed

8.3.21.2: PWM_EN

It is used to set PWM output.

PWM_EN	Frequency
0h	Disable
1h	Enable

8.3.21.3: PWM[7:0]

These registers are used to set PWM frequency. Register step 120Hz

PWM[7:0]	Frequency (Hz)
0h	120Hz
1h	240Hz
2h	360Hz
……	……
7Fh	15360Hz
80h	15480Hz
……	……
FEh	30600Hz
FFh	30720Hz

Hardware RESET	Default
PWM_POL	0h
PWM_EN	1h
PWM[7:0]	03h

8.3.22 DGC_CTR

This command is used to control digital gamma.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_CTR	W	1	1	1	0	0	0	1	1	E3h
Parameter	1	0	0	0	0	0	0	DTR_EN	DGC_EN	00h

8.3.22.1: DTR_EN

It is used to set dithering function.

DTR_EN	Status
0h	Disable
1h	Enable

8.3.22.2: DGC_EN

It is used to set digital gamma function

DGC_EN	Status
0h	Disable
1h	Enable

Hardware RESET	Default
DTR_EN	0h
DGC_EN	0h

8.3.23 DGC_R

This command is used to set digital gamma gray red.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_R	W	1	1	1	0	0	1	0	0	E4h
Parameter	1	DGC_R_V255[9:2]								FFh
Parameter	2	DGC_R_V254[9:2]								FEh
Parameter	3	DGC_R_V252[9:2]								FCh
Parameter	4	DGC_R_V250[9:2]								FAh
Parameter	5	DGC_R_V248[9:2]								F8h
Parameter	6	DGC_R_V244[9:2]								F4h
Parameter	7	DGC_R_V240[9:2]								F0h
Parameter	8	DGC_R_V232[9:2]								E8h
Parameter	9	DGC_R_V224[9:2]								E0h
Parameter	10	DGC_R_V208[9:2]								D0h
Parameter	11	DGC_R_V192[9:2]								C0h
Parameter	12	DGC_R_V160[9:2]								A0h
Parameter	13	DGC_R_V128[9:2]								80h
Parameter	14	DGC_R_V127[9:2]								7Fh
Parameter	15	DGC_R_V95[9:2]								5Fh
Parameter	16	DGC_R_V63[9:2]								3Fh
Parameter	17	DGC_R_V47[9:2]								2Fh
Parameter	18	DGC_R_V31[9:2]								1Fh
Parameter	19	DGC_R_V23[9:2]								17h
Parameter	20	DGC_R_V15[9:2]								0Fh
Parameter	21	DGC_R_V11[9:2]								0Bh
Parameter	22	DGC_R_V7[9:2]								07h
Parameter	23	DGC_R_V5[9:2]								05h
Parameter	24	DGC_R_V3[9:2]								03h
Parameter	25	DGC_R_V1[9:2]								01h
Parameter	26	DGC_R_V0[9:2]								00h

8.3.24 DGC_G

This command is used to set digital gamma gray green.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_G	W	1	1	1	0	0	1	0	1	E5h
Parameter	1	DGC_G_V255[9:2]								FFh
Parameter	2	DGC_G_V254[9:2]								FEh
Parameter	3	DGC_G_V252[9:2]								FCh
Parameter	4	DGC_G_V250[9:2]								FAh
Parameter	5	DGC_G_V248[9:2]								F8h
Parameter	6	DGC_G_V244[9:2]								F4h
Parameter	7	DGC_G_V240[9:2]								F0h
Parameter	8	DGC_G_V232[9:2]								E8h
Parameter	9	DGC_G_V224[9:2]								E0h
Parameter	10	DGC_G_V208[9:2]								D0h
Parameter	11	DGC_G_V192[9:2]								C0h
Parameter	12	DGC_G_V160[9:2]								A0h
Parameter	13	DGC_G_V128[9:2]								80h
Parameter	14	DGC_G_V127[9:2]								7Fh
Parameter	15	DGC_G_V95[9:2]								5Fh
Parameter	16	DGC_G_V63[9:2]								3Fh
Parameter	17	DGC_G_V47[9:2]								2Fh
Parameter	18	DGC_G_V31[9:2]								1Fh
Parameter	19	DGC_G_V23[9:2]								17h
Parameter	20	DGC_G_V15[9:2]								0Fh
Parameter	21	DGC_G_V11[9:2]								0Bh
Parameter	22	DGC_G_V7[9:2]								07h
Parameter	23	DGC_G_V5[9:2]								05h
Parameter	24	DGC_G_V3[9:2]								03h
Parameter	25	DGC_G_V1[9:2]								01h
Parameter	26	DGC_G_V0[9:2]								00h

8.3.25 DGC_B

This command is used to set digital gamma gray blue

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_B	W	1	1	1	0	0	1	1	0	E6h
Parameter	1	DGC_B_V255[9:2]								FFh
Parameter	2	DGC_B_V254[9:2]								FEh
Parameter	3	DGC_B_V252[9:2]								FCh
Parameter	4	DGC_B_V250[9:2]								FAh
Parameter	5	DGC_B_V248[9:2]								F8h
Parameter	6	DGC_B_V244[9:2]								F4h
Parameter	7	DGC_B_V240[9:2]								F0h
Parameter	8	DGC_B_V232[9:2]								E8h
Parameter	9	DGC_B_V224[9:2]								E0h
Parameter	10	DGC_B_V208[9:2]								D0h
Parameter	11	DGC_B_V192[9:2]								C0h
Parameter	12	DGC_B_V160[9:2]								A0h
Parameter	13	DGC_B_V128[9:2]								80h
Parameter	14	DGC_B_V127[9:2]								7Fh
Parameter	15	DGC_B_V95[9:2]								5Fh
Parameter	16	DGC_B_V63[9:2]								3Fh
Parameter	17	DGC_B_V47[9:2]								2Fh
Parameter	18	DGC_B_V31[9:2]								1Fh
Parameter	19	DGC_B_V23[9:2]								17h
Parameter	20	DGC_B_V15[9:2]								0Fh
Parameter	21	DGC_B_V11[9:2]								0Bh
Parameter	22	DGC_B_V7[9:2]								07h
Parameter	23	DGC_B_V5[9:2]								05h
Parameter	24	DGC_B_V3[9:2]								03h
Parameter	25	DGC_B_V1[9:2]								01h
Parameter	26	DGC_B_V0[9:2]								00h

8.3.26 DGC_R_L

This command is used to set digital gamma gray red.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_R_L	W	1	1	1	0	0	1	1	1	E7h
Parameter	1	DGC_R_V255[1:0]		DGC_R_V254[1:0]		DGC_R_V252[1:0]		DGC_R_V250[1:0]		00h
Parameter	2	DGC_R_V248[1:0]		DGC_R_V244[1:0]		DGC_R_V240[1:0]		DGC_R_V232[1:0]		00h
Parameter	3	DGC_R_V224[1:0]		DGC_R_V208[1:0]		DGC_R_V192[1:0]		DGC_R_V160[1:0]		00h
Parameter	4	DGC_R_V128[1:0]		DGC_R_V127[1:0]		DGC_R_V95[1:0]		DGC_R_V63[1:0]		00h
Parameter	5	DGC_R_V47[1:0]		DGC_R_V31[1:0]		DGC_R_V23[1:0]		DGC_R_V15[1:0]		00h
Parameter	6	DGC_R_V11[1:0]		DGC_R_V7[1:0]		DGC_R_V5[1:0]		DGC_R_V3[1:0]		00h
Parameter	7	DGC_R_V1[1:0]		DGC_R_V0[1:0]		0	0	0	0	00h

8.3.27 DGC_G_L

This command is used to set digital gamma gray green.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_G_L	W	1	1	1	0	1	0	0	0	E8h
Parameter	1	DGC_G_V255[1:0]		DGC_G_V254[1:0]		DGC_G_V252[1:0]		DGC_G_V250[1:0]		00h
Parameter	2	DGC_G_V248[1:0]		DGC_G_V244[1:0]		DGC_G_V240[1:0]		DGC_G_V232[1:0]		00h
Parameter	3	DGC_G_V224[1:0]		DGC_G_V208[1:0]		DGC_G_V192[1:0]		DGC_G_V160[1:0]		00h
Parameter	4	DGC_G_V128[1:0]		DGC_G_V127[1:0]		DGC_G_V95[1:0]		DGC_G_V63[1:0]		00h
Parameter	5	DGC_G_V47[1:0]		DGC_G_V31[1:0]		DGC_G_V23[1:0]		DGC_G_V15[1:0]		00h
Parameter	6	DGC_G_V11[1:0]		DGC_G_V7[1:0]		DGC_G_V5[1:0]		DGC_G_V3[1:0]		00h
Parameter	7	DGC_G_V1[1:0]		DGC_G_V0[1:0]		0	0	0	0	00h

8.3.28 DGC_B_L

This command is used to set digital gamma gray blue.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DGC_B_L	W	1	1	1	0	1	0	0	1	E9h
Parameter	1	DGC_B_V255[1:0]		DGC_B_V254[1:0]		DGC_B_V252[1:0]		DGC_B_V250[1:0]		00h
Parameter	2	DGC_B_V248[1:0]		DGC_B_V244[1:0]		DGC_B_V240[1:0]		DGC_B_V232[1:0]		00h
Parameter	3	DGC_B_V224[1:0]		DGC_B_V208[1:0]		DGC_B_V192[1:0]		DGC_B_V160[1:0]		00h
Parameter	4	DGC_B_V128[1:0]		DGC_B_V127[1:0]		DGC_B_V95[1:0]		DGC_B_V63[1:0]		00h
Parameter	5	DGC_B_V47[1:0]		DGC_B_V31[1:0]		DGC_B_V23[1:0]		DGC_B_V15[1:0]		00h
Parameter	6	DGC_B_V11[1:0]		DGC_B_V7[1:0]		DGC_B_V5[1:0]		DGC_B_V3[1:0]		00h
Parameter	7	DGC_B_V1[1:0]		DGC_B_V0[1:0]		0	0	0	0	00h

8.3.29 PASSWORD1

This command is used to enable Level 2 and OTP Function.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PASSWORD1	W	1	1	1	1	0	0	0	0	F0h
Parameter	1	Password1_1[7:0]								A5
Parameter	2	Password1_2[7:0]								A5

This Password is for accessing Level 2 registers.

Password1_1[7:0]: This register should be set to “5Ah” for writing / reading Level 2 registers.
Password1_2[7:0]: This register should be set to “5Ah” for writing / reading Level 2 registers.
Password1_1[7:0]: This register should be set to “B4h” for writing / reading Level 2 and OTP registers.
Password1_2[7:0]: This register should be set to “4Bh” for writing / reading Level 2 and OTP registers.

8.3.30 PASSWORD2

This command is used to enable Level 2 and OTP Function.

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PASSWORD2	W	1	1	1	1	0	0	0	1	F1h
Parameter	1	Password2_1[7:0]								5Ah
Parameter	2	Password2_2[7:0]								5Ah

This Password is for accessing Level 2 registers.

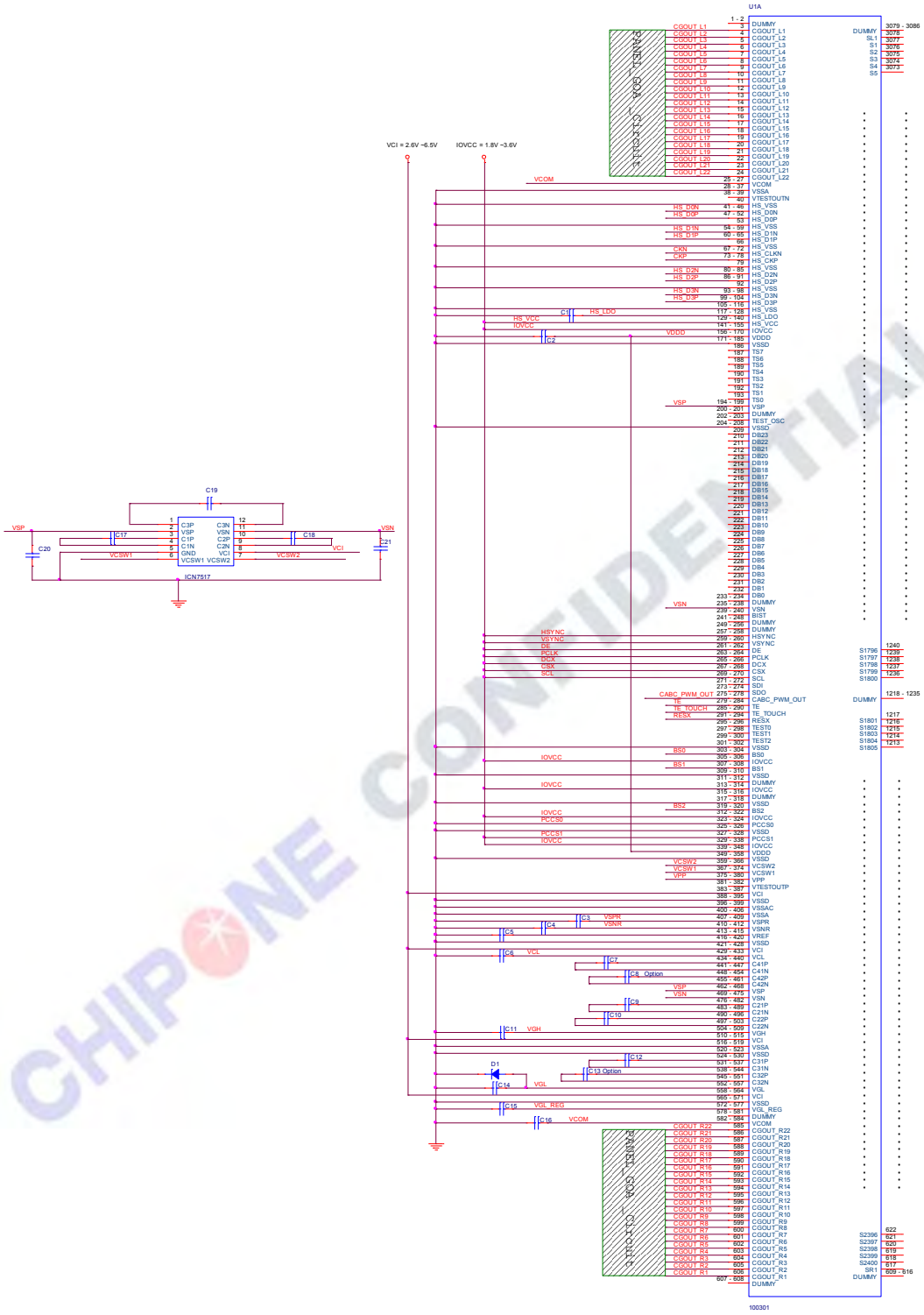
Password1_1[7:0]: This register should be set to “A5h” for writing / reading Level 2 registers.
Password1_2[7:0]: This register should be set to “A5h” for writing / reading Level 2 registers.

9、Application

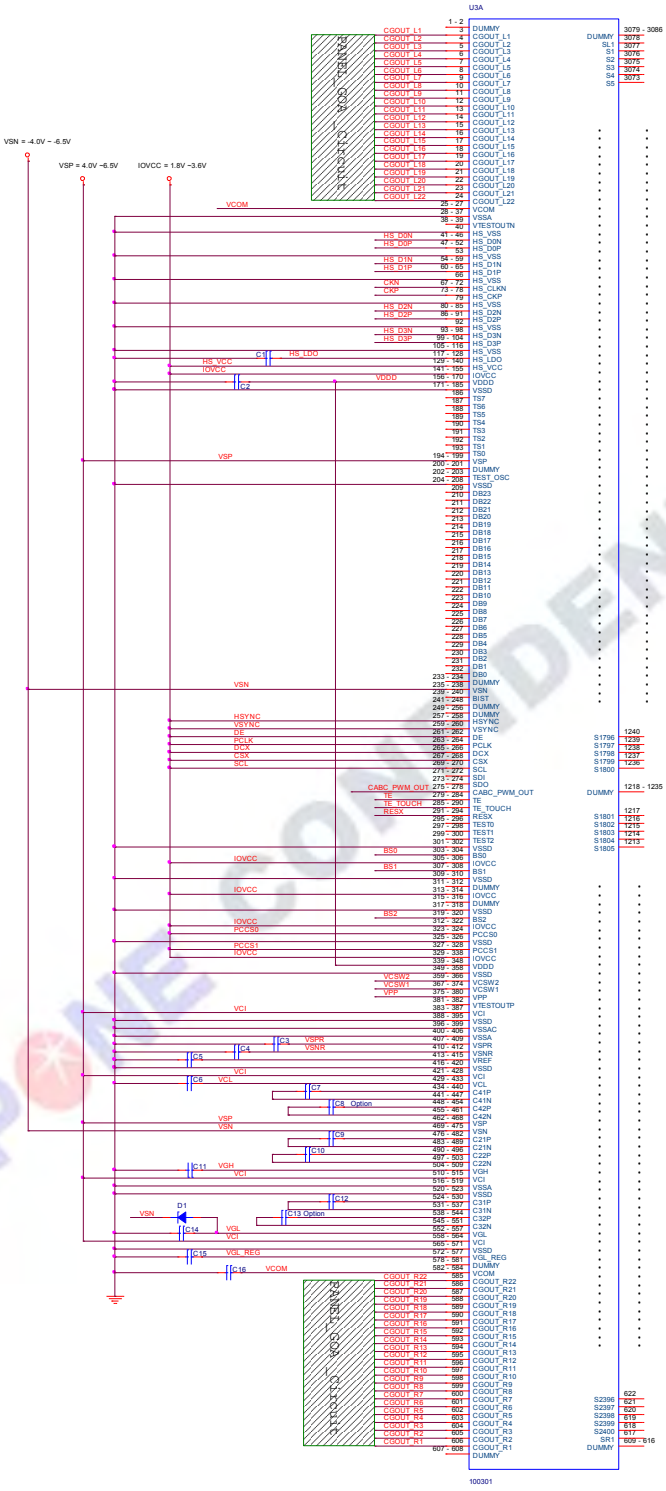
9.1、PCCS [1:0] = 0,0 Mode

BUMP UP View

9.2、PCCS [1:0] = 1,0 Mode



9.3、PCCS [1:0] = 1,1 Mode



9.4、External Components Connection

9.4.1 PCCS[1:0] = 0,0 Mode

Pad Name	Symbol	Connection	Typical Component Value
HS_LDO	C1	Connect to Capacitor (Max :6V): HS_LDO(+) ----| |---- (-) GND	1.0uF
VDDD	C2	Connect to Capacitor (Max :6V): VDDD(+) ----| |---- (-) GND	1.0uF
VSPR	C3 (Option)	Connect to Capacitor (Max :10V): VSPR(+) ----| |---- (-) GND	1.0uF
VSNR	C4 (Option)	Connect to Capacitor (Max :10V): VSNR(-) ----| |---- (+) GND	1.0uF
VREF	C5 (Option)	Connect to Capacitor (Max :6V): VREF(+) ----| |---- (-) GND	1.0uF
VCL	C6	Connect to Capacitor (Max :6V): VCL(-) ----| |---- (+) GND	1.0uF
C41P - C41N	C7 (Option)	Connect to Capacitor (Max :6V): C41P(+) ----| |---- (-) C41N	1.0uF
C42P – C42N	C8 (Option)	Connect to Capacitor (Max :6V): C42P (+) ----| |---- (-) C42N	1.0uF
VGL	D1	Connect to Schottky Diode (VR>= 30V) VGL(+) ----▶|----(-) VSN	VF<0.4V / 20mA @25℃,VR> =30V
VGL_REG	C15 (Option)	Connect to Capacitor (Max :25V): VGL_REG(-) ----| |---- (+) GND	1.0uF
VCOM	C16	Connect to Capacitor (Max :6V): VCOM(-) ----| |---- (+) GND	2.2uF

9.4.1 PCCS[1:0] = 1,0 Mode

Pad Name	Symbol	Connection	Typical Component Value
HS_LDO	C1	Connect to Capacitor (Max :6V): HS_LDO(+) ----| |---- (-) GND	1.0uF
VDDD	C2	Connect to Capacitor (Max :6V): VDDD(+) ----| |---- (-) GND	1.0uF
VSPR	C3 (Option)	Connect to Capacitor (Max :10V): VSPR(+) ----| |---- (-) GND	1.0uF
VSNR	C4 (Option)	Connect to Capacitor (Max :10V): VSNR(-) ----| |---- (+) GND	1.0uF
VREF	C5 (Option)	Connect to Capacitor (Max :6V): VREF(+) ----| |---- (-) GND	1.0uF
VCL	C6	Connect to Capacitor (Max :6V): VCL(-) ----| |---- (+) GND	1.0uF
C41P - C41N	C7 (Option)	Connect to Capacitor (Max :6V): C41P(+) ----| |---- (-) C41N	1.0uF
C42P – C42N	C8 (Option)	Connect to Capacitor (Max :6V): C42P (+) ----| |---- (-) C42N	1.0uF
C21P – C21N	C9	Connect to Capacitor (Max :25V): C21P (+) ----| |---- (-) C21N	1.0uF
C22P – C22N	C10	Connect to Capacitor (Max :25V): C22P (+) ----| |---- (-) C22N	1.0uF
VGH	C11	Connect to Capacitor (Max :25V): VGH (+) ----| |---- (-) GND	1.0uF
C31P – C31N	C12	Connect to Capacitor (Max :25V): C31P (+) ----| |---- (-) C31N	1.0uF
C32P – C32N	C13 (Option)	Connect to Capacitor (Max :25V): C32P (+) ----| |---- (-) C32N	1.0uF
VGL	C14	Connect to Capacitor (Max :25V): VGL (-) ----| |---- (+) GND	1.0uF
VGL	D1	Connect to Schottky Diode (VR>= 30V) VGL(+) ----▶|----(-) GND	VF<0.4V / 20mA @25℃,VR> =30V
VGL_REG	C15 (Option)	Connect to Capacitor (Max :25V): VGL_REG(-) ----| |---- (+) GND	1.0uF
VCOM	C16	Connect to Capacitor (Max :6V): VCOM(-) ----| |---- (+) GND	2.2uF

C1P – C1N (ICN7517)	C17	Connect to Capacitor (Max :10V): C1P (+) ----| |---- (-) C1N	1.0uF
C2P – C2N (ICN7517)	C18	Connect to Capacitor (Max :10V): C2P (+) ----| |---- (-) C2N	1.0uF
C3P – C3N (ICN7517)	C19	Connect to Capacitor (Max :10V): C3P (+) ----| |---- (-) C3N	1.0uF
VSP	C20	Connect to Capacitor (Max :10V): VSP (+) ----| |---- (-) GND	2.2uF
VSN	C21	Connect to Capacitor (Max :10V): VSN (-) ----| |---- (+) GND	2.2uF

9.4.1 PCCS[1:0] = 1,1 Mode

Pad Name	Symbol	Connection	Typical Component Value
HS_LDO	C1	Connect to Capacitor (Max :6V): HS_LDO(+) ----| |---- (-) GND	1.0uF
VDDD	C2	Connect to Capacitor (Max :6V): VDDD(+) ----| |---- (-) GND	1.0uF
VSPR	C3 (Option)	Connect to Capacitor (Max :10V): VSPR(+) ----| |---- (-) GND	1.0uF
VSNR	C4 (Option)	Connect to Capacitor (Max :10V): VSNR(-) ----| |---- (+) GND	1.0uF
VREF	C5 (Option)	Connect to Capacitor (Max :6V): VREF(+) ----| |---- (-) GND	1.0uF
VCL	C6	Connect to Capacitor (Max :6V): VCL(-) ----| |---- (+) GND	1.0uF
C41P - C41N	C7 (Option)	Connect to Capacitor (Max :6V): C41P(+) ----| |---- (-) C41N	1.0uF
C42P – C42N	C8 (Option)	Connect to Capacitor (Max :6V): C42P (+) ----| |---- (-) C42N	1.0uF
C21P – C21N	C9	Connect to Capacitor (Max :25V): C21P (+) ----| |---- (-) C21N	1.0uF
C22P – C22N	C10	Connect to Capacitor (Max :25V): C22P (+) ----| |---- (-) C22N	1.0uF
VGH	C11	Connect to Capacitor (Max :25V): VGH (+) ----| |---- (-) GND	1.0uF
C31P – C31N	C12	Connect to Capacitor (Max :25V): C31P (+) ----| |---- (-) C31N	1.0uF
C32P – C32N	C13 (Option)	Connect to Capacitor (Max :25V): C32P (+) ----| |---- (-) C32N	1.0uF
VGL	C14	Connect to Capacitor (Max :25V): VGL (-) ----| |---- (+) GND	1.0uF
VGL	D1	Connect to Schottky Diode (VR>= 30V) VGL(+) ----▶|----(-) VSN	VF<0.4V / 20mA @25℃,VR> =30V
VGL_REG	C15 (Option)	Connect to Capacitor (Max :25V): VGL_REG(-) ----| |---- (+) GND	1.0uF
VCOM	C16	Connect to Capacitor (Max :6V): VCOM(-) ----| |---- (+) GND	2.2uF

9.5、Maximum Layout Resistance

No.	Name	Maximum series Resistance	No.	Name	Maximum series Resistance
1 - 2	DUMMY	NA	263 - 264	PCLK	100
3	CGOUT_L1	10	265 - 266	DCX	100
4	CGOUT_L2	10	267 - 268	CSX	100
5	CGOUT_L3	10	269 - 270	SCL	100
6	CGOUT_L4	10	271 - 272	SDI	100
7	CGOUT_L5	10	273 - 274	SDO	100
8	CGOUT_L6	10	275 - 278	CABC_PWM_OUT	100
9	CGOUT_L7	10	279 - 284	TE	100
10	CGOUT_L8	10	285 - 290	TE_TOUCH	100
11	CGOUT_L9	10	291 - 294	RESX	100
12	CGOUT_L10	10	295 - 296	TEST0	100
13	CGOUT_L11	10	297 - 298	TEST1	100
14	CGOUT_L12	10	299 - 300	TEST2	100
15	CGOUT_L13	10	301 - 302	VSSD	5
16	CGOUT_L14	10	303 - 304	BS0	100
17	CGOUT_L15	10	305 - 306	IOVCC	5
18	CGOUT_L16	10	307 - 308	BS1	100
19	CGOUT_L17	10	309 - 310	VSSD	5
20	CGOUT_L18	10	311 - 312	DUMMY	NA
21	CGOUT_L19	10	313 - 314	IOVCC	5
22	CGOUT_L20	10	315 - 316	DUMMY	NA
23	CGOUT_L21	10	317 - 318	VSSD	5
24	CGOUT_L22	10	319 - 320	BS2	100
25 - 27	VCOM	10	321 - 322	IOVCC	5
28 - 37	VSSA	5	323 - 324	PCCS0	100
38 - 39	VTESTOUTN	100	325 - 326	VSSD	5
40	HS_VSS	5	327 - 328	PCCS1	100
41 - 46	HS_D0N	5	329 - 338	IOVCC	5
47 - 52	HS_D0P	5	339 - 348	VDDD	5
53	HS_VSS	5	349 - 358	VSSD	5
54 - 59	HS_D1N	5	359 - 366	VCSW2	20
60 - 65	HS_D1P	5	367 - 374	VCSW1	20
66	HS_VSS	5	375 - 380	VPP	10
67 - 72	HS_CKN	5	381 - 382	VTESTOUTP	100

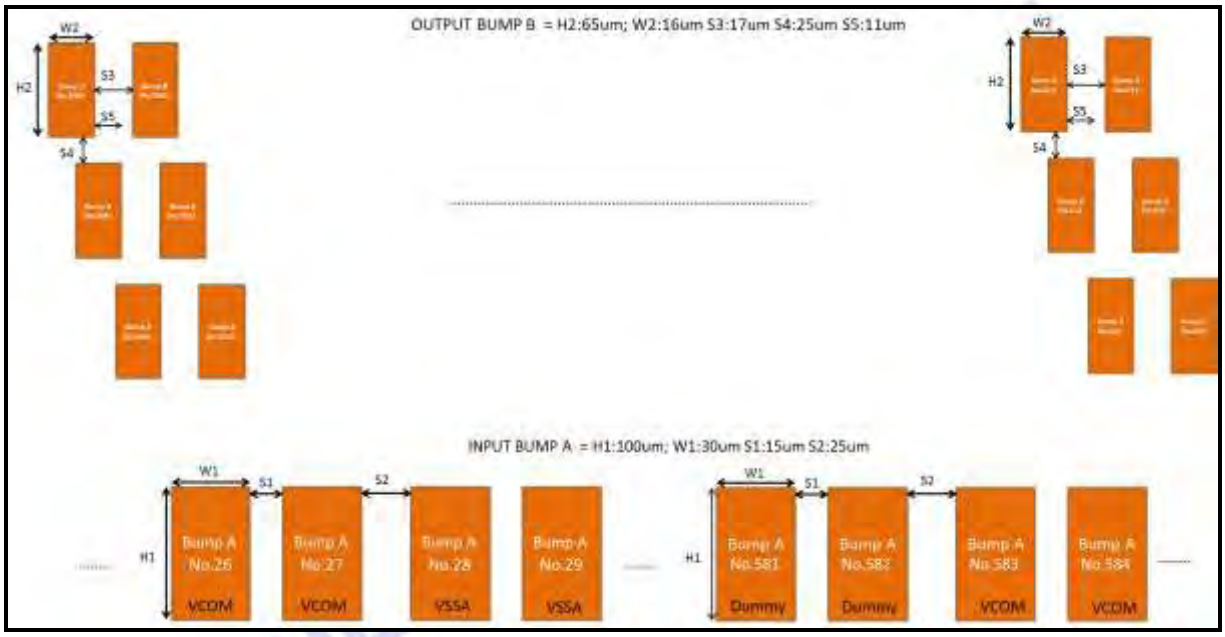
73 - 78	HS_CKP	5	383 - 387	VCI	5
79	HS_VSS	5	388 - 395	VSSD	5
80 - 85	HS_D2N	5	396 - 399	VSSAC	5
86 - 91	HS_D2P	5	400 - 406	VSSA	5
92	HS_VSS	5	407 - 409	VSPR	5
93 - 98	HS_D3N	5	410 - 412	VSNR	5
99 - 104	HS_D3P	5	413 - 415	VREF	20
105 - 116	HS_VSS	5	416 - 420	VSSD	5
117 - 128	HS_LDO	5	421 - 428	VCI	5
129 - 140	HS_VCC	5	429 - 433	VCL	5
141 - 155	IOVCC	5	434 - 440	C41P	5
156 - 170	VDDD	5	441 - 447	C41N	5
171 - 185	VSSD	5	448 - 454	C42P	5
186	TS7	100	455 - 461	C42N	5
187	TS6	100	462 - 468	VSP	5
188	TS5	100	469 - 475	VSN	5
189	TS4	100	476 - 482	C21P	5
190	TS3	100	483 - 489	C21N	5
191	TS2	100	490 - 496	C22P	5
192	TS1	100	497 - 503	C22N	5
193	TS0	100	504 - 509	VGH	5
194 - 199	VSP	5	510 - 515	VCI	5
200 - 201	DUMMY	NA	516 - 519	VSSA	5
202 - 203	TEST_OSC	100	520 - 523	VSSD	5
204 - 208	VSSD	5	524 - 530	C31P	5
209	DB_23	100	531 - 537	C31N	5
210	DB_22	100	538 - 544	C32P	5
211	DB_21	100	545 - 551	C32N	5
212	DB_20	100	552 - 557	VGL	5
213	DB_19	100	558 - 564	VCI	5
214	DB_18	100	565 - 571	VSSD	5
215	DB_17	100	572 - 577	VGL_REG	5
216	DB_16	100	578 - 581	DUMMY	NA
217	DB_15	100	582 - 584	VCOM	5
218	DB_14	100	585	CGOUT_R22	10
219	DB_13	100	586	CGOUT_R21	10
220	DB_12	100	587	CGOUT_R20	10
221	DB_11	100	588	CGOUT_R19	10
222	DB_10	100	589	CGOUT_R18	10
223	DB_9	100	590	CGOUT_R17	10

224	DB_8	100	591	CGOUT_R16	10
225	DB_7	100	592	CGOUT_R15	10
226	DB_6	100	593	CGOUT_R14	10
227	DB_5	100	594	CGOUT_R13	10
228	DB_4	100	595	CGOUT_R12	10
229	DB_3	100	596	CGOUT_R11	10
230	DB_2	100	597	CGOUT_R10	10
231	DB_1	100	598	CGOUT_R9	10
232	DB_0	100	599	CGOUT_R8	10
233 - 234	DUMMY	NA	600	CGOUT_R7	10
235 - 238	VSN	5	601	CGOUT_R6	10
239 - 240	BIST	100	602	CGOUT_R5	10
241 - 248	DUMMY	NA	603	CGOUT_R4	10
249 - 256	DUMMY	NA	604	CGOUT_R3	10
257 - 258	HSYNC	100	605	CGOUT_R2	10
259 - 260	VSYNC	100	606	CGOUT_R1	10
261 - 262	DE	100	607 - 608	DUMMY	NA

10、Pad Location Information

10.1、Chip Information

10.1.1 Pad Location

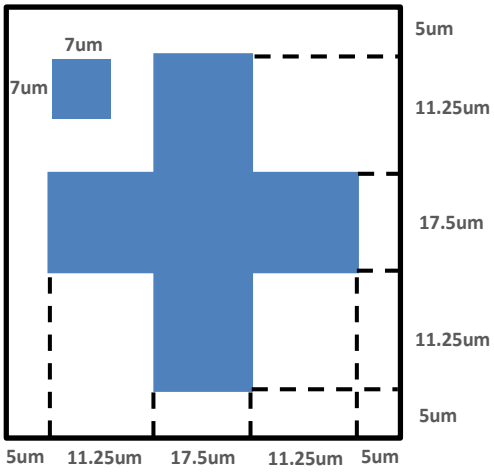


10.1.2 Chip Size

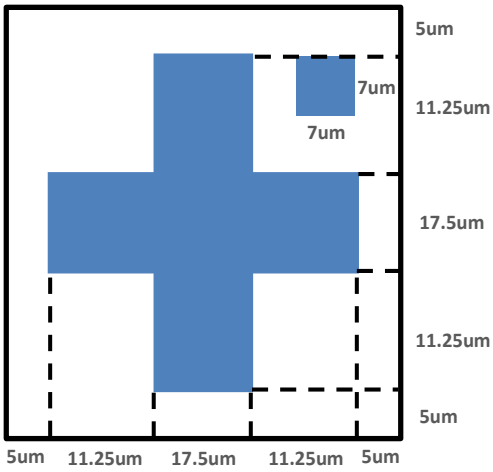
Chip size	X	Y	Unit
	27680	930	um

10.1.3 Alignment Mark

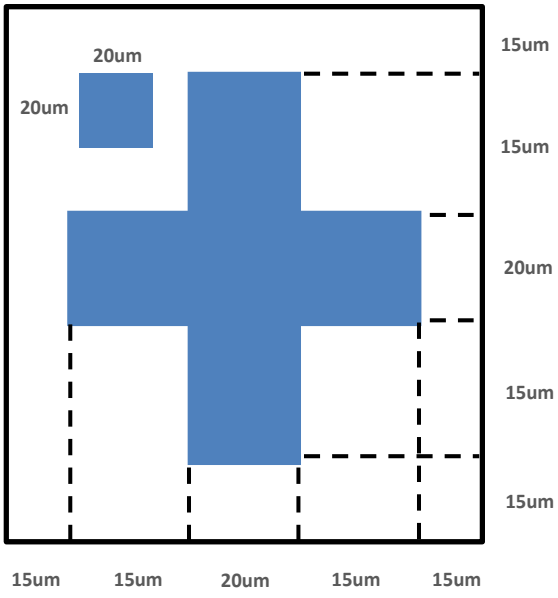
A1: Left (-13706,398.5)



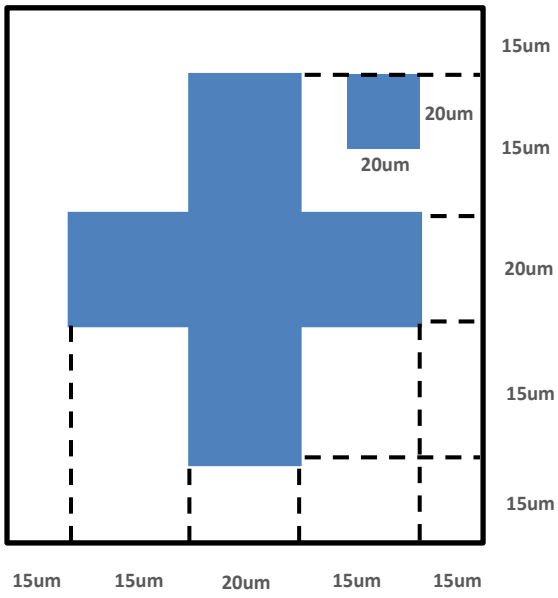
A2: Right (13706,398.5)



B1: Left (-13706,311.5)



B2: Right (13706,311.5)



10.2、Input Pad Location

PAD		Coordinate		PAD		Coordinate	
No.	Name	X-axis	Y-axis	No.	Name	X-axis	Y-axis
1	DUMMY	-13667.5	-348.5	305	IOVCC	22.5	-348.5
2	DUMMY	-13622.5	-348.5	306	IOVCC	67.5	-348.5
3	CGOUT_L1	-13577.5	-348.5	307	BS1	112.5	-348.5
4	CGOUT_L2	-13532.5	-348.5	308	BS1	157.5	-348.5
5	CGOUT_L3	-13487.5	-348.5	309	VSSD	202.5	-348.5
6	CGOUT_L4	-13442.5	-348.5	310	VSSD	247.5	-348.5
7	CGOUT_L5	-13397.5	-348.5	311	DUMMY	292.5	-348.5
8	CGOUT_L6	-13352.5	-348.5	312	DUMMY	337.5	-348.5
9	CGOUT_L7	-13307.5	-348.5	313	IOVCC	382.5	-348.5
10	CGOUT_L8	-13262.5	-348.5	314	IOVCC	427.5	-348.5
11	CGOUT_L9	-13217.5	-348.5	315	DUMMY	472.5	-348.5
12	CGOUT_L10	-13172.5	-348.5	316	DUMMY	517.5	-348.5
13	CGOUT_L11	-13127.5	-348.5	317	VSSD	562.5	-348.5
14	CGOUT_L12	-13082.5	-348.5	318	VSSD	607.5	-348.5
15	CGOUT_L13	-13037.5	-348.5	319	BS2	652.5	-348.5
16	CGOUT_L14	-12992.5	-348.5	320	BS2	697.5	-348.5
17	CGOUT_L15	-12947.5	-348.5	321	IOVCC	742.5	-348.5
18	CGOUT_L16	-12902.5	-348.5	322	IOVCC	787.5	-348.5
19	CGOUT_L17	-12857.5	-348.5	323	PCCS0	832.5	-348.5
20	CGOUT_L18	-12812.5	-348.5	324	PCCS0	877.5	-348.5
21	CGOUT_L19	-12767.5	-348.5	325	VSSD	922.5	-348.5
22	CGOUT_L20	-12722.5	-348.5	326	VSSD	967.5	-348.5
23	CGOUT_L21	-12677.5	-348.5	327	PCCS1	1012.5	-348.5
24	CGOUT_L22	-12632.5	-348.5	328	PCCS1	1057.5	-348.5
25	VCOM	-12587.5	-348.5	329	IOVCC	1102.5	-348.5
26	VCOM	-12542.5	-348.5	330	IOVCC	1147.5	-348.5
27	VCOM	-12497.5	-348.5	331	IOVCC	1192.5	-348.5
28	VSSA	-12442.5	-348.5	332	IOVCC	1237.5	-348.5
29	VSSA	-12397.5	-348.5	333	IOVCC	1282.5	-348.5
30	VSSA	-12352.5	-348.5	334	IOVCC	1327.5	-348.5
31	VSSA	-12307.5	-348.5	335	IOVCC	1372.5	-348.5
32	VSSA	-12262.5	-348.5	336	IOVCC	1417.5	-348.5
33	VSSA	-12217.5	-348.5	337	IOVCC	1462.5	-348.5
34	VSSA	-12172.5	-348.5	338	IOVCC	1507.5	-348.5

35	VSSA	-12127.5	-348.5	339	VDDD	1552.5	-348.5
36	VSSA	-12082.5	-348.5	340	VDDD	1597.5	-348.5
37	VSSA	-12037.5	-348.5	341	VDDD	1642.5	-348.5
38	VTESTOUTN	-11992.5	-348.5	342	VDDD	1687.5	-348.5
39	VTESTOUTN	-11947.5	-348.5	343	VDDD	1732.5	-348.5
40	HS_VSS	-11902.5	-348.5	344	VDDD	1777.5	-348.5
41	HS_D0N	-11857.5	-348.5	345	VDDD	1822.5	-348.5
42	HS_D0N	-11812.5	-348.5	346	VDDD	1867.5	-348.5
43	HS_D0N	-11767.5	-348.5	347	VDDD	1912.5	-348.5
44	HS_D0N	-11722.5	-348.5	348	VDDD	1957.5	-348.5
45	HS_D0N	-11677.5	-348.5	349	VSSD	2002.5	-348.5
46	HS_D0N	-11632.5	-348.5	350	VSSD	2047.5	-348.5
47	HS_D0P	-11587.5	-348.5	351	VSSD	2092.5	-348.5
48	HS_D0P	-11542.5	-348.5	352	VSSD	2137.5	-348.5
49	HS_D0P	-11497.5	-348.5	353	VSSD	2182.5	-348.5
50	HS_D0P	-11452.5	-348.5	354	VSSD	2227.5	-348.5
51	HS_D0P	-11407.5	-348.5	355	VSSD	2272.5	-348.5
52	HS_D0P	-11362.5	-348.5	356	VSSD	2317.5	-348.5
53	HS_VSS	-11317.5	-348.5	357	VSSD	2362.5	-348.5
54	HS_D1N	-11272.5	-348.5	358	VSSD	2407.5	-348.5
55	HS_D1N	-11227.5	-348.5	359	VCSW2	2452.5	-348.5
56	HS_D1N	-11182.5	-348.5	360	VCSW2	2497.5	-348.5
57	HS_D1N	-11137.5	-348.5	361	VCSW2	2542.5	-348.5
58	HS_D1N	-11092.5	-348.5	362	VCSW2	2587.5	-348.5
59	HS_D1N	-11047.5	-348.5	363	VCSW2	2632.5	-348.5
60	HS_D1P	-11002.5	-348.5	364	VCSW2	2677.5	-348.5
61	HS_D1P	-10957.5	-348.5	365	VCSW2	2722.5	-348.5
62	HS_D1P	-10912.5	-348.5	366	VCSW2	2767.5	-348.5
63	HS_D1P	-10867.5	-348.5	367	VCSW1	2812.5	-348.5
64	HS_D1P	-10822.5	-348.5	368	VCSW1	2857.5	-348.5
65	HS_D1P	-10777.5	-348.5	369	VCSW1	2902.5	-348.5
66	HS_VSS	-10732.5	-348.5	370	VCSW1	2947.5	-348.5
67	HS_CKN	-10687.5	-348.5	371	VCSW1	2992.5	-348.5
68	HS_CKN	-10642.5	-348.5	372	VCSW1	3037.5	-348.5
69	HS_CKN	-10597.5	-348.5	373	VCSW1	3082.5	-348.5
70	HS_CKN	-10552.5	-348.5	374	VCSW1	3127.5	-348.5
71	HS_CKN	-10507.5	-348.5	375	VPP	3172.5	-348.5
72	HS_CKN	-10462.5	-348.5	376	VPP	3217.5	-348.5
73	HS_CKP	-10417.5	-348.5	377	VPP	3262.5	-348.5
74	HS_CKP	-10372.5	-348.5	378	VPP	3307.5	-348.5

75	HS_CKP	-10327.5	-348.5	379	VPP	3352.5	-348.5
76	HS_CKP	-10282.5	-348.5	380	VPP	3397.5	-348.5
77	HS_CKP	-10237.5	-348.5	381	VTESTOUTP	3442.5	-348.5
78	HS_CKP	-10192.5	-348.5	382	VTESTOUTP	3487.5	-348.5
79	HS_VSS	-10147.5	-348.5	383	VCI	3532.5	-348.5
80	HS_D2N	-10102.5	-348.5	384	VCI	3577.5	-348.5
81	HS_D2N	-10057.5	-348.5	385	VCI	3622.5	-348.5
82	HS_D2N	-10012.5	-348.5	386	VCI	3667.5	-348.5
83	HS_D2N	-9967.5	-348.5	387	VCI	3712.5	-348.5
84	HS_D2N	-9922.5	-348.5	388	VSSD	3757.5	-348.5
85	HS_D2N	-9877.5	-348.5	389	VSSD	3802.5	-348.5
86	HS_D2P	-9832.5	-348.5	390	VSSD	3847.5	-348.5
87	HS_D2P	-9787.5	-348.5	391	VSSD	3892.5	-348.5
88	HS_D2P	-9742.5	-348.5	392	VSSD	3937.5	-348.5
89	HS_D2P	-9697.5	-348.5	393	VSSD	3982.5	-348.5
90	HS_D2P	-9652.5	-348.5	394	VSSD	4027.5	-348.5
91	HS_D2P	-9607.5	-348.5	395	VSSD	4072.5	-348.5
92	HS_VSS	-9562.5	-348.5	396	VSSAC	4117.5	-348.5
93	HS_D3N	-9517.5	-348.5	397	VSSAC	4162.5	-348.5
94	HS_D3N	-9472.5	-348.5	398	VSSAC	4207.5	-348.5
95	HS_D3N	-9427.5	-348.5	399	VSSAC	4252.5	-348.5
96	HS_D3N	-9382.5	-348.5	400	VSSA	4297.5	-348.5
97	HS_D3N	-9337.5	-348.5	401	VSSA	4342.5	-348.5
98	HS_D3N	-9292.5	-348.5	402	VSSA	4387.5	-348.5
99	HS_D3P	-9247.5	-348.5	403	VSSA	4432.5	-348.5
100	HS_D3P	-9202.5	-348.5	404	VSSA	4477.5	-348.5
101	HS_D3P	-9157.5	-348.5	405	VSSA	4522.5	-348.5
102	HS_D3P	-9112.5	-348.5	406	VSSA	4567.5	-348.5
103	HS_D3P	-9067.5	-348.5	407	VSPR	4612.5	-348.5
104	HS_D3P	-9022.5	-348.5	408	VSPR	4657.5	-348.5
105	HS_VSS	-8977.5	-348.5	409	VSPR	4702.5	-348.5
106	HS_VSS	-8932.5	-348.5	410	VSNR	4747.5	-348.5
107	HS_VSS	-8887.5	-348.5	411	VSNR	4792.5	-348.5
108	HS_VSS	-8842.5	-348.5	412	VSNR	4837.5	-348.5
109	HS_VSS	-8797.5	-348.5	413	VREF	4882.5	-348.5
110	HS_VSS	-8752.5	-348.5	414	VREF	4927.5	-348.5
111	HS_VSS	-8707.5	-348.5	415	VREF	4972.5	-348.5
112	HS_VSS	-8662.5	-348.5	416	VSSD	5017.5	-348.5
113	HS_VSS	-8617.5	-348.5	417	VSSD	5062.5	-348.5
114	HS_VSS	-8572.5	-348.5	418	VSSD	5107.5	-348.5

115	HS_VSS	-8527.5	-348.5	419	VSSD	5152.5	-348.5
116	HS_VSS	-8482.5	-348.5	420	VSSD	5197.5	-348.5
117	HS_LDO	-8437.5	-348.5	421	VCI	5242.5	-348.5
118	HS_LDO	-8392.5	-348.5	422	VCI	5287.5	-348.5
119	HS_LDO	-8347.5	-348.5	423	VCI	5332.5	-348.5
120	HS_LDO	-8302.5	-348.5	424	VCI	5377.5	-348.5
121	HS_LDO	-8257.5	-348.5	425	VCI	5422.5	-348.5
122	HS_LDO	-8212.5	-348.5	426	VCI	5467.5	-348.5
123	HS_LDO	-8167.5	-348.5	427	VCI	5512.5	-348.5
124	HS_LDO	-8122.5	-348.5	428	VCI	5557.5	-348.5
125	HS_LDO	-8077.5	-348.5	429	VCL	5602.5	-348.5
126	HS_LDO	-8032.5	-348.5	430	VCL	5647.5	-348.5
127	HS_LDO	-7987.5	-348.5	431	VCL	5692.5	-348.5
128	HS_LDO	-7942.5	-348.5	432	VCL	5737.5	-348.5
129	HS_VCC	-7897.5	-348.5	433	VCL	5782.5	-348.5
130	HS_VCC	-7852.5	-348.5	434	C41P	5827.5	-348.5
131	HS_VCC	-7807.5	-348.5	435	C41P	5872.5	-348.5
132	HS_VCC	-7762.5	-348.5	436	C41P	5917.5	-348.5
133	HS_VCC	-7717.5	-348.5	437	C41P	5962.5	-348.5
134	HS_VCC	-7672.5	-348.5	438	C41P	6007.5	-348.5
135	HS_VCC	-7627.5	-348.5	439	C41P	6052.5	-348.5
136	HS_VCC	-7582.5	-348.5	440	C41P	6097.5	-348.5
137	HS_VCC	-7537.5	-348.5	441	C41N	6142.5	-348.5
138	HS_VCC	-7492.5	-348.5	442	C41N	6187.5	-348.5
139	HS_VCC	-7447.5	-348.5	443	C41N	6232.5	-348.5
140	HS_VCC	-7402.5	-348.5	444	C41N	6277.5	-348.5
141	IOVCC	-7357.5	-348.5	445	C41N	6322.5	-348.5
142	IOVCC	-7312.5	-348.5	446	C41N	6367.5	-348.5
143	IOVCC	-7267.5	-348.5	447	C41N	6412.5	-348.5
144	IOVCC	-7222.5	-348.5	448	C42P	6457.5	-348.5
145	IOVCC	-7177.5	-348.5	449	C42P	6502.5	-348.5
146	IOVCC	-7132.5	-348.5	450	C42P	6547.5	-348.5
147	IOVCC	-7087.5	-348.5	451	C42P	6592.5	-348.5
148	IOVCC	-7042.5	-348.5	452	C42P	6637.5	-348.5
149	IOVCC	-6997.5	-348.5	453	C42P	6682.5	-348.5
150	IOVCC	-6952.5	-348.5	454	C42P	6727.5	-348.5
151	IOVCC	-6907.5	-348.5	455	C42N	6772.5	-348.5
152	IOVCC	-6862.5	-348.5	456	C42N	6817.5	-348.5
153	IOVCC	-6817.5	-348.5	457	C42N	6862.5	-348.5
154	IOVCC	-6772.5	-348.5	458	C42N	6907.5	-348.5

155	IOVCC	-6727.5	-348.5	459	C42N	6952.5	-348.5
156	VDDD	-6682.5	-348.5	460	C42N	6997.5	-348.5
157	VDDD	-6637.5	-348.5	461	C42N	7042.5	-348.5
158	VDDD	-6592.5	-348.5	462	VSP	7087.5	-348.5
159	VDDD	-6547.5	-348.5	463	VSP	7132.5	-348.5
160	VDDD	-6502.5	-348.5	464	VSP	7177.5	-348.5
161	VDDD	-6457.5	-348.5	465	VSP	7222.5	-348.5
162	VDDD	-6412.5	-348.5	466	VSP	7267.5	-348.5
163	VDDD	-6367.5	-348.5	467	VSP	7312.5	-348.5
164	VDDD	-6322.5	-348.5	468	VSP	7357.5	-348.5
165	VDDD	-6277.5	-348.5	469	VSN	7402.5	-348.5
166	VDDD	-6232.5	-348.5	470	VSN	7447.5	-348.5
167	VDDD	-6187.5	-348.5	471	VSN	7492.5	-348.5
168	VDDD	-6142.5	-348.5	472	VSN	7537.5	-348.5
169	VDDD	-6097.5	-348.5	473	VSN	7582.5	-348.5
170	VDDD	-6052.5	-348.5	474	VSN	7627.5	-348.5
171	VSSD	-6007.5	-348.5	475	VSN	7672.5	-348.5
172	VSSD	-5962.5	-348.5	476	C21P	7717.5	-348.5
173	VSSD	-5917.5	-348.5	477	C21P	7762.5	-348.5
174	VSSD	-5872.5	-348.5	478	C21P	7807.5	-348.5
175	VSSD	-5827.5	-348.5	479	C21P	7852.5	-348.5
176	VSSD	-5782.5	-348.5	480	C21P	7897.5	-348.5
177	VSSD	-5737.5	-348.5	481	C21P	7942.5	-348.5
178	VSSD	-5692.5	-348.5	482	C21P	7987.5	-348.5
179	VSSD	-5647.5	-348.5	483	C21N	8032.5	-348.5
180	VSSD	-5602.5	-348.5	484	C21N	8077.5	-348.5
181	VSSD	-5557.5	-348.5	485	C21N	8122.5	-348.5
182	VSSD	-5512.5	-348.5	486	C21N	8167.5	-348.5
183	VSSD	-5467.5	-348.5	487	C21N	8212.5	-348.5
184	VSSD	-5422.5	-348.5	488	C21N	8257.5	-348.5
185	VSSD	-5377.5	-348.5	489	C21N	8302.5	-348.5
186	TS7	-5332.5	-348.5	490	C22P	8347.5	-348.5
187	TS6	-5287.5	-348.5	491	C22P	8392.5	-348.5
188	TS5	-5242.5	-348.5	492	C22P	8437.5	-348.5
189	TS4	-5197.5	-348.5	493	C22P	8482.5	-348.5
190	TS3	-5152.5	-348.5	494	C22P	8527.5	-348.5
191	TS2	-5107.5	-348.5	495	C22P	8572.5	-348.5
192	TS1	-5062.5	-348.5	496	C22P	8617.5	-348.5
193	TS0	-5017.5	-348.5	497	C22N	8662.5	-348.5
194	VSP	-4972.5	-348.5	498	C22N	8707.5	-348.5

195	VSP	-4927.5	-348.5	499	C22N	8752.5	-348.5
196	VSP	-4882.5	-348.5	500	C22N	8797.5	-348.5
197	VSP	-4837.5	-348.5	501	C22N	8842.5	-348.5
198	VSP	-4792.5	-348.5	502	C22N	8887.5	-348.5
199	VSP	-4747.5	-348.5	503	C22N	8932.5	-348.5
200	DUMMY	-4702.5	-348.5	504	VGH	8977.5	-348.5
201	DUMMY	-4657.5	-348.5	505	VGH	9022.5	-348.5
202	TEST_OSC	-4612.5	-348.5	506	VGH	9067.5	-348.5
203	TEST_OSC	-4567.5	-348.5	507	VGH	9112.5	-348.5
204	VSSD	-4522.5	-348.5	508	VGH	9157.5	-348.5
205	VSSD	-4477.5	-348.5	509	VGH	9202.5	-348.5
206	VSSD	-4432.5	-348.5	510	VCI	9247.5	-348.5
207	VSSD	-4387.5	-348.5	511	VCI	9292.5	-348.5
208	VSSD	-4342.5	-348.5	512	VCI	9337.5	-348.5
209	DB_23	-4297.5	-348.5	513	VCI	9382.5	-348.5
210	DB_22	-4252.5	-348.5	514	VCI	9427.5	-348.5
211	DB_21	-4207.5	-348.5	515	VCI	9472.5	-348.5
212	DB_20	-4162.5	-348.5	516	VSSA	9517.5	-348.5
213	DB_19	-4117.5	-348.5	517	VSSA	9562.5	-348.5
214	DB_18	-4072.5	-348.5	518	VSSA	9607.5	-348.5
215	DB_17	-4027.5	-348.5	519	VSSA	9652.5	-348.5
216	DB_16	-3982.5	-348.5	520	VSSD	9697.5	-348.5
217	DB_15	-3937.5	-348.5	521	VSSD	9742.5	-348.5
218	DB_14	-3892.5	-348.5	522	VSSD	9787.5	-348.5
219	DB_13	-3847.5	-348.5	523	VSSD	9832.5	-348.5
220	DB_12	-3802.5	-348.5	524	C31P	9877.5	-348.5
221	DB_11	-3757.5	-348.5	525	C31P	9922.5	-348.5
222	DB_10	-3712.5	-348.5	526	C31P	9967.5	-348.5
223	DB_9	-3667.5	-348.5	527	C31P	10012.5	-348.5
224	DB_8	-3622.5	-348.5	528	C31P	10057.5	-348.5
225	DB_7	-3577.5	-348.5	529	C31P	10102.5	-348.5
226	DB_6	-3532.5	-348.5	530	C31P	10147.5	-348.5
227	DB_5	-3487.5	-348.5	531	C31N	10192.5	-348.5
228	DB_4	-3442.5	-348.5	532	C31N	10237.5	-348.5
229	DB_3	-3397.5	-348.5	533	C31N	10282.5	-348.5
230	DB_2	-3352.5	-348.5	534	C31N	10327.5	-348.5
231	DB_1	-3307.5	-348.5	535	C31N	10372.5	-348.5
232	DB_0	-3262.5	-348.5	536	C31N	10417.5	-348.5
233	DUMMY	-3217.5	-348.5	537	C31N	10462.5	-348.5
234	DUMMY	-3172.5	-348.5	538	C32P	10507.5	-348.5

235	VSN	-3127.5	-348.5	539	C32P	10552.5	-348.5
236	VSN	-3082.5	-348.5	540	C32P	10597.5	-348.5
237	VSN	-3037.5	-348.5	541	C32P	10642.5	-348.5
238	VSN	-2992.5	-348.5	542	C32P	10687.5	-348.5
239	BIST	-2947.5	-348.5	543	C32P	10732.5	-348.5
240	BIST	-2902.5	-348.5	544	C32P	10777.5	-348.5
241	DUMMY	-2857.5	-348.5	545	C32N	10822.5	-348.5
242	DUMMY	-2812.5	-348.5	546	C32N	10867.5	-348.5
243	DUMMY	-2767.5	-348.5	547	C32N	10912.5	-348.5
244	DUMMY	-2722.5	-348.5	548	C32N	10957.5	-348.5
245	DUMMY	-2677.5	-348.5	549	C32N	11002.5	-348.5
246	DUMMY	-2632.5	-348.5	550	C32N	11047.5	-348.5
247	DUMMY	-2587.5	-348.5	551	C32N	11092.5	-348.5
248	DUMMY	-2542.5	-348.5	552	VGL	11137.5	-348.5
249	DUMMY	-2497.5	-348.5	553	VGL	11182.5	-348.5
250	DUMMY	-2452.5	-348.5	554	VGL	11227.5	-348.5
251	DUMMY	-2407.5	-348.5	555	VGL	11272.5	-348.5
252	DUMMY	-2362.5	-348.5	556	VGL	11317.5	-348.5
253	DUMMY	-2317.5	-348.5	557	VGL	11362.5	-348.5
254	DUMMY	-2272.5	-348.5	558	VCI	11407.5	-348.5
255	DUMMY	-2227.5	-348.5	559	VCI	11452.5	-348.5
256	DUMMY	-2182.5	-348.5	560	VCI	11497.5	-348.5
257	HSYNC	-2137.5	-348.5	561	VCI	11542.5	-348.5
258	HSYNC	-2092.5	-348.5	562	VCI	11587.5	-348.5
259	VSYNC	-2047.5	-348.5	563	VCI	11632.5	-348.5
260	VSYNC	-2002.5	-348.5	564	VCI	11677.5	-348.5
261	DE	-1957.5	-348.5	565	VSSD	11722.5	-348.5
262	DE	-1912.5	-348.5	566	VSSD	11767.5	-348.5
263	PCLK	-1867.5	-348.5	567	VSSD	11812.5	-348.5
264	PCLK	-1822.5	-348.5	568	VSSD	11857.5	-348.5
265	DCX	-1777.5	-348.5	569	VSSD	11902.5	-348.5
266	DCX	-1732.5	-348.5	570	VSSD	11947.5	-348.5
267	CSX	-1687.5	-348.5	571	VSSD	11992.5	-348.5
268	CSX	-1642.5	-348.5	572	VGL_REG	12037.5	-348.5
269	SCL	-1597.5	-348.5	573	VGL_REG	12082.5	-348.5
270	SCL	-1552.5	-348.5	574	VGL_REG	12127.5	-348.5
271	SDI	-1507.5	-348.5	575	VGL_REG	12172.5	-348.5
272	SDI	-1462.5	-348.5	576	VGL_REG	12217.5	-348.5
273	SDO	-1417.5	-348.5	577	VGL_REG	12262.5	-348.5
274	SDO	-1372.5	-348.5	578	DUMMY	12307.5	-348.5

275	CABC_PWM_OUT	-1327.5	-348.5	579	DUMMY	12352.5	-348.5
276	CABC_PWM_OUT	-1282.5	-348.5	580	DUMMY	12397.5	-348.5
277	CABC_PWM_OUT	-1237.5	-348.5	581	DUMMY	12442.5	-348.5
278	CABC_PWM_OUT	-1192.5	-348.5	582	VCOM	12497.5	-348.5
279	TE	-1147.5	-348.5	583	VCOM	12542.5	-348.5
280	TE	-1102.5	-348.5	584	VCOM	12587.5	-348.5
281	TE	-1057.5	-348.5	585	CGOUT_R22	12632.5	-348.5
282	TE	-1012.5	-348.5	586	CGOUT_R21	12677.5	-348.5
283	TE	-967.5	-348.5	587	CGOUT_R20	12722.5	-348.5
284	TE	-922.5	-348.5	588	CGOUT_R19	12767.5	-348.5
285	TE_TOUCH	-877.5	-348.5	589	CGOUT_R18	12812.5	-348.5
286	TE_TOUCH	-832.5	-348.5	590	CGOUT_R17	12857.5	-348.5
287	TE_TOUCH	-787.5	-348.5	591	CGOUT_R16	12902.5	-348.5
288	TE_TOUCH	-742.5	-348.5	592	CGOUT_R15	12947.5	-348.5
289	TE_TOUCH	-697.5	-348.5	593	CGOUT_R14	12992.5	-348.5
290	TE_TOUCH	-652.5	-348.5	594	CGOUT_R13	13037.5	-348.5
291	RESX	-607.5	-348.5	595	CGOUT_R12	13082.5	-348.5
292	RESX	-562.5	-348.5	596	CGOUT_R11	13127.5	-348.5
293	RESX	-517.5	-348.5	597	CGOUT_R10	13172.5	-348.5
294	RESX	-472.5	-348.5	598	CGOUT_R9	13217.5	-348.5
295	TEST0	-427.5	-348.5	599	CGOUT_R8	13262.5	-348.5
296	TEST0	-382.5	-348.5	600	CGOUT_R7	13307.5	-348.5
297	TEST1	-337.5	-348.5	601	CGOUT_R6	13352.5	-348.5
298	TEST1	-292.5	-348.5	602	CGOUT_R5	13397.5	-348.5
299	TEST2	-247.5	-348.5	603	CGOUT_R4	13442.5	-348.5
300	TEST2	-202.5	-348.5	604	CGOUT_R3	13487.5	-348.5
301	VSSD	-157.5	-348.5	605	CGOUT_R2	13532.5	-348.5
302	VSSD	-112.5	-348.5	606	CGOUT_R1	13577.5	-348.5
303	BS0	-67.5	-348.5	607	DUMMY	13622.5	-348.5
304	BS0	-22.5	-348.5	608	DUMMY	13667.5	-348.5

10.3、Output Pad Location

PAD		Coordinate		PAD		Coordinate	
No.	Name	X-axis	Y-axis	No.	Name	X-axis	Y-axis
609	DUMMY	13623.5	211	1848	DUMMY	-5.5	211
610	DUMMY	13612.5	301	1849	DUMMY	-16.5	301
611	DUMMY	13601.5	391	1850	DUMMY	-27.5	391
612	DUMMY	13590.5	211	1851	DUMMY	-38.5	211
613	DUMMY	13579.5	301	1852	DUMMY	-49.5	301
614	DUMMY	13568.5	391	1853	DUMMY	-60.5	391
615	DUMMY	13557.5	211	1854	DUMMY	-71.5	211
616	DUMMY	13546.5	301	1855	DUMMY	-82.5	301
617	SR1	13535.5	391	1856	DUMMY	-93.5	391
618	S2400	13524.5	211	1857	DUMMY	-104.5	211
619	S2399	13513.5	301	1858	DUMMY	-115.5	301
620	S2398	13502.5	391	1859	DUMMY	-126.5	391
621	S2397	13491.5	211	1860	S1200	-137.5	211
622	S2396	13480.5	301	1861	S1199	-148.5	301
623	S2395	13469.5	391	1862	S1198	-159.5	391
624	S2394	13458.5	211	1863	S1197	-170.5	211
625	S2393	13447.5	301	1864	S1196	-181.5	301
626	S2392	13436.5	391	1865	S1195	-192.5	391
627	S2391	13425.5	211	1866	S1194	-203.5	211
628	S2390	13414.5	301	1867	S1193	-214.5	301
629	S2389	13403.5	391	1868	S1192	-225.5	391
630	S2388	13392.5	211	1869	S1191	-236.5	211
631	S2387	13381.5	301	1870	S1190	-247.5	301
632	S2386	13370.5	391	1871	S1189	-258.5	391
633	S2385	13359.5	211	1872	S1188	-269.5	211
634	S2384	13348.5	301	1873	S1187	-280.5	301
635	S2383	13337.5	391	1874	S1186	-291.5	391
636	S2382	13326.5	211	1875	S1185	-302.5	211
637	S2381	13315.5	301	1876	S1184	-313.5	301
638	S2380	13304.5	391	1877	S1183	-324.5	391
639	S2379	13293.5	211	1878	S1182	-335.5	211
640	S2378	13282.5	301	1879	S1181	-346.5	301
641	S2377	13271.5	391	1880	S1180	-357.5	391
642	S2376	13260.5	211	1881	S1179	-368.5	211
643	S2375	13249.5	301	1882	S1178	-379.5	301

644	S2374	13238.5	391	1883	S1177	-390.5	391
645	S2373	13227.5	211	1884	S1176	-401.5	211
646	S2372	13216.5	301	1885	S1175	-412.5	301
647	S2371	13205.5	391	1886	S1174	-423.5	391
648	S2370	13194.5	211	1887	S1173	-434.5	211
649	S2369	13183.5	301	1888	S1172	-445.5	301
650	S2368	13172.5	391	1889	S1171	-456.5	391
651	S2367	13161.5	211	1890	S1170	-467.5	211
652	S2366	13150.5	301	1891	S1169	-478.5	301
653	S2365	13139.5	391	1892	S1168	-489.5	391
654	S2364	13128.5	211	1893	S1167	-500.5	211
655	S2363	13117.5	301	1894	S1166	-511.5	301
656	S2362	13106.5	391	1895	S1165	-522.5	391
657	S2361	13095.5	211	1896	S1164	-533.5	211
658	S2360	13084.5	301	1897	S1163	-544.5	301
659	S2359	13073.5	391	1898	S1162	-555.5	391
660	S2358	13062.5	211	1899	S1161	-566.5	211
661	S2357	13051.5	301	1900	S1160	-577.5	301
662	S2356	13040.5	391	1901	S1159	-588.5	391
663	S2355	13029.5	211	1902	S1158	-599.5	211
664	S2354	13018.5	301	1903	S1157	-610.5	301
665	S2353	13007.5	391	1904	S1156	-621.5	391
666	S2352	12996.5	211	1905	S1155	-632.5	211
667	S2351	12985.5	301	1906	S1154	-643.5	301
668	S2350	12974.5	391	1907	S1153	-654.5	391
669	S2349	12963.5	211	1908	S1152	-665.5	211
670	S2348	12952.5	301	1909	S1151	-676.5	301
671	S2347	12941.5	391	1910	S1150	-687.5	391
672	S2346	12930.5	211	1911	S1149	-698.5	211
673	S2345	12919.5	301	1912	S1148	-709.5	301
674	S2344	12908.5	391	1913	S1147	-720.5	391
675	S2343	12897.5	211	1914	S1146	-731.5	211
676	S2342	12886.5	301	1915	S1145	-742.5	301
677	S2341	12875.5	391	1916	S1144	-753.5	391
678	S2340	12864.5	211	1917	S1143	-764.5	211
679	S2339	12853.5	301	1918	S1142	-775.5	301
680	S2338	12842.5	391	1919	S1141	-786.5	391
681	S2337	12831.5	211	1920	S1140	-797.5	211
682	S2336	12820.5	301	1921	S1139	-808.5	301
683	S2335	12809.5	391	1922	S1138	-819.5	391

684	S2334	12798.5	211	1923	S1137	-830.5	211
685	S2333	12787.5	301	1924	S1136	-841.5	301
686	S2332	12776.5	391	1925	S1135	-852.5	391
687	S2331	12765.5	211	1926	S1134	-863.5	211
688	S2330	12754.5	301	1927	S1133	-874.5	301
689	S2329	12743.5	391	1928	S1132	-885.5	391
690	S2328	12732.5	211	1929	S1131	-896.5	211
691	S2327	12721.5	301	1930	S1130	-907.5	301
692	S2326	12710.5	391	1931	S1129	-918.5	391
693	S2325	12699.5	211	1932	S1128	-929.5	211
694	S2324	12688.5	301	1933	S1127	-940.5	301
695	S2323	12677.5	391	1934	S1126	-951.5	391
696	S2322	12666.5	211	1935	S1125	-962.5	211
697	S2321	12655.5	301	1936	S1124	-973.5	301
698	S2320	12644.5	391	1937	S1123	-984.5	391
699	S2319	12633.5	211	1938	S1122	-995.5	211
700	S2318	12622.5	301	1939	S1121	-1006.5	301
701	S2317	12611.5	391	1940	S1120	-1017.5	391
702	S2316	12600.5	211	1941	S1119	-1028.5	211
703	S2315	12589.5	301	1942	S1118	-1039.5	301
704	S2314	12578.5	391	1943	S1117	-1050.5	391
705	S2313	12567.5	211	1944	S1116	-1061.5	211
706	S2312	12556.5	301	1945	S1115	-1072.5	301
707	S2311	12545.5	391	1946	S1114	-1083.5	391
708	S2310	12534.5	211	1947	S1113	-1094.5	211
709	S2309	12523.5	301	1948	S1112	-1105.5	301
710	S2308	12512.5	391	1949	S1111	-1116.5	391
711	S2307	12501.5	211	1950	S1110	-1127.5	211
712	S2306	12490.5	301	1951	S1109	-1138.5	301
713	S2305	12479.5	391	1952	S1108	-1149.5	391
714	S2304	12468.5	211	1953	S1107	-1160.5	211
715	S2303	12457.5	301	1954	S1106	-1171.5	301
716	S2302	12446.5	391	1955	S1105	-1182.5	391
717	S2301	12435.5	211	1956	S1104	-1193.5	211
718	S2300	12424.5	301	1957	S1103	-1204.5	301
719	S2299	12413.5	391	1958	S1102	-1215.5	391
720	S2298	12402.5	211	1959	S1101	-1226.5	211
721	S2297	12391.5	301	1960	S1100	-1237.5	301
722	S2296	12380.5	391	1961	S1099	-1248.5	391
723	S2295	12369.5	211	1962	S1098	-1259.5	211

724	S2294	12358.5	301	1963	S1097	-1270.5	301
725	S2293	12347.5	391	1964	S1096	-1281.5	391
726	S2292	12336.5	211	1965	S1095	-1292.5	211
727	S2291	12325.5	301	1966	S1094	-1303.5	301
728	S2290	12314.5	391	1967	S1093	-1314.5	391
729	S2289	12303.5	211	1968	S1092	-1325.5	211
730	S2288	12292.5	301	1969	S1091	-1336.5	301
731	S2287	12281.5	391	1970	S1090	-1347.5	391
732	S2286	12270.5	211	1971	S1089	-1358.5	211
733	S2285	12259.5	301	1972	S1088	-1369.5	301
734	S2284	12248.5	391	1973	S1087	-1380.5	391
735	S2283	12237.5	211	1974	S1086	-1391.5	211
736	S2282	12226.5	301	1975	S1085	-1402.5	301
737	S2281	12215.5	391	1976	S1084	-1413.5	391
738	S2280	12204.5	211	1977	S1083	-1424.5	211
739	S2279	12193.5	301	1978	S1082	-1435.5	301
740	S2278	12182.5	391	1979	S1081	-1446.5	391
741	S2277	12171.5	211	1980	S1080	-1457.5	211
742	S2276	12160.5	301	1981	S1079	-1468.5	301
743	S2275	12149.5	391	1982	S1078	-1479.5	391
744	S2274	12138.5	211	1983	S1077	-1490.5	211
745	S2273	12127.5	301	1984	S1076	-1501.5	301
746	S2272	12116.5	391	1985	S1075	-1512.5	391
747	S2271	12105.5	211	1986	S1074	-1523.5	211
748	S2270	12094.5	301	1987	S1073	-1534.5	301
749	S2269	12083.5	391	1988	S1072	-1545.5	391
750	S2268	12072.5	211	1989	S1071	-1556.5	211
751	S2267	12061.5	301	1990	S1070	-1567.5	301
752	S2266	12050.5	391	1991	S1069	-1578.5	391
753	S2265	12039.5	211	1992	S1068	-1589.5	211
754	S2264	12028.5	301	1993	S1067	-1600.5	301
755	S2263	12017.5	391	1994	S1066	-1611.5	391
756	S2262	12006.5	211	1995	S1065	-1622.5	211
757	S2261	11995.5	301	1996	S1064	-1633.5	301
758	S2260	11984.5	391	1997	S1063	-1644.5	391
759	S2259	11973.5	211	1998	S1062	-1655.5	211
760	S2258	11962.5	301	1999	S1061	-1666.5	301
761	S2257	11951.5	391	2000	S1060	-1677.5	391
762	S2256	11940.5	211	2001	S1059	-1688.5	211
763	S2255	11929.5	301	2002	S1058	-1699.5	301

764	S2254	11918.5	391	2003	S1057	-1710.5	391
765	S2253	11907.5	211	2004	S1056	-1721.5	211
766	S2252	11896.5	301	2005	S1055	-1732.5	301
767	S2251	11885.5	391	2006	S1054	-1743.5	391
768	S2250	11874.5	211	2007	S1053	-1754.5	211
769	S2249	11863.5	301	2008	S1052	-1765.5	301
770	S2248	11852.5	391	2009	S1051	-1776.5	391
771	S2247	11841.5	211	2010	S1050	-1787.5	211
772	S2246	11830.5	301	2011	S1049	-1798.5	301
773	S2245	11819.5	391	2012	S1048	-1809.5	391
774	S2244	11808.5	211	2013	S1047	-1820.5	211
775	S2243	11797.5	301	2014	S1046	-1831.5	301
776	S2242	11786.5	391	2015	S1045	-1842.5	391
777	S2241	11775.5	211	2016	S1044	-1853.5	211
778	S2240	11764.5	301	2017	S1043	-1864.5	301
779	S2239	11753.5	391	2018	S1042	-1875.5	391
780	S2238	11742.5	211	2019	S1041	-1886.5	211
781	S2237	11731.5	301	2020	S1040	-1897.5	301
782	S2236	11720.5	391	2021	S1039	-1908.5	391
783	S2235	11709.5	211	2022	S1038	-1919.5	211
784	S2234	11698.5	301	2023	S1037	-1930.5	301
785	S2233	11687.5	391	2024	S1036	-1941.5	391
786	S2232	11676.5	211	2025	S1035	-1952.5	211
787	S2231	11665.5	301	2026	S1034	-1963.5	301
788	S2230	11654.5	391	2027	S1033	-1974.5	391
789	S2229	11643.5	211	2028	S1032	-1985.5	211
790	S2228	11632.5	301	2029	S1031	-1996.5	301
791	S2227	11621.5	391	2030	S1030	-2007.5	391
792	S2226	11610.5	211	2031	S1029	-2018.5	211
793	S2225	11599.5	301	2032	S1028	-2029.5	301
794	S2224	11588.5	391	2033	S1027	-2040.5	391
795	S2223	11577.5	211	2034	S1026	-2051.5	211
796	S2222	11566.5	301	2035	S1025	-2062.5	301
797	S2221	11555.5	391	2036	S1024	-2073.5	391
798	S2220	11544.5	211	2037	S1023	-2084.5	211
799	S2219	11533.5	301	2038	S1022	-2095.5	301
800	S2218	11522.5	391	2039	S1021	-2106.5	391
801	S2217	11511.5	211	2040	S1020	-2117.5	211
802	S2216	11500.5	301	2041	S1019	-2128.5	301
803	S2215	11489.5	391	2042	S1018	-2139.5	391

804	S2214	11478.5	211	2043	S1017	-2150.5	211
805	S2213	11467.5	301	2044	S1016	-2161.5	301
806	S2212	11456.5	391	2045	S1015	-2172.5	391
807	S2211	11445.5	211	2046	S1014	-2183.5	211
808	S2210	11434.5	301	2047	S1013	-2194.5	301
809	S2209	11423.5	391	2048	S1012	-2205.5	391
810	S2208	11412.5	211	2049	S1011	-2216.5	211
811	S2207	11401.5	301	2050	S1010	-2227.5	301
812	S2206	11390.5	391	2051	S1009	-2238.5	391
813	S2205	11379.5	211	2052	S1008	-2249.5	211
814	S2204	11368.5	301	2053	S1007	-2260.5	301
815	S2203	11357.5	391	2054	S1006	-2271.5	391
816	S2202	11346.5	211	2055	S1005	-2282.5	211
817	S2201	11335.5	301	2056	S1004	-2293.5	301
818	S2200	11324.5	391	2057	S1003	-2304.5	391
819	S2199	11313.5	211	2058	S1002	-2315.5	211
820	S2198	11302.5	301	2059	S1001	-2326.5	301
821	S2197	11291.5	391	2060	S1000	-2337.5	391
822	S2196	11280.5	211	2061	S999	-2348.5	211
823	S2195	11269.5	301	2062	S998	-2359.5	301
824	S2194	11258.5	391	2063	S997	-2370.5	391
825	S2193	11247.5	211	2064	S996	-2381.5	211
826	S2192	11236.5	301	2065	S995	-2392.5	301
827	S2191	11225.5	391	2066	S994	-2403.5	391
828	S2190	11214.5	211	2067	S993	-2414.5	211
829	S2189	11203.5	301	2068	S992	-2425.5	301
830	S2188	11192.5	391	2069	S991	-2436.5	391
831	S2187	11181.5	211	2070	S990	-2447.5	211
832	S2186	11170.5	301	2071	S989	-2458.5	301
833	S2185	11159.5	391	2072	S988	-2469.5	391
834	S2184	11148.5	211	2073	S987	-2480.5	211
835	S2183	11137.5	301	2074	S986	-2491.5	301
836	S2182	11126.5	391	2075	S985	-2502.5	391
837	S2181	11115.5	211	2076	S984	-2513.5	211
838	S2180	11104.5	301	2077	S983	-2524.5	301
839	S2179	11093.5	391	2078	S982	-2535.5	391
840	S2178	11082.5	211	2079	S981	-2546.5	211
841	S2177	11071.5	301	2080	S980	-2557.5	301
842	S2176	11060.5	391	2081	S979	-2568.5	391
843	S2175	11049.5	211	2082	S978	-2579.5	211

844	S2174	11038.5	301	2083	S977	-2590.5	301
845	S2173	11027.5	391	2084	S976	-2601.5	391
846	S2172	11016.5	211	2085	S975	-2612.5	211
847	S2171	11005.5	301	2086	S974	-2623.5	301
848	S2170	10994.5	391	2087	S973	-2634.5	391
849	S2169	10983.5	211	2088	S972	-2645.5	211
850	S2168	10972.5	301	2089	S971	-2656.5	301
851	S2167	10961.5	391	2090	S970	-2667.5	391
852	S2166	10950.5	211	2091	S969	-2678.5	211
853	S2165	10939.5	301	2092	S968	-2689.5	301
854	S2164	10928.5	391	2093	S967	-2700.5	391
855	S2163	10917.5	211	2094	S966	-2711.5	211
856	S2162	10906.5	301	2095	S965	-2722.5	301
857	S2161	10895.5	391	2096	S964	-2733.5	391
858	S2160	10884.5	211	2097	S963	-2744.5	211
859	S2159	10873.5	301	2098	S962	-2755.5	301
860	S2158	10862.5	391	2099	S961	-2766.5	391
861	S2157	10851.5	211	2100	S960	-2777.5	211
862	S2156	10840.5	301	2101	S959	-2788.5	301
863	S2155	10829.5	391	2102	S958	-2799.5	391
864	S2154	10818.5	211	2103	S957	-2810.5	211
865	S2153	10807.5	301	2104	S956	-2821.5	301
866	S2152	10796.5	391	2105	S955	-2832.5	391
867	S2151	10785.5	211	2106	S954	-2843.5	211
868	S2150	10774.5	301	2107	S953	-2854.5	301
869	S2149	10763.5	391	2108	S952	-2865.5	391
870	S2148	10752.5	211	2109	S951	-2876.5	211
871	S2147	10741.5	301	2110	S950	-2887.5	301
872	S2146	10730.5	391	2111	S949	-2898.5	391
873	S2145	10719.5	211	2112	S948	-2909.5	211
874	S2144	10708.5	301	2113	S947	-2920.5	301
875	S2143	10697.5	391	2114	S946	-2931.5	391
876	S2142	10686.5	211	2115	S945	-2942.5	211
877	S2141	10675.5	301	2116	S944	-2953.5	301
878	S2140	10664.5	391	2117	S943	-2964.5	391
879	S2139	10653.5	211	2118	S942	-2975.5	211
880	S2138	10642.5	301	2119	S941	-2986.5	301
881	S2137	10631.5	391	2120	S940	-2997.5	391
882	S2136	10620.5	211	2121	S939	-3008.5	211
883	S2135	10609.5	301	2122	S938	-3019.5	301

884	S2134	10598.5	391	2123	S937	-3030.5	391
885	S2133	10587.5	211	2124	S936	-3041.5	211
886	S2132	10576.5	301	2125	S935	-3052.5	301
887	S2131	10565.5	391	2126	S934	-3063.5	391
888	S2130	10554.5	211	2127	S933	-3074.5	211
889	S2129	10543.5	301	2128	S932	-3085.5	301
890	S2128	10532.5	391	2129	S931	-3096.5	391
891	S2127	10521.5	211	2130	S930	-3107.5	211
892	S2126	10510.5	301	2131	S929	-3118.5	301
893	S2125	10499.5	391	2132	S928	-3129.5	391
894	S2124	10488.5	211	2133	S927	-3140.5	211
895	S2123	10477.5	301	2134	S926	-3151.5	301
896	S2122	10466.5	391	2135	S925	-3162.5	391
897	S2121	10455.5	211	2136	S924	-3173.5	211
898	S2120	10444.5	301	2137	S923	-3184.5	301
899	S2119	10433.5	391	2138	S922	-3195.5	391
900	S2118	10422.5	211	2139	S921	-3206.5	211
901	S2117	10411.5	301	2140	S920	-3217.5	301
902	S2116	10400.5	391	2141	S919	-3228.5	391
903	S2115	10389.5	211	2142	S918	-3239.5	211
904	S2114	10378.5	301	2143	S917	-3250.5	301
905	S2113	10367.5	391	2144	S916	-3261.5	391
906	S2112	10356.5	211	2145	S915	-3272.5	211
907	S2111	10345.5	301	2146	S914	-3283.5	301
908	S2110	10334.5	391	2147	S913	-3294.5	391
909	S2109	10323.5	211	2148	S912	-3305.5	211
910	S2108	10312.5	301	2149	S911	-3316.5	301
911	S2107	10301.5	391	2150	S910	-3327.5	391
912	S2106	10290.5	211	2151	S909	-3338.5	211
913	S2105	10279.5	301	2152	S908	-3349.5	301
914	S2104	10268.5	391	2153	S907	-3360.5	391
915	S2103	10257.5	211	2154	S906	-3371.5	211
916	S2102	10246.5	301	2155	S905	-3382.5	301
917	S2101	10235.5	391	2156	S904	-3393.5	391
918	S2100	10224.5	211	2157	S903	-3404.5	211
919	S2099	10213.5	301	2158	S902	-3415.5	301
920	S2098	10202.5	391	2159	S901	-3426.5	391
921	S2097	10191.5	211	2160	S900	-3437.5	211
922	S2096	10180.5	301	2161	S899	-3448.5	301
923	S2095	10169.5	391	2162	S898	-3459.5	391

924	S2094	10158.5	211	2163	S897	-3470.5	211
925	S2093	10147.5	301	2164	S896	-3481.5	301
926	S2092	10136.5	391	2165	S895	-3492.5	391
927	S2091	10125.5	211	2166	S894	-3503.5	211
928	S2090	10114.5	301	2167	S893	-3514.5	301
929	S2089	10103.5	391	2168	S892	-3525.5	391
930	S2088	10092.5	211	2169	S891	-3536.5	211
931	S2087	10081.5	301	2170	S890	-3547.5	301
932	S2086	10070.5	391	2171	S889	-3558.5	391
933	S2085	10059.5	211	2172	S888	-3569.5	211
934	S2084	10048.5	301	2173	S887	-3580.5	301
935	S2083	10037.5	391	2174	S886	-3591.5	391
936	S2082	10026.5	211	2175	S885	-3602.5	211
937	S2081	10015.5	301	2176	S884	-3613.5	301
938	S2080	10004.5	391	2177	S883	-3624.5	391
939	S2079	9993.5	211	2178	S882	-3635.5	211
940	S2078	9982.5	301	2179	S881	-3646.5	301
941	S2077	9971.5	391	2180	S880	-3657.5	391
942	S2076	9960.5	211	2181	S879	-3668.5	211
943	S2075	9949.5	301	2182	S878	-3679.5	301
944	S2074	9938.5	391	2183	S877	-3690.5	391
945	S2073	9927.5	211	2184	S876	-3701.5	211
946	S2072	9916.5	301	2185	S875	-3712.5	301
947	S2071	9905.5	391	2186	S874	-3723.5	391
948	S2070	9894.5	211	2187	S873	-3734.5	211
949	S2069	9883.5	301	2188	S872	-3745.5	301
950	S2068	9872.5	391	2189	S871	-3756.5	391
951	S2067	9861.5	211	2190	S870	-3767.5	211
952	S2066	9850.5	301	2191	S869	-3778.5	301
953	S2065	9839.5	391	2192	S868	-3789.5	391
954	S2064	9828.5	211	2193	S867	-3800.5	211
955	S2063	9817.5	301	2194	S866	-3811.5	301
956	S2062	9806.5	391	2195	S865	-3822.5	391
957	S2061	9795.5	211	2196	S864	-3833.5	211
958	S2060	9784.5	301	2197	S863	-3844.5	301
959	S2059	9773.5	391	2198	S862	-3855.5	391
960	S2058	9762.5	211	2199	S861	-3866.5	211
961	S2057	9751.5	301	2200	S860	-3877.5	301
962	S2056	9740.5	391	2201	S859	-3888.5	391
963	S2055	9729.5	211	2202	S858	-3899.5	211

964	S2054	9718.5	301	2203	S857	-3910.5	301
965	S2053	9707.5	391	2204	S856	-3921.5	391
966	S2052	9696.5	211	2205	S855	-3932.5	211
967	S2051	9685.5	301	2206	S854	-3943.5	301
968	S2050	9674.5	391	2207	S853	-3954.5	391
969	S2049	9663.5	211	2208	S852	-3965.5	211
970	S2048	9652.5	301	2209	S851	-3976.5	301
971	S2047	9641.5	391	2210	S850	-3987.5	391
972	S2046	9630.5	211	2211	S849	-3998.5	211
973	S2045	9619.5	301	2212	S848	-4009.5	301
974	S2044	9608.5	391	2213	S847	-4020.5	391
975	S2043	9597.5	211	2214	S846	-4031.5	211
976	S2042	9586.5	301	2215	S845	-4042.5	301
977	S2041	9575.5	391	2216	S844	-4053.5	391
978	S2040	9564.5	211	2217	S843	-4064.5	211
979	S2039	9553.5	301	2218	S842	-4075.5	301
980	S2038	9542.5	391	2219	S841	-4086.5	391
981	S2037	9531.5	211	2220	S840	-4097.5	211
982	S2036	9520.5	301	2221	S839	-4108.5	301
983	S2035	9509.5	391	2222	S838	-4119.5	391
984	S2034	9498.5	211	2223	S837	-4130.5	211
985	S2033	9487.5	301	2224	S836	-4141.5	301
986	S2032	9476.5	391	2225	S835	-4152.5	391
987	S2031	9465.5	211	2226	S834	-4163.5	211
988	S2030	9454.5	301	2227	S833	-4174.5	301
989	S2029	9443.5	391	2228	S832	-4185.5	391
990	S2028	9432.5	211	2229	S831	-4196.5	211
991	S2027	9421.5	301	2230	S830	-4207.5	301
992	S2026	9410.5	391	2231	S829	-4218.5	391
993	S2025	9399.5	211	2232	S828	-4229.5	211
994	S2024	9388.5	301	2233	S827	-4240.5	301
995	S2023	9377.5	391	2234	S826	-4251.5	391
996	S2022	9366.5	211	2235	S825	-4262.5	211
997	S2021	9355.5	301	2236	S824	-4273.5	301
998	S2020	9344.5	391	2237	S823	-4284.5	391
999	S2019	9333.5	211	2238	S822	-4295.5	211
1000	S2018	9322.5	301	2239	S821	-4306.5	301
1001	S2017	9311.5	391	2240	S820	-4317.5	391
1002	S2016	9300.5	211	2241	S819	-4328.5	211
1003	S2015	9289.5	301	2242	S818	-4339.5	301

1004	S2014	9278.5	391	2243	S817	-4350.5	391
1005	S2013	9267.5	211	2244	S816	-4361.5	211
1006	S2012	9256.5	301	2245	S815	-4372.5	301
1007	S2011	9245.5	391	2246	S814	-4383.5	391
1008	S2010	9234.5	211	2247	S813	-4394.5	211
1009	S2009	9223.5	301	2248	S812	-4405.5	301
1010	S2008	9212.5	391	2249	S811	-4416.5	391
1011	S2007	9201.5	211	2250	S810	-4427.5	211
1012	S2006	9190.5	301	2251	S809	-4438.5	301
1013	S2005	9179.5	391	2252	S808	-4449.5	391
1014	S2004	9168.5	211	2253	S807	-4460.5	211
1015	S2003	9157.5	301	2254	S806	-4471.5	301
1016	S2002	9146.5	391	2255	S805	-4482.5	391
1017	S2001	9135.5	211	2256	S804	-4493.5	211
1018	S2000	9124.5	301	2257	S803	-4504.5	301
1019	S1999	9113.5	391	2258	S802	-4515.5	391
1020	S1998	9102.5	211	2259	S801	-4526.5	211
1021	S1997	9091.5	301	2260	S800	-4537.5	301
1022	S1996	9080.5	391	2261	S799	-4548.5	391
1023	S1995	9069.5	211	2262	S798	-4559.5	211
1024	S1994	9058.5	301	2263	S797	-4570.5	301
1025	S1993	9047.5	391	2264	S796	-4581.5	391
1026	S1992	9036.5	211	2265	S795	-4592.5	211
1027	S1991	9025.5	301	2266	S794	-4603.5	301
1028	S1990	9014.5	391	2267	S793	-4614.5	391
1029	S1989	9003.5	211	2268	S792	-4625.5	211
1030	S1988	8992.5	301	2269	S791	-4636.5	301
1031	S1987	8981.5	391	2270	S790	-4647.5	391
1032	S1986	8970.5	211	2271	S789	-4658.5	211
1033	S1985	8959.5	301	2272	S788	-4669.5	301
1034	S1984	8948.5	391	2273	S787	-4680.5	391
1035	S1983	8937.5	211	2274	S786	-4691.5	211
1036	S1982	8926.5	301	2275	S785	-4702.5	301
1037	S1981	8915.5	391	2276	S784	-4713.5	391
1038	S1980	8904.5	211	2277	S783	-4724.5	211
1039	S1979	8893.5	301	2278	S782	-4735.5	301
1040	S1978	8882.5	391	2279	S781	-4746.5	391
1041	S1977	8871.5	211	2280	S780	-4757.5	211
1042	S1976	8860.5	301	2281	S779	-4768.5	301
1043	S1975	8849.5	391	2282	S778	-4779.5	391

1044	S1974	8838.5	211	2283	S777	-4790.5	211
1045	S1973	8827.5	301	2284	S776	-4801.5	301
1046	S1972	8816.5	391	2285	S775	-4812.5	391
1047	S1971	8805.5	211	2286	S774	-4823.5	211
1048	S1970	8794.5	301	2287	S773	-4834.5	301
1049	S1969	8783.5	391	2288	S772	-4845.5	391
1050	S1968	8772.5	211	2289	S771	-4856.5	211
1051	S1967	8761.5	301	2290	S770	-4867.5	301
1052	S1966	8750.5	391	2291	S769	-4878.5	391
1053	S1965	8739.5	211	2292	S768	-4889.5	211
1054	S1964	8728.5	301	2293	S767	-4900.5	301
1055	S1963	8717.5	391	2294	S766	-4911.5	391
1056	S1962	8706.5	211	2295	S765	-4922.5	211
1057	S1961	8695.5	301	2296	S764	-4933.5	301
1058	S1960	8684.5	391	2297	S763	-4944.5	391
1059	S1959	8673.5	211	2298	S762	-4955.5	211
1060	S1958	8662.5	301	2299	S761	-4966.5	301
1061	S1957	8651.5	391	2300	S760	-4977.5	391
1062	S1956	8640.5	211	2301	S759	-4988.5	211
1063	S1955	8629.5	301	2302	S758	-4999.5	301
1064	S1954	8618.5	391	2303	S757	-5010.5	391
1065	S1953	8607.5	211	2304	S756	-5021.5	211
1066	S1952	8596.5	301	2305	S755	-5032.5	301
1067	S1951	8585.5	391	2306	S754	-5043.5	391
1068	S1950	8574.5	211	2307	S753	-5054.5	211
1069	S1949	8563.5	301	2308	S752	-5065.5	301
1070	S1948	8552.5	391	2309	S751	-5076.5	391
1071	S1947	8541.5	211	2310	S750	-5087.5	211
1072	S1946	8530.5	301	2311	S749	-5098.5	301
1073	S1945	8519.5	391	2312	S748	-5109.5	391
1074	S1944	8508.5	211	2313	S747	-5120.5	211
1075	S1943	8497.5	301	2314	S746	-5131.5	301
1076	S1942	8486.5	391	2315	S745	-5142.5	391
1077	S1941	8475.5	211	2316	S744	-5153.5	211
1078	S1940	8464.5	301	2317	S743	-5164.5	301
1079	S1939	8453.5	391	2318	S742	-5175.5	391
1080	S1938	8442.5	211	2319	S741	-5186.5	211
1081	S1937	8431.5	301	2320	S740	-5197.5	301
1082	S1936	8420.5	391	2321	S739	-5208.5	391
1083	S1935	8409.5	211	2322	S738	-5219.5	211

1084	S1934	8398.5	301	2323	S737	-5230.5	301
1085	S1933	8387.5	391	2324	S736	-5241.5	391
1086	S1932	8376.5	211	2325	S735	-5252.5	211
1087	S1931	8365.5	301	2326	S734	-5263.5	301
1088	S1930	8354.5	391	2327	S733	-5274.5	391
1089	S1929	8343.5	211	2328	S732	-5285.5	211
1090	S1928	8332.5	301	2329	S731	-5296.5	301
1091	S1927	8321.5	391	2330	S730	-5307.5	391
1092	S1926	8310.5	211	2331	S729	-5318.5	211
1093	S1925	8299.5	301	2332	S728	-5329.5	301
1094	S1924	8288.5	391	2333	S727	-5340.5	391
1095	S1923	8277.5	211	2334	S726	-5351.5	211
1096	S1922	8266.5	301	2335	S725	-5362.5	301
1097	S1921	8255.5	391	2336	S724	-5373.5	391
1098	S1920	8244.5	211	2337	S723	-5384.5	211
1099	S1919	8233.5	301	2338	S722	-5395.5	301
1100	S1918	8222.5	391	2339	S721	-5406.5	391
1101	S1917	8211.5	211	2340	S720	-5417.5	211
1102	S1916	8200.5	301	2341	S719	-5428.5	301
1103	S1915	8189.5	391	2342	S718	-5439.5	391
1104	S1914	8178.5	211	2343	S717	-5450.5	211
1105	S1913	8167.5	301	2344	S716	-5461.5	301
1106	S1912	8156.5	391	2345	S715	-5472.5	391
1107	S1911	8145.5	211	2346	S714	-5483.5	211
1108	S1910	8134.5	301	2347	S713	-5494.5	301
1109	S1909	8123.5	391	2348	S712	-5505.5	391
1110	S1908	8112.5	211	2349	S711	-5516.5	211
1111	S1907	8101.5	301	2350	S710	-5527.5	301
1112	S1906	8090.5	391	2351	S709	-5538.5	391
1113	S1905	8079.5	211	2352	S708	-5549.5	211
1114	S1904	8068.5	301	2353	S707	-5560.5	301
1115	S1903	8057.5	391	2354	S706	-5571.5	391
1116	S1902	8046.5	211	2355	S705	-5582.5	211
1117	S1901	8035.5	301	2356	S704	-5593.5	301
1118	S1900	8024.5	391	2357	S703	-5604.5	391
1119	S1899	8013.5	211	2358	S702	-5615.5	211
1120	S1898	8002.5	301	2359	S701	-5626.5	301
1121	S1897	7991.5	391	2360	S700	-5637.5	391
1122	S1896	7980.5	211	2361	S699	-5648.5	211
1123	S1895	7969.5	301	2362	S698	-5659.5	301

1124	S1894	7958.5	391	2363	S697	-5670.5	391
1125	S1893	7947.5	211	2364	S696	-5681.5	211
1126	S1892	7936.5	301	2365	S695	-5692.5	301
1127	S1891	7925.5	391	2366	S694	-5703.5	391
1128	S1890	7914.5	211	2367	S693	-5714.5	211
1129	S1889	7903.5	301	2368	S692	-5725.5	301
1130	S1888	7892.5	391	2369	S691	-5736.5	391
1131	S1887	7881.5	211	2370	S690	-5747.5	211
1132	S1886	7870.5	301	2371	S689	-5758.5	301
1133	S1885	7859.5	391	2372	S688	-5769.5	391
1134	S1884	7848.5	211	2373	S687	-5780.5	211
1135	S1883	7837.5	301	2374	S686	-5791.5	301
1136	S1882	7826.5	391	2375	S685	-5802.5	391
1137	S1881	7815.5	211	2376	S684	-5813.5	211
1138	S1880	7804.5	301	2377	S683	-5824.5	301
1139	S1879	7793.5	391	2378	S682	-5835.5	391
1140	S1878	7782.5	211	2379	S681	-5846.5	211
1141	S1877	7771.5	301	2380	S680	-5857.5	301
1142	S1876	7760.5	391	2381	S679	-5868.5	391
1143	S1875	7749.5	211	2382	S678	-5879.5	211
1144	S1874	7738.5	301	2383	S677	-5890.5	301
1145	S1873	7727.5	391	2384	S676	-5901.5	391
1146	S1872	7716.5	211	2385	S675	-5912.5	211
1147	S1871	7705.5	301	2386	S674	-5923.5	301
1148	S1870	7694.5	391	2387	S673	-5934.5	391
1149	S1869	7683.5	211	2388	S672	-5945.5	211
1150	S1868	7672.5	301	2389	S671	-5956.5	301
1151	S1867	7661.5	391	2390	S670	-5967.5	391
1152	S1866	7650.5	211	2391	S669	-5978.5	211
1153	S1865	7639.5	301	2392	S668	-5989.5	301
1154	S1864	7628.5	391	2393	S667	-6000.5	391
1155	S1863	7617.5	211	2394	S666	-6011.5	211
1156	S1862	7606.5	301	2395	S665	-6022.5	301
1157	S1861	7595.5	391	2396	S664	-6033.5	391
1158	S1860	7584.5	211	2397	S663	-6044.5	211
1159	S1859	7573.5	301	2398	S662	-6055.5	301
1160	S1858	7562.5	391	2399	S661	-6066.5	391
1161	S1857	7551.5	211	2400	S660	-6077.5	211
1162	S1856	7540.5	301	2401	S659	-6088.5	301
1163	S1855	7529.5	391	2402	S658	-6099.5	391

1164	S1854	7518.5	211	2403	S657	-6110.5	211
1165	S1853	7507.5	301	2404	S656	-6121.5	301
1166	S1852	7496.5	391	2405	S655	-6132.5	391
1167	S1851	7485.5	211	2406	S654	-6143.5	211
1168	S1850	7474.5	301	2407	S653	-6154.5	301
1169	S1849	7463.5	391	2408	S652	-6165.5	391
1170	S1848	7452.5	211	2409	S651	-6176.5	211
1171	S1847	7441.5	301	2410	S650	-6187.5	301
1172	S1846	7430.5	391	2411	S649	-6198.5	391
1173	S1845	7419.5	211	2412	S648	-6209.5	211
1174	S1844	7408.5	301	2413	S647	-6220.5	301
1175	S1843	7397.5	391	2414	S646	-6231.5	391
1176	S1842	7386.5	211	2415	S645	-6242.5	211
1177	S1841	7375.5	301	2416	S644	-6253.5	301
1178	S1840	7364.5	391	2417	S643	-6264.5	391
1179	S1839	7353.5	211	2418	S642	-6275.5	211
1180	S1838	7342.5	301	2419	S641	-6286.5	301
1181	S1837	7331.5	391	2420	S640	-6297.5	391
1182	S1836	7320.5	211	2421	S639	-6308.5	211
1183	S1835	7309.5	301	2422	S638	-6319.5	301
1184	S1834	7298.5	391	2423	S637	-6330.5	391
1185	S1833	7287.5	211	2424	S636	-6341.5	211
1186	S1832	7276.5	301	2425	S635	-6352.5	301
1187	S1831	7265.5	391	2426	S634	-6363.5	391
1188	S1830	7254.5	211	2427	S633	-6374.5	211
1189	S1829	7243.5	301	2428	S632	-6385.5	301
1190	S1828	7232.5	391	2429	S631	-6396.5	391
1191	S1827	7221.5	211	2430	S630	-6407.5	211
1192	S1826	7210.5	301	2431	S629	-6418.5	301
1193	S1825	7199.5	391	2432	S628	-6429.5	391
1194	S1824	7188.5	211	2433	S627	-6440.5	211
1195	S1823	7177.5	301	2434	S626	-6451.5	301
1196	S1822	7166.5	391	2435	S625	-6462.5	391
1197	S1821	7155.5	211	2436	S624	-6473.5	211
1198	S1820	7144.5	301	2437	S623	-6484.5	301
1199	S1819	7133.5	391	2438	S622	-6495.5	391
1200	S1818	7122.5	211	2439	S621	-6506.5	211
1201	S1817	7111.5	301	2440	S620	-6517.5	301
1202	S1816	7100.5	391	2441	S619	-6528.5	391
1203	S1815	7089.5	211	2442	S618	-6539.5	211

1204	S1814	7078.5	301	2443	S617	-6550.5	301
1205	S1813	7067.5	391	2444	S616	-6561.5	391
1206	S1812	7056.5	211	2445	S615	-6572.5	211
1207	S1811	7045.5	301	2446	S614	-6583.5	301
1208	S1810	7034.5	391	2447	S613	-6594.5	391
1209	S1809	7023.5	211	2448	S612	-6605.5	211
1210	S1808	7012.5	301	2449	S611	-6616.5	301
1211	S1807	7001.5	391	2450	S610	-6627.5	391
1212	S1806	6990.5	211	2451	S609	-6638.5	211
1213	S1805	6979.5	301	2452	S608	-6649.5	301
1214	S1804	6968.5	391	2453	S607	-6660.5	391
1215	S1803	6957.5	211	2454	S606	-6671.5	211
1216	S1802	6946.5	301	2455	S605	-6682.5	301
1217	S1801	6935.5	391	2456	S604	-6693.5	391
1218	DUMMY	6924.5	211	2457	S603	-6704.5	211
1219	DUMMY	6913.5	301	2458	S602	-6715.5	301
1220	DUMMY	6902.5	391	2459	S601	-6726.5	391
1221	DUMMY	6891.5	211	2460	DUMMY	-6737.5	211
1222	DUMMY	6880.5	301	2461	DUMMY	-6748.5	301
1223	DUMMY	6869.5	391	2462	DUMMY	-6759.5	391
1224	DUMMY	6858.5	211	2463	DUMMY	-6770.5	211
1225	DUMMY	6847.5	301	2464	DUMMY	-6781.5	301
1226	DUMMY	6836.5	391	2465	DUMMY	-6792.5	391
1227	DUMMY	6825.5	211	2466	DUMMY	-6803.5	211
1228	DUMMY	6814.5	301	2467	DUMMY	-6814.5	301
1229	DUMMY	6803.5	391	2468	DUMMY	-6825.5	391
1230	DUMMY	6792.5	211	2469	DUMMY	-6836.5	211
1231	DUMMY	6781.5	301	2470	DUMMY	-6847.5	301
1232	DUMMY	6770.5	391	2471	DUMMY	-6858.5	391
1233	DUMMY	6759.5	211	2472	DUMMY	-6869.5	211
1234	DUMMY	6748.5	301	2473	DUMMY	-6880.5	301
1235	DUMMY	6737.5	391	2474	DUMMY	-6891.5	391
1236	S1800	6726.5	211	2475	DUMMY	-6902.5	211
1237	S1799	6715.5	301	2476	DUMMY	-6913.5	301
1238	S1798	6704.5	391	2477	DUMMY	-6924.5	391
1239	S1797	6693.5	211	2478	S600	-6935.5	211
1240	S1796	6682.5	301	2479	S599	-6946.5	301
1241	S1795	6671.5	391	2480	S598	-6957.5	391
1242	S1794	6660.5	211	2481	S597	-6968.5	211
1243	S1793	6649.5	301	2482	S596	-6979.5	301

1244	S1792	6638.5	391	2483	S595	-6990.5	391
1245	S1791	6627.5	211	2484	S594	-7001.5	211
1246	S1790	6616.5	301	2485	S593	-7012.5	301
1247	S1789	6605.5	391	2486	S592	-7023.5	391
1248	S1788	6594.5	211	2487	S591	-7034.5	211
1249	S1787	6583.5	301	2488	S590	-7045.5	301
1250	S1786	6572.5	391	2489	S589	-7056.5	391
1251	S1785	6561.5	211	2490	S588	-7067.5	211
1252	S1784	6550.5	301	2491	S587	-7078.5	301
1253	S1783	6539.5	391	2492	S586	-7089.5	391
1254	S1782	6528.5	211	2493	S585	-7100.5	211
1255	S1781	6517.5	301	2494	S584	-7111.5	301
1256	S1780	6506.5	391	2495	S583	-7122.5	391
1257	S1779	6495.5	211	2496	S582	-7133.5	211
1258	S1778	6484.5	301	2497	S581	-7144.5	301
1259	S1777	6473.5	391	2498	S580	-7155.5	391
1260	S1776	6462.5	211	2499	S579	-7166.5	211
1261	S1775	6451.5	301	2500	S578	-7177.5	301
1262	S1774	6440.5	391	2501	S577	-7188.5	391
1263	S1773	6429.5	211	2502	S576	-7199.5	211
1264	S1772	6418.5	301	2503	S575	-7210.5	301
1265	S1771	6407.5	391	2504	S574	-7221.5	391
1266	S1770	6396.5	211	2505	S573	-7232.5	211
1267	S1769	6385.5	301	2506	S572	-7243.5	301
1268	S1768	6374.5	391	2507	S571	-7254.5	391
1269	S1767	6363.5	211	2508	S570	-7265.5	211
1270	S1766	6352.5	301	2509	S569	-7276.5	301
1271	S1765	6341.5	391	2510	S568	-7287.5	391
1272	S1764	6330.5	211	2511	S567	-7298.5	211
1273	S1763	6319.5	301	2512	S566	-7309.5	301
1274	S1762	6308.5	391	2513	S565	-7320.5	391
1275	S1761	6297.5	211	2514	S564	-7331.5	211
1276	S1760	6286.5	301	2515	S563	-7342.5	301
1277	S1759	6275.5	391	2516	S562	-7353.5	391
1278	S1758	6264.5	211	2517	S561	-7364.5	211
1279	S1757	6253.5	301	2518	S560	-7375.5	301
1280	S1756	6242.5	391	2519	S559	-7386.5	391
1281	S1755	6231.5	211	2520	S558	-7397.5	211
1282	S1754	6220.5	301	2521	S557	-7408.5	301
1283	S1753	6209.5	391	2522	S556	-7419.5	391

1284	S1752	6198.5	211	2523	S555	-7430.5	211
1285	S1751	6187.5	301	2524	S554	-7441.5	301
1286	S1750	6176.5	391	2525	S553	-7452.5	391
1287	S1749	6165.5	211	2526	S552	-7463.5	211
1288	S1748	6154.5	301	2527	S551	-7474.5	301
1289	S1747	6143.5	391	2528	S550	-7485.5	391
1290	S1746	6132.5	211	2529	S549	-7496.5	211
1291	S1745	6121.5	301	2530	S548	-7507.5	301
1292	S1744	6110.5	391	2531	S547	-7518.5	391
1293	S1743	6099.5	211	2532	S546	-7529.5	211
1294	S1742	6088.5	301	2533	S545	-7540.5	301
1295	S1741	6077.5	391	2534	S544	-7551.5	391
1296	S1740	6066.5	211	2535	S543	-7562.5	211
1297	S1739	6055.5	301	2536	S542	-7573.5	301
1298	S1738	6044.5	391	2537	S541	-7584.5	391
1299	S1737	6033.5	211	2538	S540	-7595.5	211
1300	S1736	6022.5	301	2539	S539	-7606.5	301
1301	S1735	6011.5	391	2540	S538	-7617.5	391
1302	S1734	6000.5	211	2541	S537	-7628.5	211
1303	S1733	5989.5	301	2542	S536	-7639.5	301
1304	S1732	5978.5	391	2543	S535	-7650.5	391
1305	S1731	5967.5	211	2544	S534	-7661.5	211
1306	S1730	5956.5	301	2545	S533	-7672.5	301
1307	S1729	5945.5	391	2546	S532	-7683.5	391
1308	S1728	5934.5	211	2547	S531	-7694.5	211
1309	S1727	5923.5	301	2548	S530	-7705.5	301
1310	S1726	5912.5	391	2549	S529	-7716.5	391
1311	S1725	5901.5	211	2550	S528	-7727.5	211
1312	S1724	5890.5	301	2551	S527	-7738.5	301
1313	S1723	5879.5	391	2552	S526	-7749.5	391
1314	S1722	5868.5	211	2553	S525	-7760.5	211
1315	S1721	5857.5	301	2554	S524	-7771.5	301
1316	S1720	5846.5	391	2555	S523	-7782.5	391
1317	S1719	5835.5	211	2556	S522	-7793.5	211
1318	S1718	5824.5	301	2557	S521	-7804.5	301
1319	S1717	5813.5	391	2558	S520	-7815.5	391
1320	S1716	5802.5	211	2559	S519	-7826.5	211
1321	S1715	5791.5	301	2560	S518	-7837.5	301
1322	S1714	5780.5	391	2561	S517	-7848.5	391
1323	S1713	5769.5	211	2562	S516	-7859.5	211

1324	S1712	5758.5	301	2563	S515	-7870.5	301
1325	S1711	5747.5	391	2564	S514	-7881.5	391
1326	S1710	5736.5	211	2565	S513	-7892.5	211
1327	S1709	5725.5	301	2566	S512	-7903.5	301
1328	S1708	5714.5	391	2567	S511	-7914.5	391
1329	S1707	5703.5	211	2568	S510	-7925.5	211
1330	S1706	5692.5	301	2569	S509	-7936.5	301
1331	S1705	5681.5	391	2570	S508	-7947.5	391
1332	S1704	5670.5	211	2571	S507	-7958.5	211
1333	S1703	5659.5	301	2572	S506	-7969.5	301
1334	S1702	5648.5	391	2573	S505	-7980.5	391
1335	S1701	5637.5	211	2574	S504	-7991.5	211
1336	S1700	5626.5	301	2575	S503	-8002.5	301
1337	S1699	5615.5	391	2576	S502	-8013.5	391
1338	S1698	5604.5	211	2577	S501	-8024.5	211
1339	S1697	5593.5	301	2578	S500	-8035.5	301
1340	S1696	5582.5	391	2579	S499	-8046.5	391
1341	S1695	5571.5	211	2580	S498	-8057.5	211
1342	S1694	5560.5	301	2581	S497	-8068.5	301
1343	S1693	5549.5	391	2582	S496	-8079.5	391
1344	S1692	5538.5	211	2583	S495	-8090.5	211
1345	S1691	5527.5	301	2584	S494	-8101.5	301
1346	S1690	5516.5	391	2585	S493	-8112.5	391
1347	S1689	5505.5	211	2586	S492	-8123.5	211
1348	S1688	5494.5	301	2587	S491	-8134.5	301
1349	S1687	5483.5	391	2588	S490	-8145.5	391
1350	S1686	5472.5	211	2589	S489	-8156.5	211
1351	S1685	5461.5	301	2590	S488	-8167.5	301
1352	S1684	5450.5	391	2591	S487	-8178.5	391
1353	S1683	5439.5	211	2592	S486	-8189.5	211
1354	S1682	5428.5	301	2593	S485	-8200.5	301
1355	S1681	5417.5	391	2594	S484	-8211.5	391
1356	S1680	5406.5	211	2595	S483	-8222.5	211
1357	S1679	5395.5	301	2596	S482	-8233.5	301
1358	S1678	5384.5	391	2597	S481	-8244.5	391
1359	S1677	5373.5	211	2598	S480	-8255.5	211
1360	S1676	5362.5	301	2599	S479	-8266.5	301
1361	S1675	5351.5	391	2600	S478	-8277.5	391
1362	S1674	5340.5	211	2601	S477	-8288.5	211
1363	S1673	5329.5	301	2602	S476	-8299.5	301

1364	S1672	5318.5	391	2603	S475	-8310.5	391
1365	S1671	5307.5	211	2604	S474	-8321.5	211
1366	S1670	5296.5	301	2605	S473	-8332.5	301
1367	S1669	5285.5	391	2606	S472	-8343.5	391
1368	S1668	5274.5	211	2607	S471	-8354.5	211
1369	S1667	5263.5	301	2608	S470	-8365.5	301
1370	S1666	5252.5	391	2609	S469	-8376.5	391
1371	S1665	5241.5	211	2610	S468	-8387.5	211
1372	S1664	5230.5	301	2611	S467	-8398.5	301
1373	S1663	5219.5	391	2612	S466	-8409.5	391
1374	S1662	5208.5	211	2613	S465	-8420.5	211
1375	S1661	5197.5	301	2614	S464	-8431.5	301
1376	S1660	5186.5	391	2615	S463	-8442.5	391
1377	S1659	5175.5	211	2616	S462	-8453.5	211
1378	S1658	5164.5	301	2617	S461	-8464.5	301
1379	S1657	5153.5	391	2618	S460	-8475.5	391
1380	S1656	5142.5	211	2619	S459	-8486.5	211
1381	S1655	5131.5	301	2620	S458	-8497.5	301
1382	S1654	5120.5	391	2621	S457	-8508.5	391
1383	S1653	5109.5	211	2622	S456	-8519.5	211
1384	S1652	5098.5	301	2623	S455	-8530.5	301
1385	S1651	5087.5	391	2624	S454	-8541.5	391
1386	S1650	5076.5	211	2625	S453	-8552.5	211
1387	S1649	5065.5	301	2626	S452	-8563.5	301
1388	S1648	5054.5	391	2627	S451	-8574.5	391
1389	S1647	5043.5	211	2628	S450	-8585.5	211
1390	S1646	5032.5	301	2629	S449	-8596.5	301
1391	S1645	5021.5	391	2630	S448	-8607.5	391
1392	S1644	5010.5	211	2631	S447	-8618.5	211
1393	S1643	4999.5	301	2632	S446	-8629.5	301
1394	S1642	4988.5	391	2633	S445	-8640.5	391
1395	S1641	4977.5	211	2634	S444	-8651.5	211
1396	S1640	4966.5	301	2635	S443	-8662.5	301
1397	S1639	4955.5	391	2636	S442	-8673.5	391
1398	S1638	4944.5	211	2637	S441	-8684.5	211
1399	S1637	4933.5	301	2638	S440	-8695.5	301
1400	S1636	4922.5	391	2639	S439	-8706.5	391
1401	S1635	4911.5	211	2640	S438	-8717.5	211
1402	S1634	4900.5	301	2641	S437	-8728.5	301
1403	S1633	4889.5	391	2642	S436	-8739.5	391

1404	S1632	4878.5	211	2643	S435	-8750.5	211
1405	S1631	4867.5	301	2644	S434	-8761.5	301
1406	S1630	4856.5	391	2645	S433	-8772.5	391
1407	S1629	4845.5	211	2646	S432	-8783.5	211
1408	S1628	4834.5	301	2647	S431	-8794.5	301
1409	S1627	4823.5	391	2648	S430	-8805.5	391
1410	S1626	4812.5	211	2649	S429	-8816.5	211
1411	S1625	4801.5	301	2650	S428	-8827.5	301
1412	S1624	4790.5	391	2651	S427	-8838.5	391
1413	S1623	4779.5	211	2652	S426	-8849.5	211
1414	S1622	4768.5	301	2653	S425	-8860.5	301
1415	S1621	4757.5	391	2654	S424	-8871.5	391
1416	S1620	4746.5	211	2655	S423	-8882.5	211
1417	S1619	4735.5	301	2656	S422	-8893.5	301
1418	S1618	4724.5	391	2657	S421	-8904.5	391
1419	S1617	4713.5	211	2658	S420	-8915.5	211
1420	S1616	4702.5	301	2659	S419	-8926.5	301
1421	S1615	4691.5	391	2660	S418	-8937.5	391
1422	S1614	4680.5	211	2661	S417	-8948.5	211
1423	S1613	4669.5	301	2662	S416	-8959.5	301
1424	S1612	4658.5	391	2663	S415	-8970.5	391
1425	S1611	4647.5	211	2664	S414	-8981.5	211
1426	S1610	4636.5	301	2665	S413	-8992.5	301
1427	S1609	4625.5	391	2666	S412	-9003.5	391
1428	S1608	4614.5	211	2667	S411	-9014.5	211
1429	S1607	4603.5	301	2668	S410	-9025.5	301
1430	S1606	4592.5	391	2669	S409	-9036.5	391
1431	S1605	4581.5	211	2670	S408	-9047.5	211
1432	S1604	4570.5	301	2671	S407	-9058.5	301
1433	S1603	4559.5	391	2672	S406	-9069.5	391
1434	S1602	4548.5	211	2673	S405	-9080.5	211
1435	S1601	4537.5	301	2674	S404	-9091.5	301
1436	S1600	4526.5	391	2675	S403	-9102.5	391
1437	S1599	4515.5	211	2676	S402	-9113.5	211
1438	S1598	4504.5	301	2677	S401	-9124.5	301
1439	S1597	4493.5	391	2678	S400	-9135.5	391
1440	S1596	4482.5	211	2679	S399	-9146.5	211
1441	S1595	4471.5	301	2680	S398	-9157.5	301
1442	S1594	4460.5	391	2681	S397	-9168.5	391
1443	S1593	4449.5	211	2682	S396	-9179.5	211

1444	S1592	4438.5	301	2683	S395	-9190.5	301
1445	S1591	4427.5	391	2684	S394	-9201.5	391
1446	S1590	4416.5	211	2685	S393	-9212.5	211
1447	S1589	4405.5	301	2686	S392	-9223.5	301
1448	S1588	4394.5	391	2687	S391	-9234.5	391
1449	S1587	4383.5	211	2688	S390	-9245.5	211
1450	S1586	4372.5	301	2689	S389	-9256.5	301
1451	S1585	4361.5	391	2690	S388	-9267.5	391
1452	S1584	4350.5	211	2691	S387	-9278.5	211
1453	S1583	4339.5	301	2692	S386	-9289.5	301
1454	S1582	4328.5	391	2693	S385	-9300.5	391
1455	S1581	4317.5	211	2694	S384	-9311.5	211
1456	S1580	4306.5	301	2695	S383	-9322.5	301
1457	S1579	4295.5	391	2696	S382	-9333.5	391
1458	S1578	4284.5	211	2697	S381	-9344.5	211
1459	S1577	4273.5	301	2698	S380	-9355.5	301
1460	S1576	4262.5	391	2699	S379	-9366.5	391
1461	S1575	4251.5	211	2700	S378	-9377.5	211
1462	S1574	4240.5	301	2701	S377	-9388.5	301
1463	S1573	4229.5	391	2702	S376	-9399.5	391
1464	S1572	4218.5	211	2703	S375	-9410.5	211
1465	S1571	4207.5	301	2704	S374	-9421.5	301
1466	S1570	4196.5	391	2705	S373	-9432.5	391
1467	S1569	4185.5	211	2706	S372	-9443.5	211
1468	S1568	4174.5	301	2707	S371	-9454.5	301
1469	S1567	4163.5	391	2708	S370	-9465.5	391
1470	S1566	4152.5	211	2709	S369	-9476.5	211
1471	S1565	4141.5	301	2710	S368	-9487.5	301
1472	S1564	4130.5	391	2711	S367	-9498.5	391
1473	S1563	4119.5	211	2712	S366	-9509.5	211
1474	S1562	4108.5	301	2713	S365	-9520.5	301
1475	S1561	4097.5	391	2714	S364	-9531.5	391
1476	S1560	4086.5	211	2715	S363	-9542.5	211
1477	S1559	4075.5	301	2716	S362	-9553.5	301
1478	S1558	4064.5	391	2717	S361	-9564.5	391
1479	S1557	4053.5	211	2718	S360	-9575.5	211
1480	S1556	4042.5	301	2719	S359	-9586.5	301
1481	S1555	4031.5	391	2720	S358	-9597.5	391
1482	S1554	4020.5	211	2721	S357	-9608.5	211
1483	S1553	4009.5	301	2722	S356	-9619.5	301

1484	S1552	3998.5	391	2723	S355	-9630.5	391
1485	S1551	3987.5	211	2724	S354	-9641.5	211
1486	S1550	3976.5	301	2725	S353	-9652.5	301
1487	S1549	3965.5	391	2726	S352	-9663.5	391
1488	S1548	3954.5	211	2727	S351	-9674.5	211
1489	S1547	3943.5	301	2728	S350	-9685.5	301
1490	S1546	3932.5	391	2729	S349	-9696.5	391
1491	S1545	3921.5	211	2730	S348	-9707.5	211
1492	S1544	3910.5	301	2731	S347	-9718.5	301
1493	S1543	3899.5	391	2732	S346	-9729.5	391
1494	S1542	3888.5	211	2733	S345	-9740.5	211
1495	S1541	3877.5	301	2734	S344	-9751.5	301
1496	S1540	3866.5	391	2735	S343	-9762.5	391
1497	S1539	3855.5	211	2736	S342	-9773.5	211
1498	S1538	3844.5	301	2737	S341	-9784.5	301
1499	S1537	3833.5	391	2738	S340	-9795.5	391
1500	S1536	3822.5	211	2739	S339	-9806.5	211
1501	S1535	3811.5	301	2740	S338	-9817.5	301
1502	S1534	3800.5	391	2741	S337	-9828.5	391
1503	S1533	3789.5	211	2742	S336	-9839.5	211
1504	S1532	3778.5	301	2743	S335	-9850.5	301
1505	S1531	3767.5	391	2744	S334	-9861.5	391
1506	S1530	3756.5	211	2745	S333	-9872.5	211
1507	S1529	3745.5	301	2746	S332	-9883.5	301
1508	S1528	3734.5	391	2747	S331	-9894.5	391
1509	S1527	3723.5	211	2748	S330	-9905.5	211
1510	S1526	3712.5	301	2749	S329	-9916.5	301
1511	S1525	3701.5	391	2750	S328	-9927.5	391
1512	S1524	3690.5	211	2751	S327	-9938.5	211
1513	S1523	3679.5	301	2752	S326	-9949.5	301
1514	S1522	3668.5	391	2753	S325	-9960.5	391
1515	S1521	3657.5	211	2754	S324	-9971.5	211
1516	S1520	3646.5	301	2755	S323	-9982.5	301
1517	S1519	3635.5	391	2756	S322	-9993.5	391
1518	S1518	3624.5	211	2757	S321	-10004.5	211
1519	S1517	3613.5	301	2758	S320	-10015.5	301
1520	S1516	3602.5	391	2759	S319	-10026.5	391
1521	S1515	3591.5	211	2760	S318	-10037.5	211
1522	S1514	3580.5	301	2761	S317	-10048.5	301
1523	S1513	3569.5	391	2762	S316	-10059.5	391

1524	S1512	3558.5	211	2763	S315	-10070.5	211
1525	S1511	3547.5	301	2764	S314	-10081.5	301
1526	S1510	3536.5	391	2765	S313	-10092.5	391
1527	S1509	3525.5	211	2766	S312	-10103.5	211
1528	S1508	3514.5	301	2767	S311	-10114.5	301
1529	S1507	3503.5	391	2768	S310	-10125.5	391
1530	S1506	3492.5	211	2769	S309	-10136.5	211
1531	S1505	3481.5	301	2770	S308	-10147.5	301
1532	S1504	3470.5	391	2771	S307	-10158.5	391
1533	S1503	3459.5	211	2772	S306	-10169.5	211
1534	S1502	3448.5	301	2773	S305	-10180.5	301
1535	S1501	3437.5	391	2774	S304	-10191.5	391
1536	S1500	3426.5	211	2775	S303	-10202.5	211
1537	S1499	3415.5	301	2776	S302	-10213.5	301
1538	S1498	3404.5	391	2777	S301	-10224.5	391
1539	S1497	3393.5	211	2778	S300	-10235.5	211
1540	S1496	3382.5	301	2779	S299	-10246.5	301
1541	S1495	3371.5	391	2780	S298	-10257.5	391
1542	S1494	3360.5	211	2781	S297	-10268.5	211
1543	S1493	3349.5	301	2782	S296	-10279.5	301
1544	S1492	3338.5	391	2783	S295	-10290.5	391
1545	S1491	3327.5	211	2784	S294	-10301.5	211
1546	S1490	3316.5	301	2785	S293	-10312.5	301
1547	S1489	3305.5	391	2786	S292	-10323.5	391
1548	S1488	3294.5	211	2787	S291	-10334.5	211
1549	S1487	3283.5	301	2788	S290	-10345.5	301
1550	S1486	3272.5	391	2789	S289	-10356.5	391
1551	S1485	3261.5	211	2790	S288	-10367.5	211
1552	S1484	3250.5	301	2791	S287	-10378.5	301
1553	S1483	3239.5	391	2792	S286	-10389.5	391
1554	S1482	3228.5	211	2793	S285	-10400.5	211
1555	S1481	3217.5	301	2794	S284	-10411.5	301
1556	S1480	3206.5	391	2795	S283	-10422.5	391
1557	S1479	3195.5	211	2796	S282	-10433.5	211
1558	S1478	3184.5	301	2797	S281	-10444.5	301
1559	S1477	3173.5	391	2798	S280	-10455.5	391
1560	S1476	3162.5	211	2799	S279	-10466.5	211
1561	S1475	3151.5	301	2800	S278	-10477.5	301
1562	S1474	3140.5	391	2801	S277	-10488.5	391
1563	S1473	3129.5	211	2802	S276	-10499.5	211

1564	S1472	3118.5	301	2803	S275	-10510.5	301
1565	S1471	3107.5	391	2804	S274	-10521.5	391
1566	S1470	3096.5	211	2805	S273	-10532.5	211
1567	S1469	3085.5	301	2806	S272	-10543.5	301
1568	S1468	3074.5	391	2807	S271	-10554.5	391
1569	S1467	3063.5	211	2808	S270	-10565.5	211
1570	S1466	3052.5	301	2809	S269	-10576.5	301
1571	S1465	3041.5	391	2810	S268	-10587.5	391
1572	S1464	3030.5	211	2811	S267	-10598.5	211
1573	S1463	3019.5	301	2812	S266	-10609.5	301
1574	S1462	3008.5	391	2813	S265	-10620.5	391
1575	S1461	2997.5	211	2814	S264	-10631.5	211
1576	S1460	2986.5	301	2815	S263	-10642.5	301
1577	S1459	2975.5	391	2816	S262	-10653.5	391
1578	S1458	2964.5	211	2817	S261	-10664.5	211
1579	S1457	2953.5	301	2818	S260	-10675.5	301
1580	S1456	2942.5	391	2819	S259	-10686.5	391
1581	S1455	2931.5	211	2820	S258	-10697.5	211
1582	S1454	2920.5	301	2821	S257	-10708.5	301
1583	S1453	2909.5	391	2822	S256	-10719.5	391
1584	S1452	2898.5	211	2823	S255	-10730.5	211
1585	S1451	2887.5	301	2824	S254	-10741.5	301
1586	S1450	2876.5	391	2825	S253	-10752.5	391
1587	S1449	2865.5	211	2826	S252	-10763.5	211
1588	S1448	2854.5	301	2827	S251	-10774.5	301
1589	S1447	2843.5	391	2828	S250	-10785.5	391
1590	S1446	2832.5	211	2829	S249	-10796.5	211
1591	S1445	2821.5	301	2830	S248	-10807.5	301
1592	S1444	2810.5	391	2831	S247	-10818.5	391
1593	S1443	2799.5	211	2832	S246	-10829.5	211
1594	S1442	2788.5	301	2833	S245	-10840.5	301
1595	S1441	2777.5	391	2834	S244	-10851.5	391
1596	S1440	2766.5	211	2835	S243	-10862.5	211
1597	S1439	2755.5	301	2836	S242	-10873.5	301
1598	S1438	2744.5	391	2837	S241	-10884.5	391
1599	S1437	2733.5	211	2838	S240	-10895.5	211
1600	S1436	2722.5	301	2839	S239	-10906.5	301
1601	S1435	2711.5	391	2840	S238	-10917.5	391
1602	S1434	2700.5	211	2841	S237	-10928.5	211
1603	S1433	2689.5	301	2842	S236	-10939.5	301

1604	S1432	2678.5	391	2843	S235	-10950.5	391
1605	S1431	2667.5	211	2844	S234	-10961.5	211
1606	S1430	2656.5	301	2845	S233	-10972.5	301
1607	S1429	2645.5	391	2846	S232	-10983.5	391
1608	S1428	2634.5	211	2847	S231	-10994.5	211
1609	S1427	2623.5	301	2848	S230	-11005.5	301
1610	S1426	2612.5	391	2849	S229	-11016.5	391
1611	S1425	2601.5	211	2850	S228	-11027.5	211
1612	S1424	2590.5	301	2851	S227	-11038.5	301
1613	S1423	2579.5	391	2852	S226	-11049.5	391
1614	S1422	2568.5	211	2853	S225	-11060.5	211
1615	S1421	2557.5	301	2854	S224	-11071.5	301
1616	S1420	2546.5	391	2855	S223	-11082.5	391
1617	S1419	2535.5	211	2856	S222	-11093.5	211
1618	S1418	2524.5	301	2857	S221	-11104.5	301
1619	S1417	2513.5	391	2858	S220	-11115.5	391
1620	S1416	2502.5	211	2859	S219	-11126.5	211
1621	S1415	2491.5	301	2860	S218	-11137.5	301
1622	S1414	2480.5	391	2861	S217	-11148.5	391
1623	S1413	2469.5	211	2862	S216	-11159.5	211
1624	S1412	2458.5	301	2863	S215	-11170.5	301
1625	S1411	2447.5	391	2864	S214	-11181.5	391
1626	S1410	2436.5	211	2865	S213	-11192.5	211
1627	S1409	2425.5	301	2866	S212	-11203.5	301
1628	S1408	2414.5	391	2867	S211	-11214.5	391
1629	S1407	2403.5	211	2868	S210	-11225.5	211
1630	S1406	2392.5	301	2869	S209	-11236.5	301
1631	S1405	2381.5	391	2870	S208	-11247.5	391
1632	S1404	2370.5	211	2871	S207	-11258.5	211
1633	S1403	2359.5	301	2872	S206	-11269.5	301
1634	S1402	2348.5	391	2873	S205	-11280.5	391
1635	S1401	2337.5	211	2874	S204	-11291.5	211
1636	S1400	2326.5	301	2875	S203	-11302.5	301
1637	S1399	2315.5	391	2876	S202	-11313.5	391
1638	S1398	2304.5	211	2877	S201	-11324.5	211
1639	S1397	2293.5	301	2878	S200	-11335.5	301
1640	S1396	2282.5	391	2879	S199	-11346.5	391
1641	S1395	2271.5	211	2880	S198	-11357.5	211
1642	S1394	2260.5	301	2881	S197	-11368.5	301
1643	S1393	2249.5	391	2882	S196	-11379.5	391

1644	S1392	2238.5	211	2883	S195	-11390.5	211
1645	S1391	2227.5	301	2884	S194	-11401.5	301
1646	S1390	2216.5	391	2885	S193	-11412.5	391
1647	S1389	2205.5	211	2886	S192	-11423.5	211
1648	S1388	2194.5	301	2887	S191	-11434.5	301
1649	S1387	2183.5	391	2888	S190	-11445.5	391
1650	S1386	2172.5	211	2889	S189	-11456.5	211
1651	S1385	2161.5	301	2890	S188	-11467.5	301
1652	S1384	2150.5	391	2891	S187	-11478.5	391
1653	S1383	2139.5	211	2892	S186	-11489.5	211
1654	S1382	2128.5	301	2893	S185	-11500.5	301
1655	S1381	2117.5	391	2894	S184	-11511.5	391
1656	S1380	2106.5	211	2895	S183	-11522.5	211
1657	S1379	2095.5	301	2896	S182	-11533.5	301
1658	S1378	2084.5	391	2897	S181	-11544.5	391
1659	S1377	2073.5	211	2898	S180	-11555.5	211
1660	S1376	2062.5	301	2899	S179	-11566.5	301
1661	S1375	2051.5	391	2900	S178	-11577.5	391
1662	S1374	2040.5	211	2901	S177	-11588.5	211
1663	S1373	2029.5	301	2902	S176	-11599.5	301
1664	S1372	2018.5	391	2903	S175	-11610.5	391
1665	S1371	2007.5	211	2904	S174	-11621.5	211
1666	S1370	1996.5	301	2905	S173	-11632.5	301
1667	S1369	1985.5	391	2906	S172	-11643.5	391
1668	S1368	1974.5	211	2907	S171	-11654.5	211
1669	S1367	1963.5	301	2908	S170	-11665.5	301
1670	S1366	1952.5	391	2909	S169	-11676.5	391
1671	S1365	1941.5	211	2910	S168	-11687.5	211
1672	S1364	1930.5	301	2911	S167	-11698.5	301
1673	S1363	1919.5	391	2912	S166	-11709.5	391
1674	S1362	1908.5	211	2913	S165	-11720.5	211
1675	S1361	1897.5	301	2914	S164	-11731.5	301
1676	S1360	1886.5	391	2915	S163	-11742.5	391
1677	S1359	1875.5	211	2916	S162	-11753.5	211
1678	S1358	1864.5	301	2917	S161	-11764.5	301
1679	S1357	1853.5	391	2918	S160	-11775.5	391
1680	S1356	1842.5	211	2919	S159	-11786.5	211
1681	S1355	1831.5	301	2920	S158	-11797.5	301
1682	S1354	1820.5	391	2921	S157	-11808.5	391
1683	S1353	1809.5	211	2922	S156	-11819.5	211

1684	S1352	1798.5	301	2923	S155	-11830.5	301
1685	S1351	1787.5	391	2924	S154	-11841.5	391
1686	S1350	1776.5	211	2925	S153	-11852.5	211
1687	S1349	1765.5	301	2926	S152	-11863.5	301
1688	S1348	1754.5	391	2927	S151	-11874.5	391
1689	S1347	1743.5	211	2928	S150	-11885.5	211
1690	S1346	1732.5	301	2929	S149	-11896.5	301
1691	S1345	1721.5	391	2930	S148	-11907.5	391
1692	S1344	1710.5	211	2931	S147	-11918.5	211
1693	S1343	1699.5	301	2932	S146	-11929.5	301
1694	S1342	1688.5	391	2933	S145	-11940.5	391
1695	S1341	1677.5	211	2934	S144	-11951.5	211
1696	S1340	1666.5	301	2935	S143	-11962.5	301
1697	S1339	1655.5	391	2936	S142	-11973.5	391
1698	S1338	1644.5	211	2937	S141	-11984.5	211
1699	S1337	1633.5	301	2938	S140	-11995.5	301
1700	S1336	1622.5	391	2939	S139	-12006.5	391
1701	S1335	1611.5	211	2940	S138	-12017.5	211
1702	S1334	1600.5	301	2941	S137	-12028.5	301
1703	S1333	1589.5	391	2942	S136	-12039.5	391
1704	S1332	1578.5	211	2943	S135	-12050.5	211
1705	S1331	1567.5	301	2944	S134	-12061.5	301
1706	S1330	1556.5	391	2945	S133	-12072.5	391
1707	S1329	1545.5	211	2946	S132	-12083.5	211
1708	S1328	1534.5	301	2947	S131	-12094.5	301
1709	S1327	1523.5	391	2948	S130	-12105.5	391
1710	S1326	1512.5	211	2949	S129	-12116.5	211
1711	S1325	1501.5	301	2950	S128	-12127.5	301
1712	S1324	1490.5	391	2951	S127	-12138.5	391
1713	S1323	1479.5	211	2952	S126	-12149.5	211
1714	S1322	1468.5	301	2953	S125	-12160.5	301
1715	S1321	1457.5	391	2954	S124	-12171.5	391
1716	S1320	1446.5	211	2955	S123	-12182.5	211
1717	S1319	1435.5	301	2956	S122	-12193.5	301
1718	S1318	1424.5	391	2957	S121	-12204.5	391
1719	S1317	1413.5	211	2958	S120	-12215.5	211
1720	S1316	1402.5	301	2959	S119	-12226.5	301
1721	S1315	1391.5	391	2960	S118	-12237.5	391
1722	S1314	1380.5	211	2961	S117	-12248.5	211
1723	S1313	1369.5	301	2962	S116	-12259.5	301

1724	S1312	1358.5	391	2963	S115	-12270.5	391
1725	S1311	1347.5	211	2964	S114	-12281.5	211
1726	S1310	1336.5	301	2965	S113	-12292.5	301
1727	S1309	1325.5	391	2966	S112	-12303.5	391
1728	S1308	1314.5	211	2967	S111	-12314.5	211
1729	S1307	1303.5	301	2968	S110	-12325.5	301
1730	S1306	1292.5	391	2969	S109	-12336.5	391
1731	S1305	1281.5	211	2970	S108	-12347.5	211
1732	S1304	1270.5	301	2971	S107	-12358.5	301
1733	S1303	1259.5	391	2972	S106	-12369.5	391
1734	S1302	1248.5	211	2973	S105	-12380.5	211
1735	S1301	1237.5	301	2974	S104	-12391.5	301
1736	S1300	1226.5	391	2975	S103	-12402.5	391
1737	S1299	1215.5	211	2976	S102	-12413.5	211
1738	S1298	1204.5	301	2977	S101	-12424.5	301
1739	S1297	1193.5	391	2978	S100	-12435.5	391
1740	S1296	1182.5	211	2979	S99	-12446.5	211
1741	S1295	1171.5	301	2980	S98	-12457.5	301
1742	S1294	1160.5	391	2981	S97	-12468.5	391
1743	S1293	1149.5	211	2982	S96	-12479.5	211
1744	S1292	1138.5	301	2983	S95	-12490.5	301
1745	S1291	1127.5	391	2984	S94	-12501.5	391
1746	S1290	1116.5	211	2985	S93	-12512.5	211
1747	S1289	1105.5	301	2986	S92	-12523.5	301
1748	S1288	1094.5	391	2987	S91	-12534.5	391
1749	S1287	1083.5	211	2988	S90	-12545.5	211
1750	S1286	1072.5	301	2989	S89	-12556.5	301
1751	S1285	1061.5	391	2990	S88	-12567.5	391
1752	S1284	1050.5	211	2991	S87	-12578.5	211
1753	S1283	1039.5	301	2992	S86	-12589.5	301
1754	S1282	1028.5	391	2993	S85	-12600.5	391
1755	S1281	1017.5	211	2994	S84	-12611.5	211
1756	S1280	1006.5	301	2995	S83	-12622.5	301
1757	S1279	995.5	391	2996	S82	-12633.5	391
1758	S1278	984.5	211	2997	S81	-12644.5	211
1759	S1277	973.5	301	2998	S80	-12655.5	301
1760	S1276	962.5	391	2999	S79	-12666.5	391
1761	S1275	951.5	211	3000	S78	-12677.5	211
1762	S1274	940.5	301	3001	S77	-12688.5	301
1763	S1273	929.5	391	3002	S76	-12699.5	391

1764	S1272	918.5	211	3003	S75	-12710.5	211
1765	S1271	907.5	301	3004	S74	-12721.5	301
1766	S1270	896.5	391	3005	S73	-12732.5	391
1767	S1269	885.5	211	3006	S72	-12743.5	211
1768	S1268	874.5	301	3007	S71	-12754.5	301
1769	S1267	863.5	391	3008	S70	-12765.5	391
1770	S1266	852.5	211	3009	S69	-12776.5	211
1771	S1265	841.5	301	3010	S68	-12787.5	301
1772	S1264	830.5	391	3011	S67	-12798.5	391
1773	S1263	819.5	211	3012	S66	-12809.5	211
1774	S1262	808.5	301	3013	S65	-12820.5	301
1775	S1261	797.5	391	3014	S64	-12831.5	391
1776	S1260	786.5	211	3015	S63	-12842.5	211
1777	S1259	775.5	301	3016	S62	-12853.5	301
1778	S1258	764.5	391	3017	S61	-12864.5	391
1779	S1257	753.5	211	3018	S60	-12875.5	211
1780	S1256	742.5	301	3019	S59	-12886.5	301
1781	S1255	731.5	391	3020	S58	-12897.5	391
1782	S1254	720.5	211	3021	S57	-12908.5	211
1783	S1253	709.5	301	3022	S56	-12919.5	301
1784	S1252	698.5	391	3023	S55	-12930.5	391
1785	S1251	687.5	211	3024	S54	-12941.5	211
1786	S1250	676.5	301	3025	S53	-12952.5	301
1787	S1249	665.5	391	3026	S52	-12963.5	391
1788	S1248	654.5	211	3027	S51	-12974.5	211
1789	S1247	643.5	301	3028	S50	-12985.5	301
1790	S1246	632.5	391	3029	S49	-12996.5	391
1791	S1245	621.5	211	3030	S48	-13007.5	211
1792	S1244	610.5	301	3031	S47	-13018.5	301
1793	S1243	599.5	391	3032	S46	-13029.5	391
1794	S1242	588.5	211	3033	S45	-13040.5	211
1795	S1241	577.5	301	3034	S44	-13051.5	301
1796	S1240	566.5	391	3035	S43	-13062.5	391
1797	S1239	555.5	211	3036	S42	-13073.5	211
1798	S1238	544.5	301	3037	S41	-13084.5	301
1799	S1237	533.5	391	3038	S40	-13095.5	391
1800	S1236	522.5	211	3039	S39	-13106.5	211
1801	S1235	511.5	301	3040	S38	-13117.5	301
1802	S1234	500.5	391	3041	S37	-13128.5	391
1803	S1233	489.5	211	3042	S36	-13139.5	211

1804	S1232	478.5	301	3043	S35	-13150.5	301
1805	S1231	467.5	391	3044	S34	-13161.5	391
1806	S1230	456.5	211	3045	S33	-13172.5	211
1807	S1229	445.5	301	3046	S32	-13183.5	301
1808	S1228	434.5	391	3047	S31	-13194.5	391
1809	S1227	423.5	211	3048	S30	-13205.5	211
1810	S1226	412.5	301	3049	S29	-13216.5	301
1811	S1225	401.5	391	3050	S28	-13227.5	391
1812	S1224	390.5	211	3051	S27	-13238.5	211
1813	S1223	379.5	301	3052	S26	-13249.5	301
1814	S1222	368.5	391	3053	S25	-13260.5	391
1815	S1221	357.5	211	3054	S24	-13271.5	211
1816	S1220	346.5	301	3055	S23	-13282.5	301
1817	S1219	335.5	391	3056	S22	-13293.5	391
1818	S1218	324.5	211	3057	S21	-13304.5	211
1819	S1217	313.5	301	3058	S20	-13315.5	301
1820	S1216	302.5	391	3059	S19	-13326.5	391
1821	S1215	291.5	211	3060	S18	-13337.5	211
1822	S1214	280.5	301	3061	S17	-13348.5	301
1823	S1213	269.5	391	3062	S16	-13359.5	391
1824	S1212	258.5	211	3063	S15	-13370.5	211
1825	S1211	247.5	301	3064	S14	-13381.5	301
1826	S1210	236.5	391	3065	S13	-13392.5	391
1827	S1209	225.5	211	3066	S12	-13403.5	211
1828	S1208	214.5	301	3067	S11	-13414.5	301
1829	S1207	203.5	391	3068	S10	-13425.5	391
1830	S1206	192.5	211	3069	S9	-13436.5	211
1831	S1205	181.5	301	3070	S8	-13447.5	301
1832	S1204	170.5	391	3071	S7	-13458.5	391
1833	S1203	159.5	211	3072	S6	-13469.5	211
1834	S1202	148.5	301	3073	S5	-13480.5	301
1835	S1201	137.5	391	3074	S4	-13491.5	391
1836	DUMMY	126.5	211	3075	S3	-13502.5	211
1837	DUMMY	115.5	301	3076	S2	-13513.5	301
1838	DUMMY	104.5	391	3077	S1	-13524.5	391
1839	DUMMY	93.5	211	3078	SL1	-13535.5	211
1840	DUMMY	82.5	301	3079	DUMMY	-13546.5	301
1841	DUMMY	71.5	391	3080	DUMMY	-13557.5	391
1842	DUMMY	60.5	211	3081	DUMMY	-13568.5	211
1843	DUMMY	49.5	301	3082	DUMMY	-13579.5	301

1844	DUMMY	38.5	391	3083	DUMMY	-13590.5	391
1845	DUMMY	27.5	211	3084	DUMMY	-13601.5	211
1846	DUMMY	16.5	301	3085	DUMMY	-13612.5	301
1847	DUMMY	5.5	391	3086	DUMMY	-13623.5	391

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Revision History

Version	Revisions	Date	Modified by
0.1	First draft.	2014-04-20	Yipin Huang
0.2	Modified Command 2	2015-08	Yipin Huang
0.3	Modified pad location information and description of command 2 functions.	2017/04/17	Yipin Huang
0.4	Modified the part number from ICN9706 to ICNL9706	2017/07/06	Yipin Huang
0.5	Modified application circuit and table of max layout resistance	2017/08/07	Yipin Huang
0.6	Notice option cap of application circuit	2017/10/19	Yipin Huang
0.7	Modify OTP flow Modified application circuit	2017/10/26	Dean Hsu