CHIPONE
集创北方

*ICNT86x2 series Capacitive Touch IC Specifications for Tablet*

# *ICNT8672, ICNT8682, ICNT8692*

*Model No :* *ICNT86x2*

*Document Version :* *V1.0*

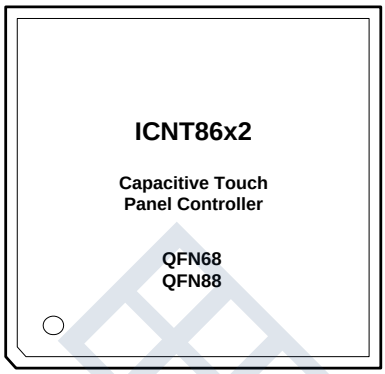
*Release Date :* *2015/12/14*



*Chipone Technology (Beijing) Co.,Ltd.*

# Index

# Features




- ✧ Combine mutual capacitive and self capacitive sensing techniques
- ✧ Support Glass/Film DITO and SITO, OGS
- ✧ Support Single-Layer Multi-Touch Glass & Film ITO sensor
- ✧ Support $I^2C$ interface to communicate with host processor, ICNT8672/ICNT8692 also support SPI interface
- ✧ Built-in MCU and DSP with 48KB of internal flash, 4KB of data SRAM
- ✧ 4 operating modes
  - ■ Active
  - ■ Monitor
  - ■ Hibernate
  - ■ Gesture
- ✧ Support $I^2C$ and Gestural wake
- ✧ Operating voltage 2.8 to 3.3V.
- ✧ Support 1.8V/3.3V digital IOVCC.
- ✧ $I^2C$ interface (up to 400kbps)
- ✧ 4 wire SPI slave interface ( up to 10 MHz) for configuration
- ✧ User-Programmable scan sequences
- ✧ Programmable capacitance resolution
- ✧ Large dynamic range of ADC
- ✧ Insensitive to environmental variations and touch variations
- ✧ Auto calibration.
- ✧ Auto Frequency-Hopping.

# 1、Description

ICNT86x2 series IC are the low power, general purpose capacitive controller with a built–in 32bit MCU with 48KB flash, the high performance ADC and digital filters. By using the mutual capacitance technique, ICNT86x2 support true multi-touch capability. In conjunction with a mutual capacitive or self-capacitive touch panel, the ICNT86x2 provide user-friendly input functions, which could be applied on many portable devices, especially for the tablets.

The ICNT86x2 series IC include ICNT8672/ICNT8682/ICNT8692; the difference between their specifications will be listed individually in this datasheet.

# 2、Typical Application

ICNT86x2 accommodates a wide range of applications with a multi-touch sensing device.

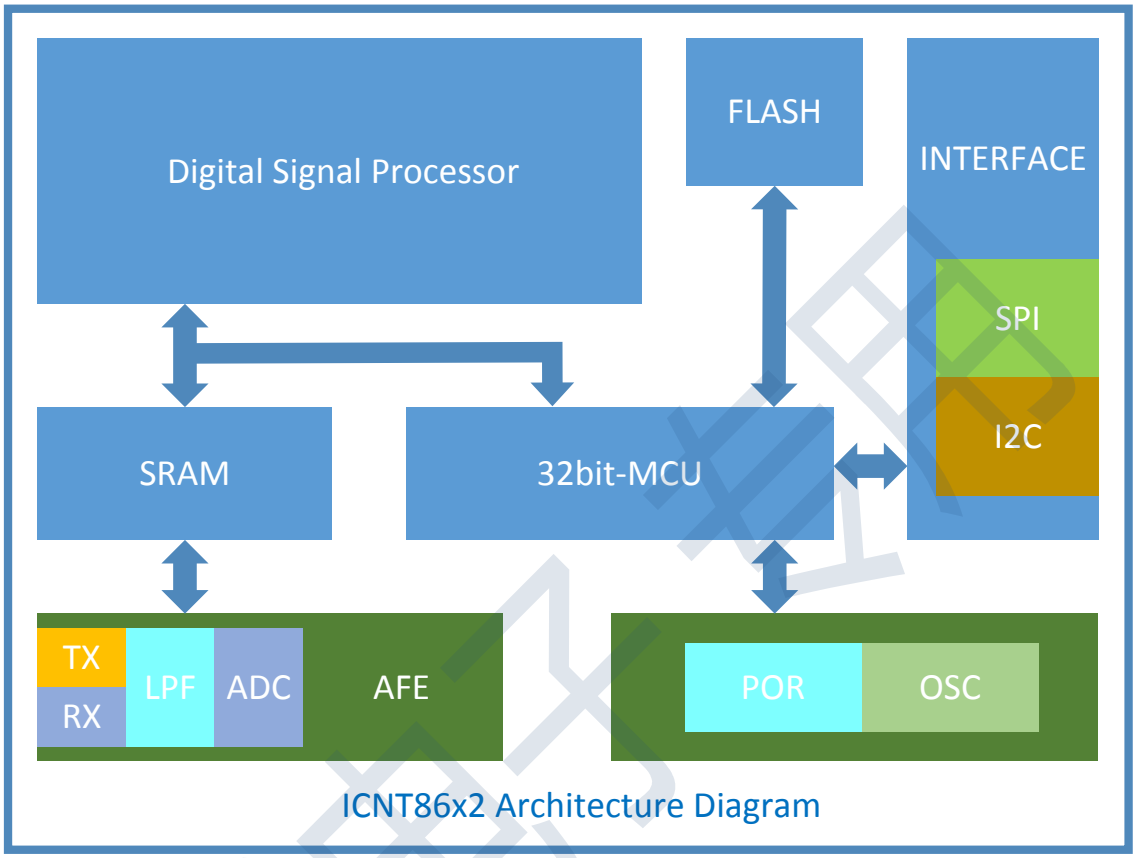
- Tablets
- Portable MP3 and MP4 media players
- Digital cameras
- Game consoles
- Navigation systems
- Information kiosks
- Keyboard, keypad, mouse, remote control
- House appliances
- Home entertainment devices

ICNT86x2 Series IC support 7”~12.1” touch panel, users may find out their target IC from the specs listed as follows.

| Model Name | Channels | | Package | | | Touch Panel Size |
|---|---|---|---|---|---|---|
| | TX | RX | Type | Pin | Size | |
| ICNT8672 | 28TX*19RX<br>29TX*18RX<br>30TX*17RX | | QFN | 68 | 8*8 | 7” ~ 9” |
| ICNT8682 | 32TX*24RX<br>33TX*23RX<br>34TX*22RX<br>35TX*21RX<br>36TX*20RX | | QFN | 68 | 8*8 | 7” ~ 10.1” |
| ICNT8692 | 42TX*30RX | | QFN | 88 | 10*10 | 8” ~ 12.1” |

# 3、Functional Description

## 3.1、Block Diagram




ICNT86x2 Architecture Diagram

ICNT86x2 can be divided into the following functional blocks:

- Touch Panel Interface
  The channel signal is converted by ADC to the digital signal.
- Data Memory
  Touch panel data buffer
- MCU
  32-bit MCU core with 48KB internal flash, 4KB data SRAM
- Watch Dog Timer
  To guarantee the robustness of the chip.
- Voltage Regulator
  To generate voltage for internal modules from the input VCC supply.
- Flash
  Program codes storage
- External Interface
  - $I^2C$/SPI: interface for system control and data transfer
  - INT/WAKE: interrupt signal to inform the host processor that touch data is ready or wakeup request for the host to change ICNT86x2 from hibernate to active mode
  - /RST: external signal to reset the chip, active low

## 3.2、Serial Interface(I²C)

There are 2 modes for I²C operation, single byte modes and multi-byte modes. Under single mode, MCU will enter interrupt service routine by every byte transaction, while under multi-byte mode, MCU could enter interrupt service routine only once after internal 8 bytes FIFO is empty or full. The latter will increase the throughput of whole system.

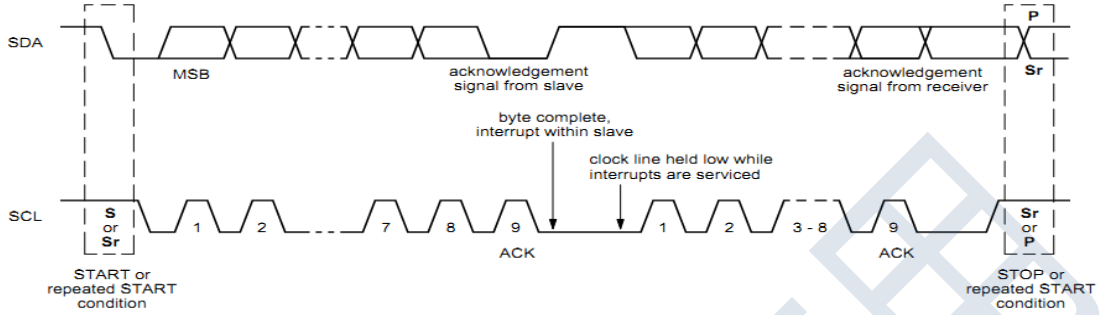



**Figure 3-1 I²C Signal Description**

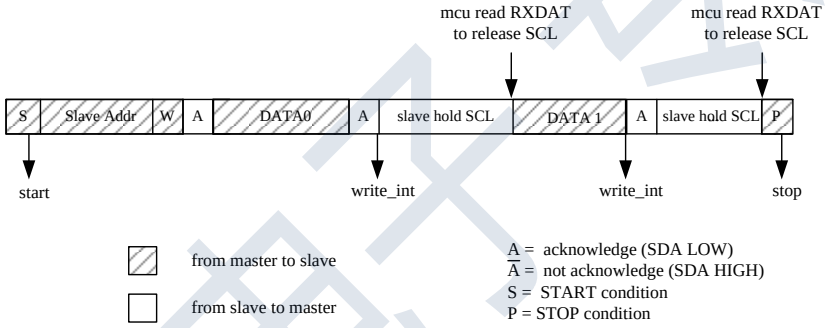



**Figure 3-2 I²C single byte write operation**

Figure 3-2 above illustrates the single byte write transaction scenario. The I²C start / stop interrupt occurs at the start and stop stage to notify MCU the protocol status. And there will be a write interrupt to notify MCU after I²C master writes each byte to slave. Before MCU reads RXDAT, the SCL will be held automatically.

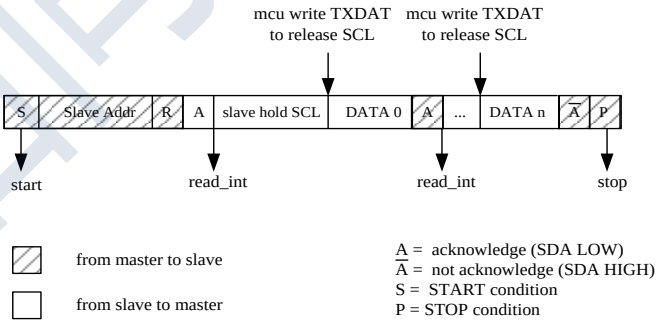



**Figure 3-3 I²C single byte read operation**

Figure 3-3 above illustrates the single byte read transaction scenario. The I²C start / stop interrupt occurs at the start and stop stage to notify MCU the protocol status. And there will be a read interrupt to notify MCU before I²C master fetches expected data from slave. Before MCU writes TXDAT, the SCL will be held automatically. The last NAK before stop will not trigger read interrupt.

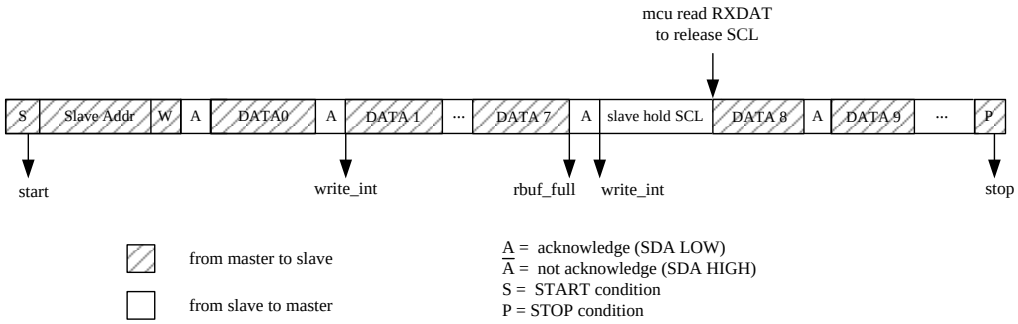



**Figure 3-4 I²C multi-byte write operation**

Figure 3-4 above illustrates the multi-byte write transaction scenario. There are 8 bytes receive FIFO in I²C slave controller. When I²C slave is configured into multi-byte mode, the SCL will be held by slave only if the receiving FIFO is full and a rbuf_full interrupt will be triggered to notify MCU. After MCU reads RXDAT, the SCL will be released to -receive new data.

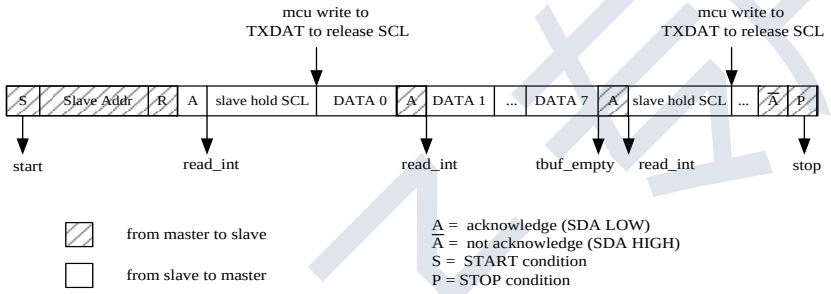



**Figure 3-5 I²C multi-byte read operation**

Figure 3-5 above illustrates the multi-byte read transaction scenario. There are 8 bytes transmission FIFO in the I²C slave controller. When I²C slave is configured into multi-byte mode, the SCL will be held by the slave only if the transmit FIFO is empty and a tbuf_empty interrupt will be triggered to notify MCU. After MCU writes new data to TXDAT, the SCL will be released for new transaction.

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $F_{SCL}$ | SCL clock frequency | | 400 | kHz |
| $T_{LOW}$ | Low period of SCL clock | 1.3 | | μs |
| $T_{HIGH}$ | High period of SCL clock | 0.6 | | μs |
| $T_{SU\_STA}$ | Set-up time for a repeated start | 0.6 | | μs |
| $T_{HD\_STA}$ | Hold time (repeated) start condition. | 0.6 | | μs |
| $T_{SU\_DAT}$ | Data set-up time | 0.1 | | μs |
| $T_{HD\_DAT}$ | Data hold time | 0.6 | 0.9 | μs |
| $T_R$ | Rise time of SDA and SCL | | 300 | ns |
| $T_F$ | Fall time of SDA and SCL | | 300 | ns |
| $T_{SU\_STO}$ | Set-up time for stop condition | 0.6 | | μs |
| $T_{BUF}$ | Bus free time between a stop and start | 1.3 | | μs |

**Table 3-1 AC Characteristics of the I²C interface**

# 4、Electrical Specifications

## 4.1、Absolute Maximum Ratings

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature with power applied | -40 | | 80 | ℃ | |
| $T_{STG}$ | Storage temperature | -45 | | 100 | ℃ | Recommend 25℃ ±25℃ |
| VDDA - VSSA | Power Supply Voltage 1 | -0.3 | | 3.6 | V | |
| VDD3 – VSS | Power Supply Voltage 2 | -0.3 | | 3.6 | V | |
| ESD | Electrostatic discharge voltage of whole chip | 2 | | | KV | HBM |

Notes

1. If used beyond the absolute maximum ratings, ICNT86x2 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA (high) ≥ VSSA (low)
3. Make sure VDD (high) ≥ VSS (low)
4. IOVCC is set to VDD3 or VDD18 by software configuration.

## 4.2、DC Electrical Characteristics

| Parameter | Description | ICNT8672 | | | ICNT8682 | | | ICNT8692 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{OPR}$ | Normal operation mode current | | 9.7 | | | 11.1 | | | 15.8 | | mA |
| $I_{MON}$ | Monitor mode current | | 3.5 | | | 4.0 | | | 5.2 | | mA |
| $I_{SUS}$ | Suspend mode current | | 167 | | | 167 | | | 167 | | μA |
| $I_{SLP}$ | Sleep mode current | | 91 | | | 91 | | | 91 | | μA |

Notes

1. The suspend mode current and the sleep mode current measured at room temperature; VCC=3.3V.
2. The suspend mode could be changed to the sleep mode by firmware configuration, and the default mode is suspend mode.

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Digital input low voltage | -0.3 | | 0.3*IOVCC | V |
| $V_{IH}$ | Digital input high voltage | 0.7*IOVCC | | IOVCC | V |
| $V_{OL}$ | Digital low output voltage | | | 0.3*IOVCC | V |
| $V_{OH}$ | Digital high output voltage | 0.7*IOVCC | | | V |
| $I_{IL}$ | Input leakage | | 1 | | nA |

## 4.3、AC Electrical Characteristics

### AC characteristics of oscillators

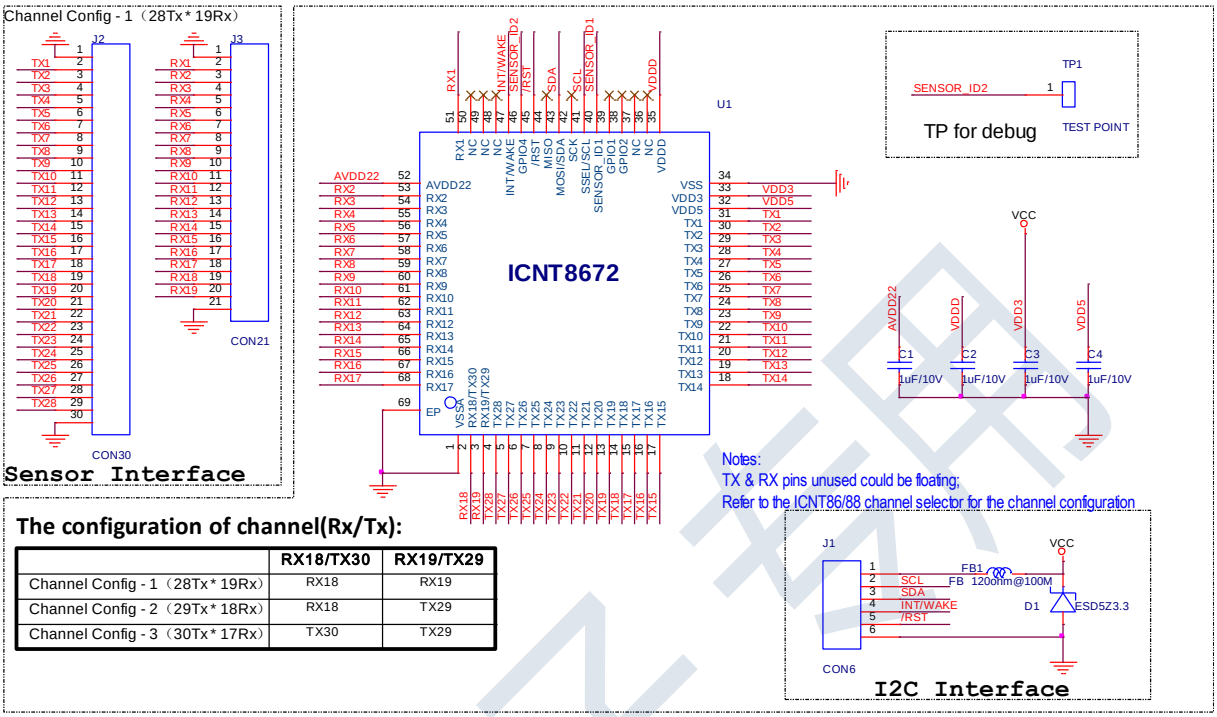
| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{OSC1}$ | Frequency of oscillator1 | | 60 | | MHz |

### AC characteristics of interface

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{TX}$ | TX acceptable clock | 30 | | 500 | kHz |

## 4.4、Circuit diagram

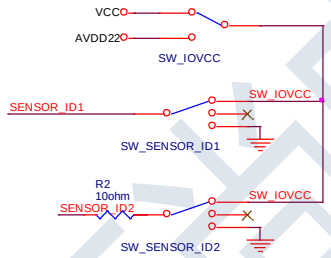
### ICNT8672




**The configuration of channel(Rx/Tx):**

| | RX18/TX30 | RX19/TX29 |
|---|---|---|
| Channel Config - 1（28Tx*19Rx） | RX18 | RX19 |
| Channel Config - 2（29Tx*18Rx） | RX18 | TX29 |
| Channel Config - 3（30Tx*17Rx） | TX30 | TX29 |

**Optional circuits as follows (necessary if the function required)**




| TP Module ID | SENSOR_ID1 | SENSOR_ID2 |
|---|---|---|
| module 1- ID : 0x00 | GND | GND |
| module 2- ID : 0x01 | SW_IOVCC | GND |
| module 3- ID : 0x02 | NC | GND |
| module 4- ID : 0x10 | GND | SW_IOVCC |
| module 5- ID : 0x11 | SW_IOVCC | SW_IOVCC |
| module 6- ID : 0x12 | NC | SW_IOVCC |
| module 7- ID : 0x20 | GND | NC |
| module 8- ID : 0x21 | SW_IOVCC | NC |
| module 9- ID : 0x22 | NC | NC |

| IO接口电压 | SW_IOVCC |
|---|---|
| 3.3V | VCC |
| 1.8V | AVDD22 |

**Notes:**
**SW_IOVCC connected to AVDD22 @ IO voltage=1.8V**
**SW_IOVCC connected to VCC @ IO voltage =3.3V**

**TP ID Recognition【Optional】**

**Notes：The LUT above used for debug and ID allocation of IDH**

Notes:Refer to the COB/COF layout guide for the design of functional circuits.

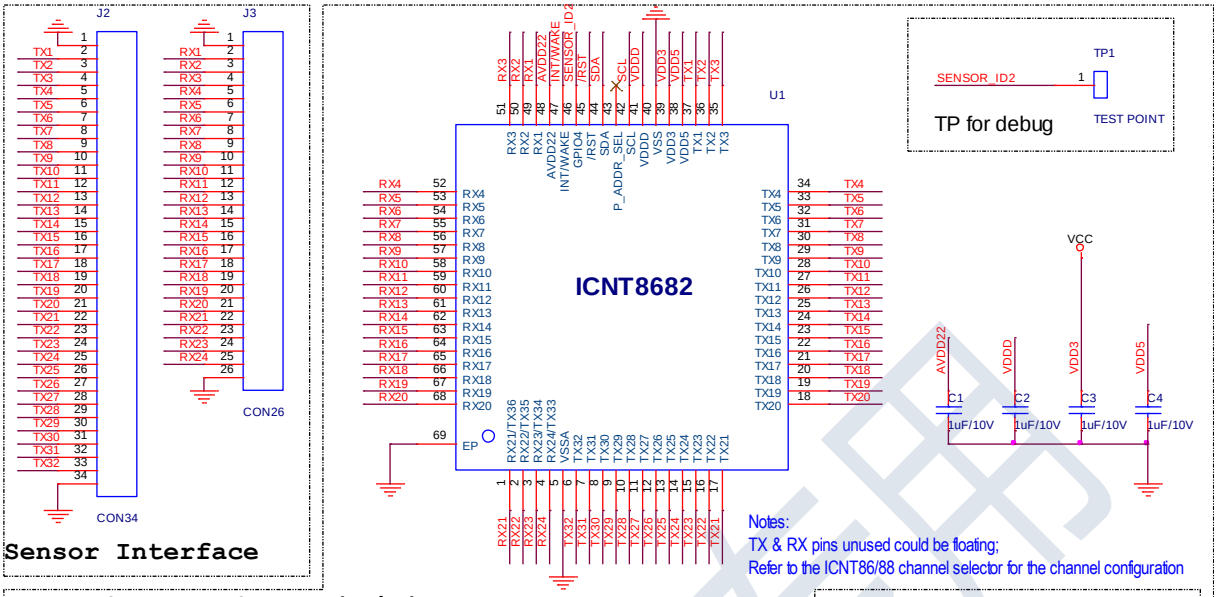
### ICNT8672 I²C Interface

## Notes

ICNT8672 supports dual frequency driving mode.

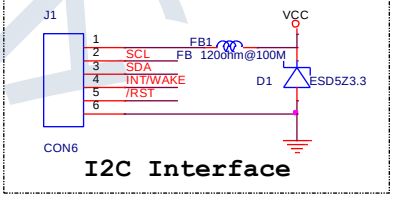
You can find guides from “ICN85xx&ICNT86xx Series COB Layout Design Rule” and “ICN85xx&ICNT86xx Series COF Layout Design Rule”.

# ICNT8682

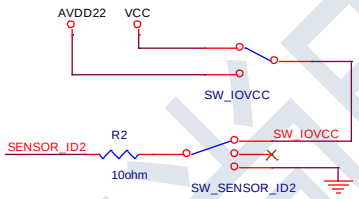



**The configuration of channel(Rx/Tx):**

| | RX21/TX36 | RX22/TX35 | RX23/TX34 | RX24/TX33 |
|---|---|---|---|---|
| Channel Config - 1（32Tx * 24Rx） | RX21 | RX22 | RX23 | RX24 |
| Channel Config - 2（33Tx * 23Rx） | RX21 | RX22 | RX23 | TX33 |
| Channel Config - 3（34Tx * 22Rx） | RX21 | RX22 | TX34 | TX33 |
| Channel Config - 4（35Tx * 21Rx） | RX21 | TX35 | TX34 | TX33 |
| Channel Config - 5（36Tx * 20Rx） | TX36 | TX35 | TX34 | TX33 |




**Optional circuits as follows (necessary if the function required)**




**TP ID Recognition【Optional】**

| TP Module ID | SENSOR_ID2 |
|---|---|
| Module 1- ID : 0x02 | GND |
| Module 2- ID : 0x12 | SW_IOVCC |
| Module 3- ID : 0x22 | NC |

**Notes：The LUT above used for debug and ID allocation of IDH**

| IO接口电压 | SW_IOVCC |
|---|---|
| 3.3V | VCC |
| 1.8V | AVDD22 |

**Notes:**
**SW_IOVCC connected to AVDD22 @ IO voltage=1.8V**
**SW_IOVCC connected to VCC @ IO voltage =3.3V**

Notes:Refer to the COB/COF layout guide for the design of functional circuits.

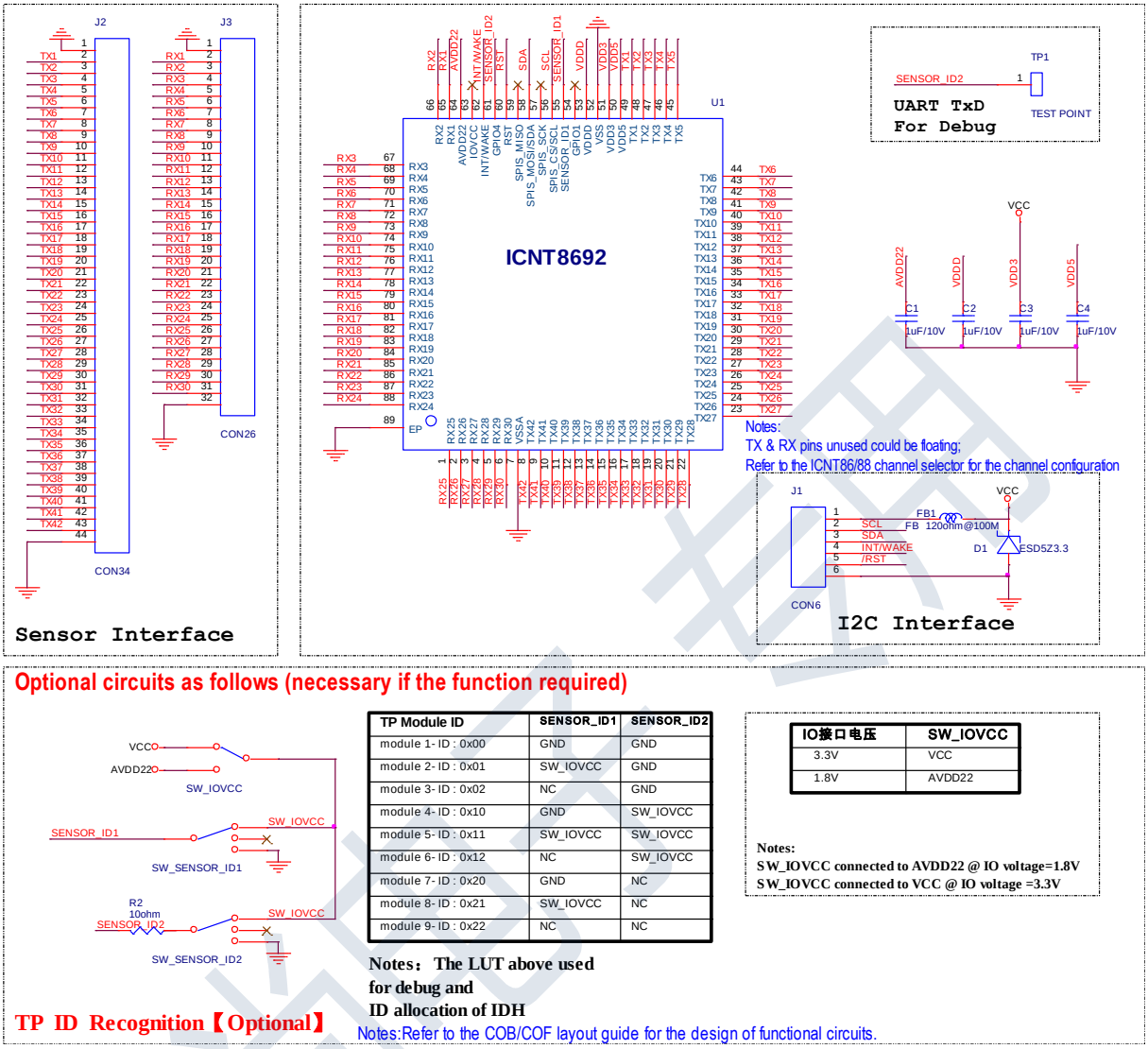
# ICNT8682 I²C Interface

## Notes

ICNT8682 supports dual frequency driving mode.

You can find guides from “ICN85xx&ICNT86xx Series COB Layout Design Rule” and “ICN85xx&ICNT86xx Series COF Layout Design Rule”.

# ICNT8692




**Optional circuits as follows (necessary if the function required)**




**TP ID Recognition【Optional】**

| TP Module ID | SENSOR_ID1 | SENSOR_ID2 |
|---|---|---|
| module 1- ID : 0x00 | GND | GND |
| module 2- ID : 0x01 | SW_IOVCC | GND |
| module 3- ID : 0x02 | NC | GND |
| module 4- ID : 0x10 | GND | SW_IOVCC |
| module 5- ID : 0x11 | SW_IOVCC | SW_IOVCC |
| module 6- ID : 0x12 | NC | SW_IOVCC |
| module 7- ID : 0x20 | GND | NC |
| module 8- ID : 0x21 | SW_IOVCC | NC |
| module 9- ID : 0x22 | NC | NC |

**Notes：The LUT above used for debug and ID allocation of IDH**

| IO接口电压 | SW_IOVCC |
|---|---|
| 3.3V | VCC |
| 1.8V | AVDD22 |

**Notes:**
**SW_IOVCC connected to AVDD22 @ IO voltage=1.8V**
**SW_IOVCC connected to VCC @ IO voltage =3.3V**

Notes:Refer to the COB/COF layout guide for the design of functional circuits.

# ICNT8692 I²C Interface

## Notes

ICNT8692 supports dual frequency driving mode.

You can find guides from “ICN85xx&ICNT86xx Series COB Layout Design Rule” and “ICN85xx&ICNT86xx Series COF Layout Design Rule”.

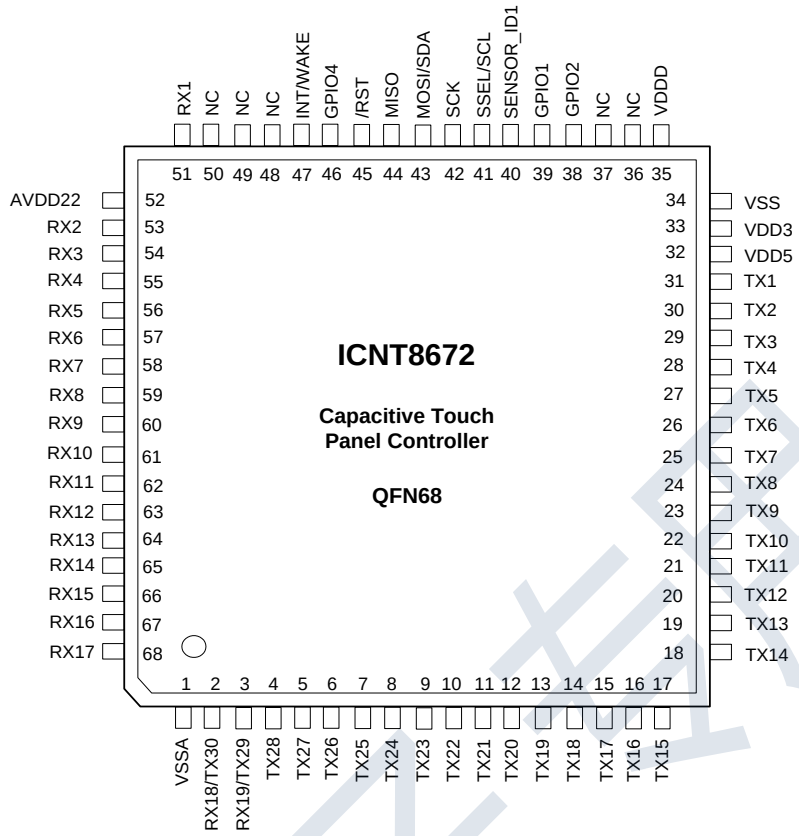
# 5、PIN DESCRIPTION

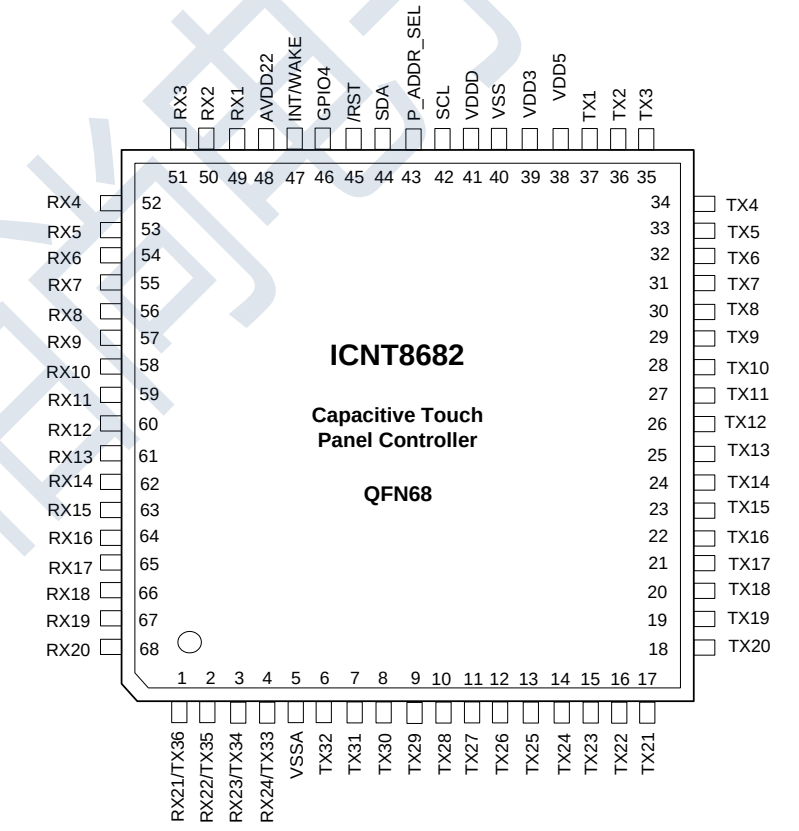
| Pin Name | Pin Num | | | Type | Description |
|---|---|---|---|---|---|
| | ICNT8672 | ICNT8682 | ICNT8692 | | |
| RX25 | | | 1 | I | Receiver input pin |
| RX26 | | | 2 | I | Receiver input pin |
| RX27 | | | 3 | I | Receiver input pin |
| RX28 | | | 4 | I | Receiver input pin |
| RX29 | | | 5 | I | Receiver input pin |
| RX30 | | | 6 | I | Receiver input pin |
| VSSA | 1 | 5 | 7 | PWR | Analog ground |
| TX42 | | | 8 | O | Transmit output pin |
| TX41 | | | 9 | O | Transmit output pin |
| TX40 | | | 10 | O | Transmit output pin |
| TX39 | | | 11 | O | Transmit output pin |
| TX38 | | | 12 | O | Transmit output pin |
| TX37 | | | 13 | O | Transmit output pin |
| TX36 | | | 14 | O | Transmit output pin |
| TX35 | | | 15 | O | Transmit output pin |
| TX34 | | | 16 | O | Transmit output pin |
| TX33 | | | 17 | O | Transmit output pin |
| TX32 | | 6 | 18 | O | Transmit output pin |
| TX31 | | 7 | 19 | O | Transmit output pin |
| TX30 | | 8 | 20 | O | Transmit output pin |
| TX29 | | 9 | 21 | O | Transmit output pin |
| TX28 | 4 | 10 | 22 | O | Transmit output pin |
| TX27 | 5 | 11 | 23 | O | Transmit output pin |
| TX26 | 6 | 12 | 24 | O | Transmit output pin |
| TX25 | 7 | 13 | 25 | O | Transmit output pin |
| TX24 | 8 | 14 | 26 | O | Transmit output pin |
| TX23 | 9 | 15 | 27 | O | Transmit output pin |
| TX22 | 10 | 16 | 28 | O | Transmit output pin |
| TX21 | 11 | 17 | 29 | O | Transmit output pin |
| TX20 | 12 | 18 | 30 | O | Transmit output pin |
| TX19 | 13 | 19 | 31 | O | Transmit output pin |
| TX18 | 14 | 20 | 32 | O | Transmit output pin |

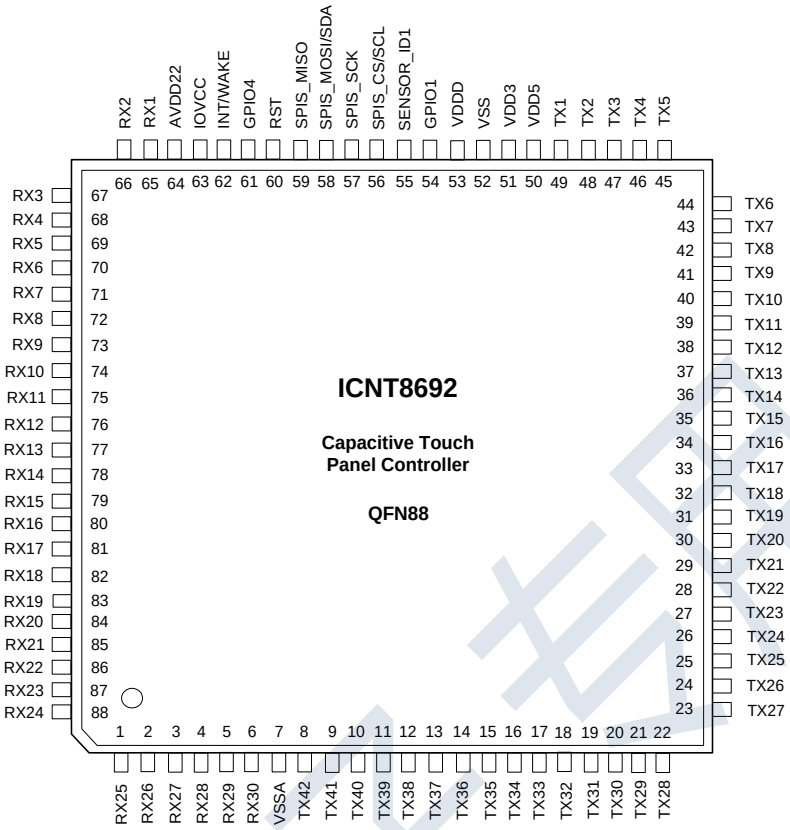
| Pin Name | Pin Num | | | Type | Description |
|---|---|---|---|---|---|
| | ICNT8672 | ICNT8682 | ICNT8692 | | |
| TX17 | 15 | 21 | 33 | O | Transmit output pin |
| TX16 | 16 | 22 | 34 | O | Transmit output pin |
| TX15 | 17 | 23 | 35 | O | Transmit output pin |
| TX14 | 18 | 24 | 36 | O | Transmit output pin |
| TX13 | 19 | 25 | 37 | O | Transmit output pin |
| TX12 | 20 | 26 | 38 | O | Transmit output pin |
| TX11 | 21 | 27 | 39 | O | Transmit output pin |
| TX10 | 22 | 28 | 40 | O | Transmit output pin |
| TX9 | 23 | 29 | 41 | O | Transmit output pin |
| TX8 | 24 | 30 | 42 | O | Transmit output pin |
| TX7 | 25 | 31 | 43 | O | Transmit output pin |
| TX6 | 26 | 32 | 44 | O | Transmit output pin |
| TX5 | 27 | 33 | 45 | O | Transmit output pin |
| TX4 | 28 | 34 | 46 | O | Transmit output pin |
| TX3 | 29 | 35 | 47 | O | Transmit output pin |
| TX2 | 30 | 36 | 48 | O | Transmit output pin |
| TX1 | 31 | 37 | 49 | O | Transmit output pin |
| VDD5 | 32 | 38 | 50 | PWR | Internal generated 5V power supply. A 1μF ceramic capacitor to ground is required. |
| VDD3 | 33 | 39 | 51 | PWR | Analog power supply |
| VSS | 34 | 40 | 52 | PWR | Analog ground |
| VDDD | 35 | 41 | 53 | PWR | Digital power supply (1.2V), generated internal. A 1μF ceramic capacitor to ground is required. |
| GPIO1 | 39 | | 54 | I/O | General Purpose Input/Output port |
| SENSOR_ID1 | 40 | | 55 | I/O | TP Sensor ID Pin |
| SSEL/SCL | 41 | | 56 | I/O | SPI Slave mode: chip select, active low<br>$I^2C$ mode: $I^2C$ clock input |
| SCK | 42 | | 57 | I | SPI Slave mode: clock input<br>$I^2C$ mode: $I^2C$ programming address strapping pin，<br>NC/Pull down: $I^2C$ programming address is 0x60/0x61(including R/W bit);<br>Pull up: $I^2C$ programming address is 0xB0/0xB1(including R/W bit); |

| Pin Name | Pin Num | | | Type | Description |
|---|---|---|---|---|---|
| | ICNT8672 | ICNT8682 | ICNT8692 | | |
| MOSI/SDA | 43 | | 58 | I/O | SPI Slave mode: data input<br>$I^2C$ mode: $I^2C$ data input and output |
| SDA | | 44 | | I/O | $I^2C$ data input and output |
| MISO | 44 | | 59 | O | SPI Slave mode, data output |
| /RST | 45 | 45 | 60 | I | External Reset, active low |
| GPIO4 | 46 | 46 | 61 | I/O | General Purpose Input/Output port<br>or UART TXD Pin |
| INT/WAKE | 47 | 47 | 62 | I/O | External interrupt to the host or<br>Wakeup request from the host |
| IOVCC | | | 63 | PWR | IO power supply |
| AVDD22 | 52 | 48 | 64 | PWR | Analog power supply. A 1μF ceramic capacitor to ground is required. |
| RX1 | 51 | 49 | 65 | I | Receiver input pin |
| RX2 | 53 | 50 | 66 | I | Receiver input pin |
| RX3 | 54 | 51 | 67 | I | Receiver input pin |
| RX4 | 55 | 52 | 68 | I | Receiver input pin |
| RX5 | 56 | 53 | 69 | I | Receiver input pin |
| RX6 | 57 | 54 | 70 | I | Receiver input pin |
| RX7 | 58 | 55 | 71 | I | Receiver input pin |
| RX8 | 59 | 56 | 72 | I | Receiver input pin |
| RX9 | 60 | 57 | 73 | I | Receiver input pin |
| RX10 | 61 | 58 | 74 | I | Receiver input pin |
| RX11 | 62 | 59 | 75 | I | Receiver input pin |
| RX12 | 63 | 60 | 76 | I | Receiver input pin |
| RX13 | 64 | 61 | 77 | I | Receiver input pin |
| RX14 | 65 | 62 | 78 | I | Receiver input pin |
| RX15 | 66 | 63 | 79 | I | Receiver input pin |
| RX16 | 67 | 64 | 80 | I | Receiver input pin |
| RX17 | 68 | 65 | 81 | I | Receiver input pin |
| RX18 | | 66 | 82 | I | Receiver input pin |
| RX18/TX30 | 2 | | | I/O | Receiver input pin/ Transmit output pin |
| RX19 | | 67 | 83 | I | Receiver input pin |
| RX19/TX29 | 3 | | | I/O | Receiver input pin/ Transmit output pin |

| Pin Name | Pin Num | | | Type | Description |
|---|---|---|---|---|---|
| | ICNT8672 | ICNT8682 | ICNT8692 | | |
| RX20 | | 68 | 84 | I | Receiver input pin |
| RX21 | | | 85 | I | Receiver input pin |
| RX21/TX36 | | 1 | | I/O | Receiver input pin/ Transmit output pin |
| RX22 | | | 86 | I | Receiver input pin |
| RX22/TX35 | | 2 | | I/O | Receiver input pin/ Transmit output pin |
| RX23 | | | 87 | I | Receiver input pin |
| RX23/TX34 | | 3 | | I/O | Receiver input pin/ Transmit output pin |
| RX24 | | | 88 | I | Receiver input pin |
| RX24/TX33 | | 4 | | I/O | Receiver input pin/ Transmit output pin |
| NC | 36 | | | | Not connected |
| NC | 37 | | | | Not connected |
| GPIO2 | 38 | | | I/O | General Purpose Input/Output port |
| SCL | | 42 | | I | $I^2C$ clock input |
| P_ADDR_SEL | | 43 | | I | $I^2C$ programming address strapping pin,<br>NC/Pull down: $I^2C$ programming address is 0x60/0x61(including R/W bit);<br>Pull up: $I^2C$ programming address is 0xB0/0xB1(including R/W bit); |
| NC | 48 | | | | Not connected |
| NC | 49 | | | | Not connected |
| NC | 50 | | | | Not connected |

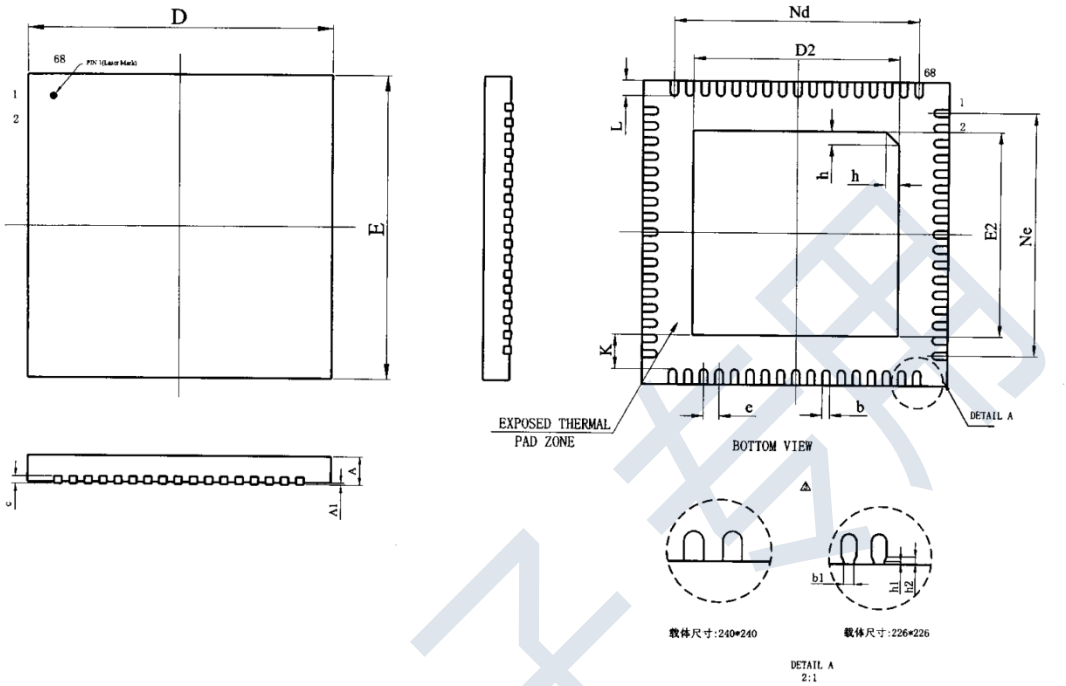

ICNT8672
Capacitive Touch Panel Controller
QFN68
1 RX1
2 NC
3 NC
4 NC
5 INT/WAKE
6 GPIO4
7 /RST
8 MISO
9 MOSI/SDA
10 SCK
11 SSEL/SCL
12 SENSOR_ID1
13 GPIO1
14 GPIO2
15 NC
16 NC
17 VDDD
18 AVDD22
19 RX2
20 RX3
21 RX4
22 RX5
23 RX6
24 RX7
25 RX8
26 RX9
27 RX10
28 RX11
29 RX12
30 RX13
31 RX14
32 RX15
33 RX16
34 RX17
35 VSSA
36 RX18/TX30
37 RX19/TX29
38 TX28
39 TX27
40 TX26
41 TX25
42 TX24
43 TX23
44 TX22
45 TX21
46 TX20
47 TX19
48 TX18
49 TX17
50 TX16
51 TX15
52 VSS
53 VDD3
54 VDD5
55 TX1
56 TX2
57 TX3
58 TX4
59 TX5
60 TX6
61 TX7
62 TX8
63 TX9
64 TX10
65 TX11
66 TX12
67 TX13
68 TX14


ICNT8682
Capacitive Touch Panel Controller
QFN68
1 RX3
2 RX2
3 RX1
4 AVDD22
5 INT/WAKE
6 GPIO4
7 /RST
8 SDA
9 P_ADDR_SEL
10 SCL
11 VDDD
12 VSS
13 VDD3
14 VDD5
15 TX1
16 TX2
17 TX3
18 RX4
19 RX5
20 RX6
21 RX7
22 RX8
23 RX9
24 RX10
25 RX11
26 RX12
27 RX13
28 RX14
29 RX15
30 RX16
31 RX17
32 RX18
33 RX19
34 RX20
35 RX21/TX36
36 RX22/TX35
37 RX23/TX34
38 RX24/TX33
39 VSSA
40 TX32
41 TX31
42 TX30
43 TX29
44 TX28
45 TX27
46 TX26
47 TX25
48 TX24
49 TX23
50 TX22
51 TX21
52 TX4
53 TX5
54 TX6
55 TX7
56 TX8
57 TX9
58 TX10
59 TX11
60 TX12
61 TX13
62 TX14
63 TX15
64 TX16
65 TX17
66 TX18
67 TX19
68 TX20


ICNT8692
Capacitive Touch
Panel Controller
QFN88
RX2 RX1 AVDD22 IOVCC INT/WAKE GPIO4 RST SPIS_MISO SPIS_MOSI/SDA SPIS_SCK SPIS_CS/SCL SENSOR_ID1 GPIO1 VDDD VSS VDD3 VDD5 TX1 TX2 TX3 TX4 TX5
66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45
RX3 67
RX4 68
RX5 69
RX6 70
RX7 71
RX8 72
RX9 73
RX10 74
RX11 75
RX12 76
RX13 77
RX14 78
RX15 79
RX16 80
RX17 81
RX18 82
RX19 83
RX20 84
RX21 85
RX22 86
RX23 87
RX24 88
44 TX6
43 TX7
42 TX8
41 TX9
40 TX10
39 TX11
38 TX12
37 TX13
36 TX14
35 TX15
34 TX16
33 TX17
32 TX18
31 TX19
30 TX20
29 TX21
28 TX22
27 TX23
26 TX24
25 TX25
24 TX26
23 TX27
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
RX25 RX26 RX27 RX28 RX29 RX30 VSSA TX42 TX41 TX40 TX39 TX38 TX37 TX36 TX35 TX34 TX33 TX32 TX31 TX30 TX29 TX28

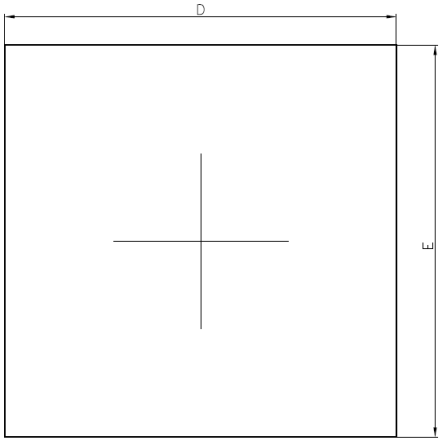
# 6、Package Outline

## QFN-8x8-68L

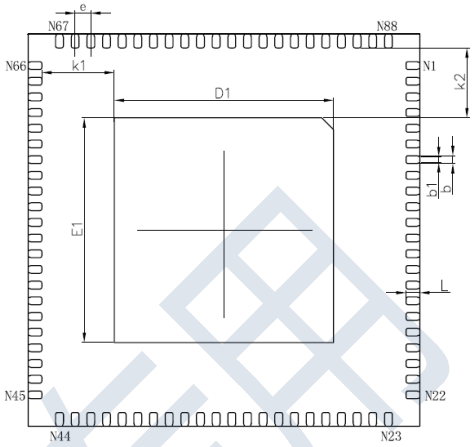



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | | 0.14REF | |
| c | 0.18 | 0.20 | 0.25 |
| D | 7.90 | 8.00 | 8.10 |
| e | | 0.40BSC | |
| Nd | | 6.40BSC | |
| E | 7.90 | 8.00 | 8.10 |
| Ne | | 6.40BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| h | 0.30 | 0.35 | 0.40 |
| h1 | | 0.04REF | |
| h2 | | 0.10REF | |

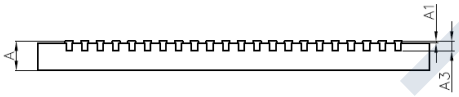
## QFN-10x10-88L




TOP VIEW




BOTTOM VIEW




SIDE VIEW

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 9.900 | 10.100 | 0.390 | 0.398 |
| E | 9.900 | 10.100 | 0.390 | 0.398 |
| D1 | 5.500 | 5.700 | 0.217 | 0.224 |
| E1 | 5.630 | 5.830 | 0.222 | 0.230 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| b1 | 0.150REF. | | 0.006REF. | |
| e | 0.400BSC. | | 0.016BSC. | |
| k1 | 1.850REF. | | 0.073REF. | |
| k2 | 1.785REF. | | 0.070REF. | |
| L | 0.274 | 0.426 | 0.011 | 0.017 |

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# Revision History

| Version | Revisions | Date | Modified by |
|---|---|---|---|
| 0.1 | 1. First draft. | 2014-11-04 | |
| 0.2 | 1. Characteristics and features revision<br>2. Update pin description and circuit diagram<br>3. SPI description modification. | 2014-12-09 | |
| 0.3 | 1.Update the suspend mode and notes | 2015-03-16 | |
| 0.4 | 1.Update the circuit diagram | 2015-06-05 | |
| 1.0 | 1.Update the POD | 2015-12-14 | |
| | | | |
| | | | |