ICONIC RF

a MICROCHIP company

23-31GHz 5W GaN PA MMIC

ICP2637

Product Overview

ICONICRF's ICP2637 is a three stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. The PA operates from 23-31GHz with 37dBm output power, 25% PAE and 23dB small signal gain. The die has integrated DC blocking capacitors and is matched to 50ohms on the RF input and output ports. The operating frequency provides flexible operation for a variety of applications including satellite and 5G. The ICP2637P is 100% DC and RF tested on-wafer to ensure compliance with electrical specifications.

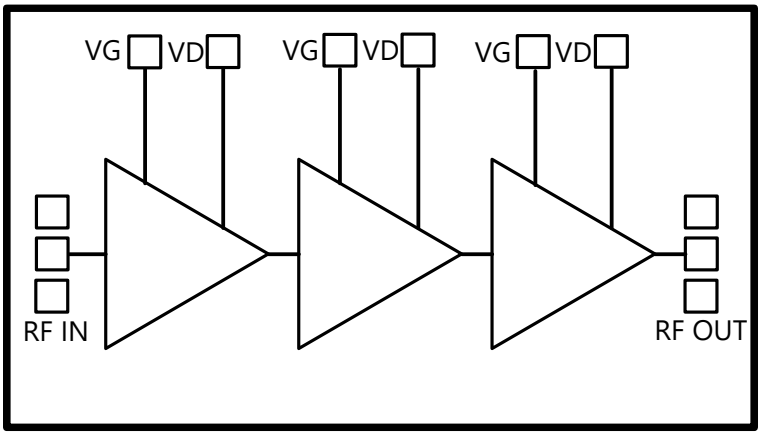
Key Features

- Frequency Range: 23-31GHz
- Pout: 37 dBm @ 19dBm Pin
- PAE: 25 %
- Small Signal Gain: 23dB
- Bias: VD=28V IDQ=84mA
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Integrated Power Detector
- Chip Dimensions: 3.1x1.78x0.05mm

Applications

- 5G
- Satellite Communications
- Aerospace & Defense

Functional Block Diagram



Electrical Specifications | Test Conditions unless otherwise stated | V_D=*28V*, I_D=*84mA*, *TA*=25 °C, CW

Parameter	Conditions	Min	Typ	Max	Units
Frequency		23		31	GHz
Output Power @ P_{sat}	Pin=19dBm		37		dBm
PAE @ P_{sat}	Pin=19dBm		25		%
Small Signal Gain			23		dB
Input Return Loss			10		dB
Output Return Loss			7		dB
I_{DQ}			84		mA

Absolute Maximum Ratings

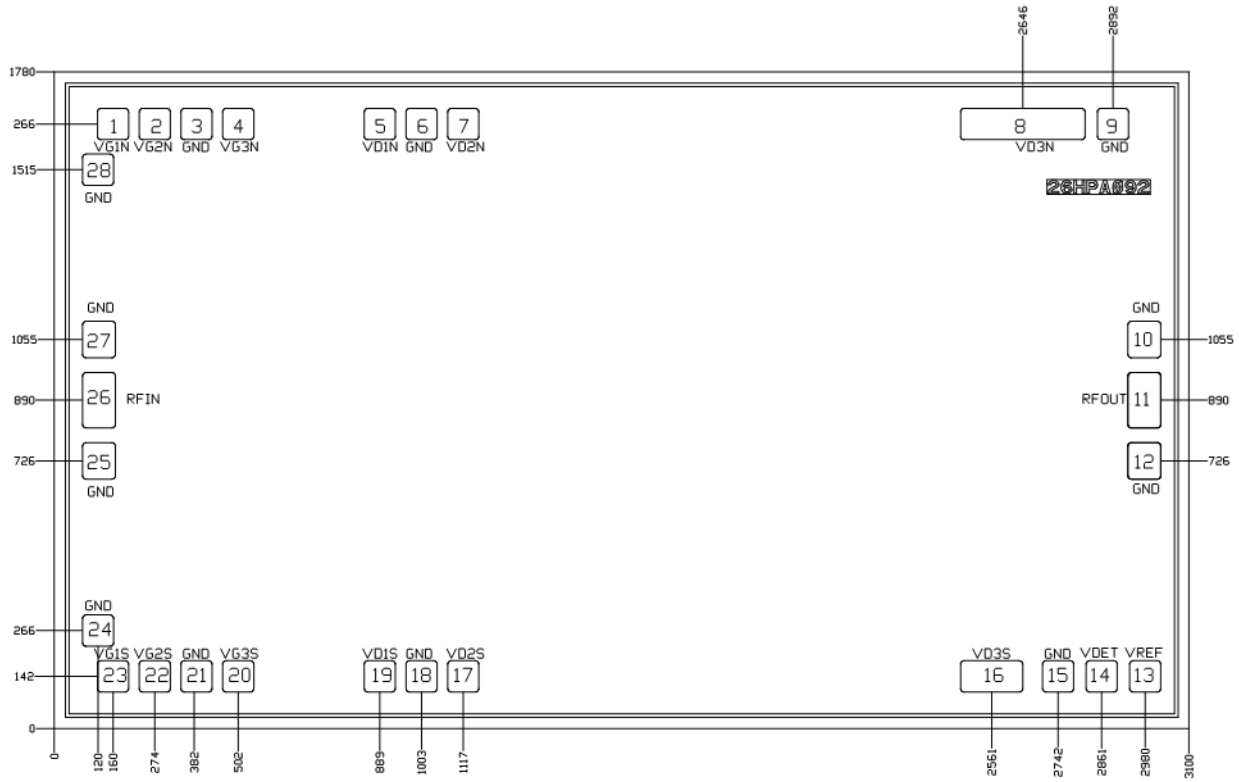
Parameter	Absolute Maximum
Drain Voltage (V_D)	30.0V
Gate Voltage Range (V_G)	-5 to 0V
Gate Current	4.2mA
Drain Current (CW) T_A=25ºC	1.5A
CW Input Power 50ohm, T_A=25ºC	+25dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C

Exceeding any one or combination of these limits may cause permanent damage to this device.
ICONIC RF does not recommend sustained operation near these survivability limits.

Ordering Information

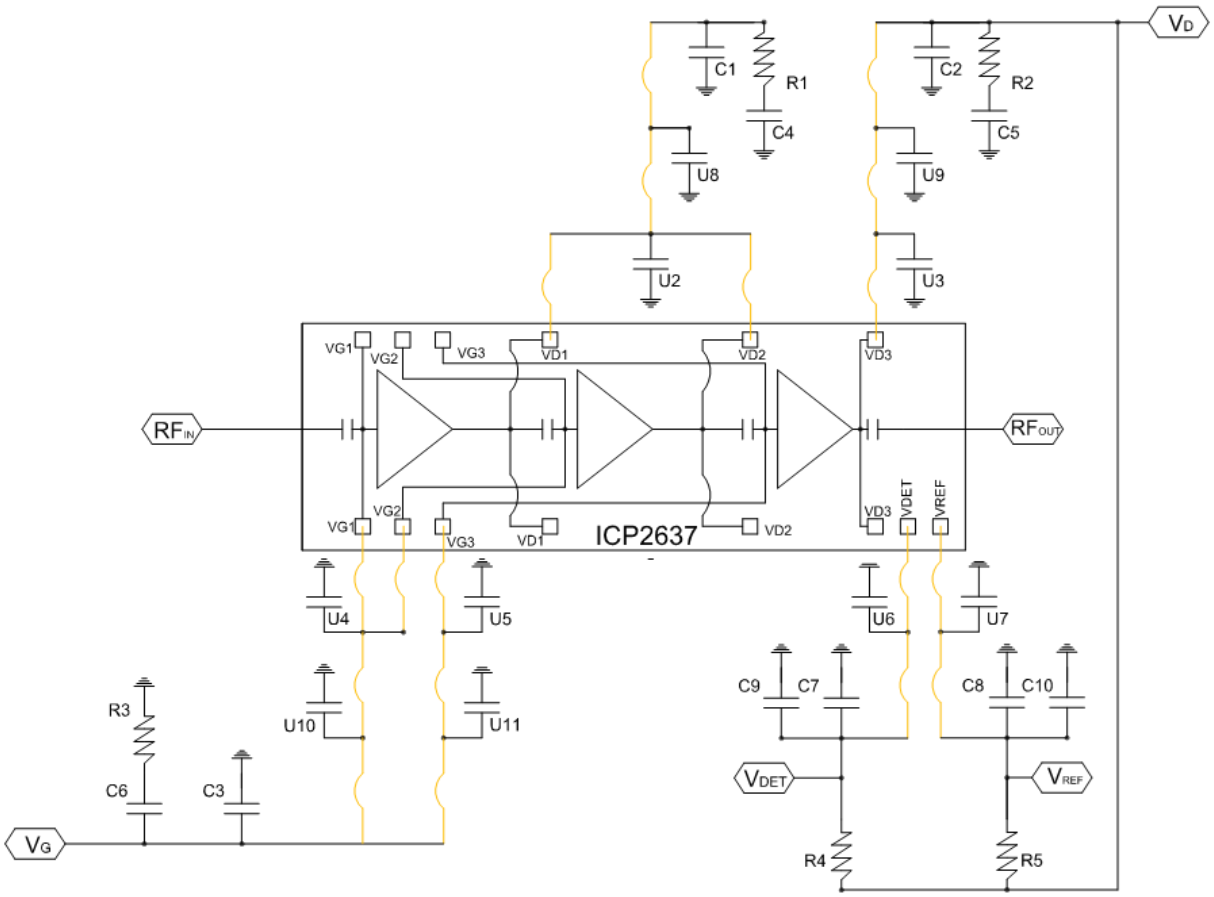
Part No.	Description
ICP2637-1-110I	Bare die in Gel Pack
ICP2637-1-505U	EVB with 2.4mm connectors

Mechanical Drawing



Pad No	Pad size (um)	Function	Description
1,23	85x85	VG1	First stage gate bias, decoupling and bypass caps required
2,22	85x85	VG2	Second stage gate bias, decoupling and bypass caps required
3,21	85x85	GND	Ground Pads
4,20	85x85	VG3	Third stage gate bias, decoupling and bypass caps required
5,19	85x85	VD1	First stage drain voltage, decoupling and bypass caps required
6,18	85x85	GND	Ground Pads
7.17	85x85	VD2	Second stage drain voltage, decoupling and bypass caps required
8	340x85	VD3	Third stage drain voltage, decoupling and bypass caps required
9,15	85x85	GND	Ground Pads
10,12,25,27	90x100	GND	Ground Pads
11	90x150	RFOUT	RF Output
13	85x85	VREF	Detector circuit reference voltage output
14	85x85	VDET	Detector circuit voltage output
16	170x85	VD3	Third stage drain voltage
24,28	85x85	GND	Ground Pads
26	90x150	RFIN	RF Input

Application Circuit



Bill of Materials

Assembly Reference	Value	Description
U1		ICP2637 MMIC
U2-U7	100pF	100pF SLC Capacitor
U8-U11	10nF	10nF SLC Capacitor
C1-C3	10nF	10nF Capacitor,10%,50V,0402
C4-C6,C9,C10	10uF	10uF Capacitor,10%,50V,1206
C7,C8	1000pF	1000pF Capacitor,10%,50V,0402
R1-R3	5.1Ohm	5.1 ohm resistor, 0402
R4,R5	200KOhms	200Kohm resistor, 0402

Assembly Guidance

Optimum RF power performance achieved by minimizing output RF bond wire length.

Interconnect assembly Notes

- Ball Bonding is preferred technique
- Force, time and ultrasonic parameters are critical.
- Aluminum wire bonding is not recommended.
- Bond Wire diameter of 1mil is recommended.

Die attach of component using adhesive

- Vacuum collets are preferred method of pickup.
- Pickup method must consider the avoidance of die air bridges.
- Die suitable for Eutectic and Epoxy die attach.
- Where Epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:-
    - Kyocera CT2700R7S

Die attach using Eutectic

- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280ºC) preform is preferred between the die and attached surface.
- Recommended preform should be approximately 0.0012" thick.
- Die bonder using heated collet with a temperature of 310ºC and die scrubbing should be used to ensure wetting and prevent formation of voids.
- Exposure to extreme temperature should be kept to a minimum.
- The optimum die attach environment is nitrogen atmosphere.

Reflow Process

- Maximum temperature 320ºC for 30 seconds.
- Material matching for coefficient of thermal expansion is crucial for long-term reliability

Bias-Up Procedure

1. Set V_G=-5V
2. Set V_D to 20-28V
3. Adjust V_G positive until I_D quiescent is achieved
4. Limit I_D to safe level to protect device
5. Apply RF Signal

Bias-down Procedure

1. Turn off RF
2. Turn off V_D, allow drain capacitor to discharge
3. Turn off V_G.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. Class 1A HBM (250-500V) ESD Classification is anticipated.

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