

27.5 – 31 GHz 9W GaN PA MMIC

Product Overview

Microchip's ICP2840 is a Ka Band MMIC power amplifier fabricated using GaN SiC technology. It achieves 39.5 dBm saturated output power from 27.5 – 31 GHz, with 22% PAE and 22 dB small signal gain. The balanced topology provides excellent broadband input and output match to 50Ω and DC blocking capacitors ensure simple integration.

Excellent linearity characteristics make ICP2840 well suited to applications in Satellite Communications. The die are 100% DC and RF tested on wafer ensuring compliance to the electrical specifications.

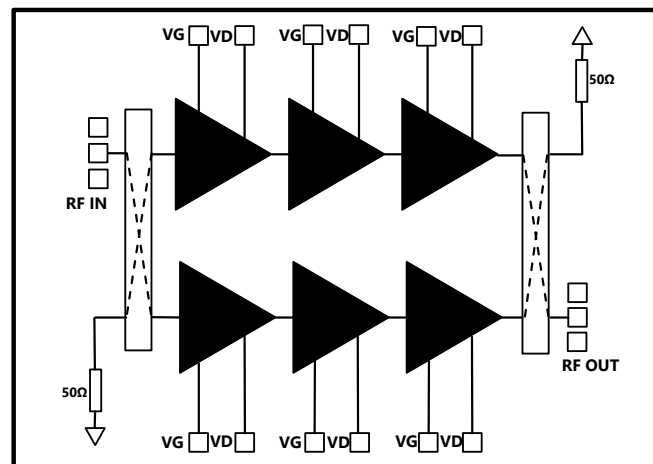
Key Features

- Frequency range: 27.5 – 31 GHz
- Pout: 39.5 dBm (Pin = 24 dBm)
- PAE: 22% (Pin = 24 dBm)
- Small Signal Gain: 22 dB (28 GHz)
- Return Loss: 15 dB
- Drain Bias 24V, IDQ = 112 mA – 224 mA
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Dimensions: 3.025 mm × 3.405 mm × 0.10 mm

Applications

- Satellite Communications
- Aerospace & Defense
- 5G

Functional Block Diagram



Typical Performances

Parameter	Typical	Units	Conditions ¹
Frequency range	27.5 – 31	GHz	
Saturated Output Power, Psat	39.5	dBm	Pin = 24 dBm
Power Added Efficiency, PAE	22	%	Pin = 24 dBm
Small Signal Gain, S21	22	dB	
Input Return Loss	-15	dB	
Output Return Loss	-15	dB	

Note:

1. Test conditions unless otherwise stated CW, VD = 24V, IDQ = 110 mA, VG ~ -1.84V typical, TA = 25 °C

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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Electrical Specifications

Parameter	Min	Typical	Max	Units	Conditions(1)
Frequency Range	27.5		31	GHz	
Saturated Output Power, Psat	37	39.5		dBm	Pin = 24 dBm
Power Added Efficiency, PAE		22		%	Pin = 24 dBm
Small Signal Gain, S21		22		dB	
Input Return Loss		-15		dB	
Output Return Loss		-15		dB	
Power Detector Range	20		39	dBm	Temperature reference diode provided

(1) Test conditions unless otherwise stated CW, VD = 24V, IDQ = 110 mA ,VG~ -1.84V typical, TA = 25 °C

Table 1-2. Recommended Operating Conditions

Parameters	Value
Drain Voltage (VD)	20V – 24V
Drain Quiescent Current (IDQ)	100 mA – 224 mA
Gate Voltage Range (VG)	-2V to -1.5V
Operating Temperature (TA)	-40 °C to +85 °C

1.2 Absolute Maximum Ratings

Table 1-3. Thermal and Reliability

Parameters	Value
Thermal resistance	4.9 °C/W

Notes

1. Assumes silver sintered epoxy attach (20 μm thick) mounted on CuMo carrier.
2. Base temperature is assumed at the top of the CuMo carrier
3. Thermal resistance calculated using IR measurement of the channel temperature

Table 1-4. Absolute Maximum Ratings

Parameters	Absolute Maximum
Drain voltage (VDG)	32V
Gate voltage range (VG)	-5V to 0V
Drain current (ID)	3A

.....continued	
Parameters	Absolute Maximum
Gate current (IG)	6.0 mA
CW power dissipation (85 °C)	40W
CW input power—no instability (4:1 VSWR, VD = 20V, IDQ = 112 mA, 25 °C)	+25 dBm
CW input power—no damage (10:1 VSWR, VD = 20V, IDQ = 112 mA, 25 °C)	+25 dBm
Channel temperature	275 °C
Eutectic die attach temperature (30s)	320 °C
Storage temperature	-65 °C to +150 °C

Note: Exceeding any one or combination of these limits may cause permanent damage to this device. Microchip does not recommend sustained operation near these survivability limits.

1.3 Typical RF Performance

1.3.1 Typical Small Signal Performance

Test Conditions (unless otherwise stated): Temp = 25 °C, CW, VD = 24V, ID = 110 mA.

Figure 1-1. Gain vs. Temperature @ 20V/110mA

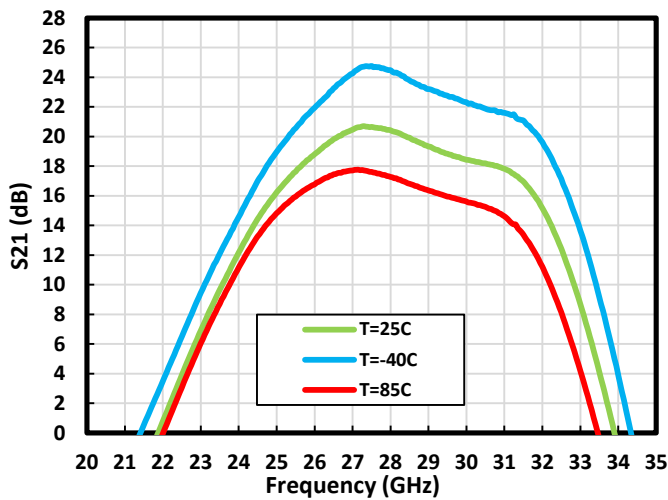


Figure 1-2. Gain vs. Temperature @ 24V/110mA

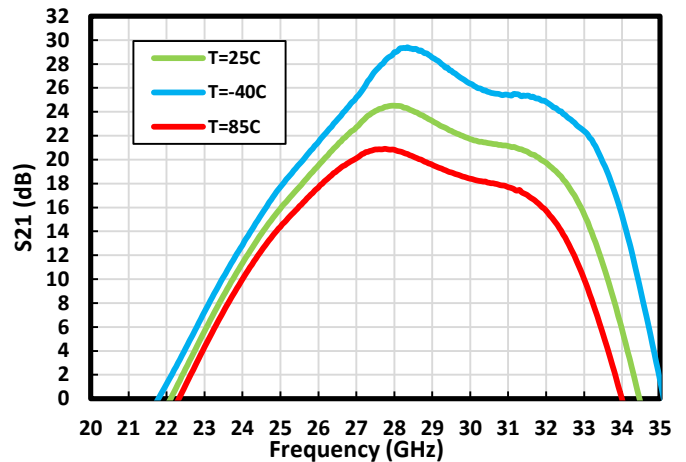


Figure 1-3. S11 vs. Temperature @ 20V/110mA

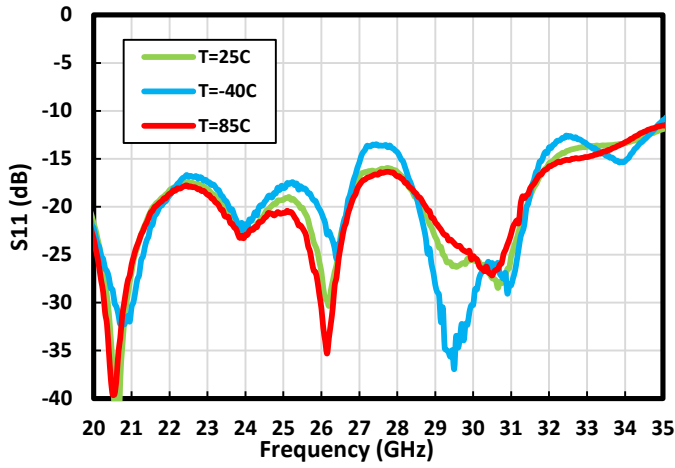


Figure 1-4. S11 vs. Temperature @ 24V/110mA

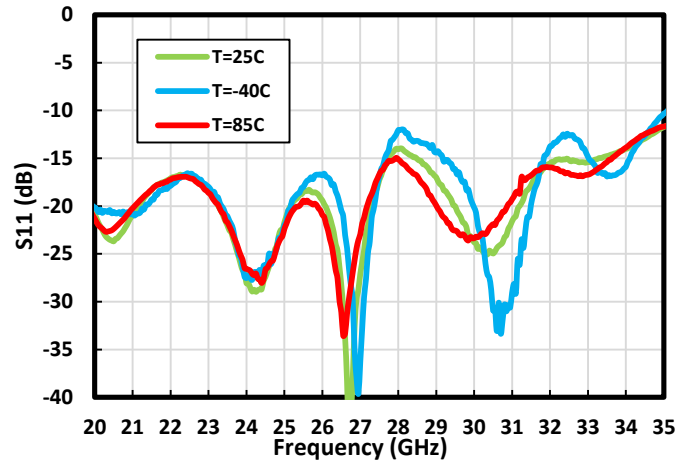


Figure 1-5. S22 vs. Temperature @ 20V/110mA

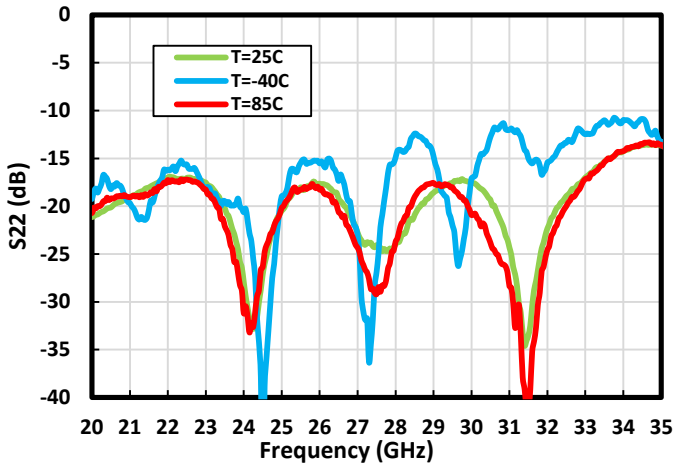
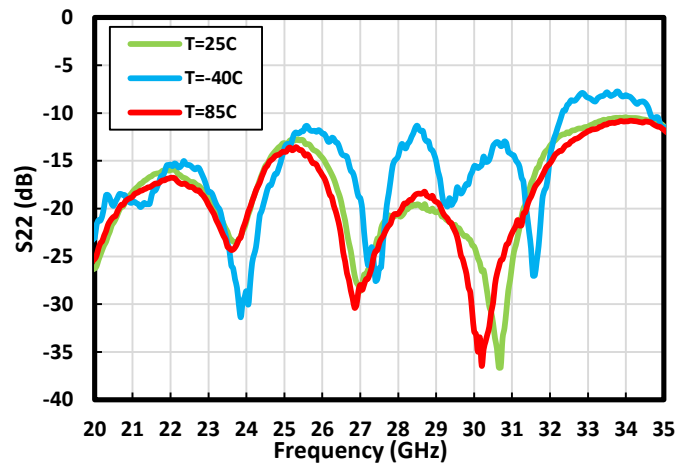


Figure 1-6. S22 vs. Temperature @ 24V/110mA



1.3.2 Typical Power Performance

Test Conditions (unless otherwise stated): Temp = 25 °C, CW, VD = 24V, ID = 110 mA.

Figure 1-7. Pout vs. Pin @ 20V

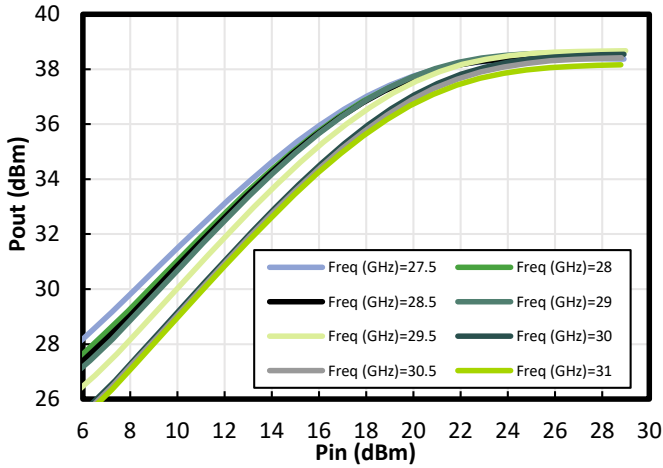


Figure 1-8. Gain vs. Pout @ 20V

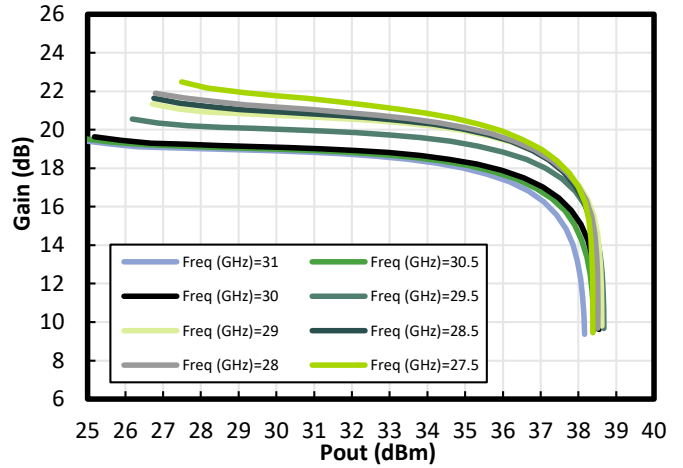


Figure 1-9. PAE vs. Pout @ 20V

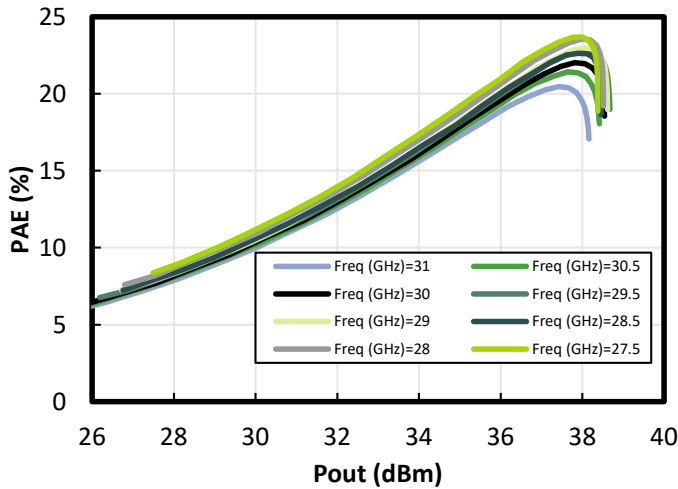


Figure 1-10. Id vs. Pout @ 20V

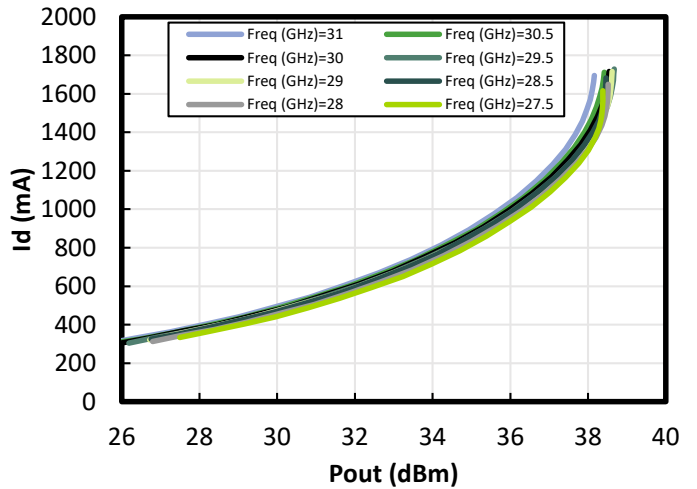


Figure 1-11. Pout vs. Pin @ 24V/100mA

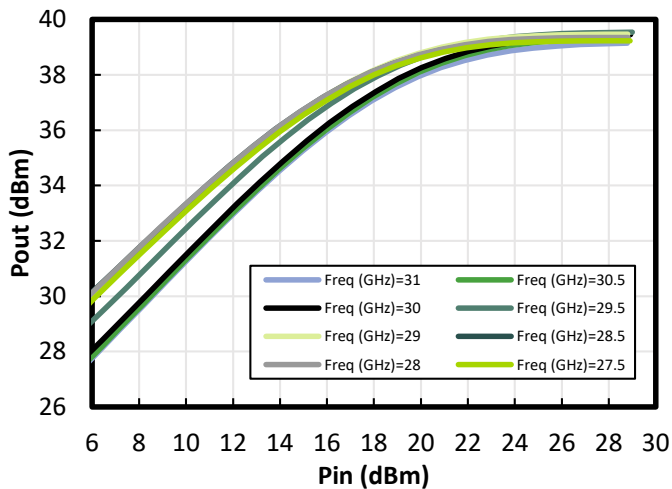


Figure 1-12. Gain vs. Pout @ 24V/100mA

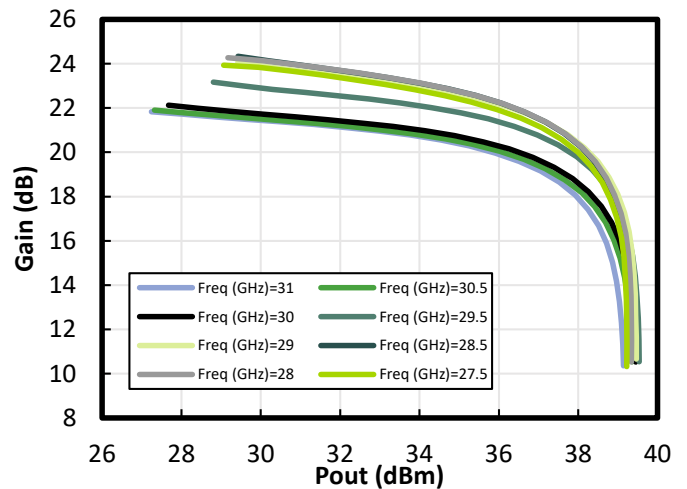


Figure 1-13. PAE vs. Pout @ 24V/100mA

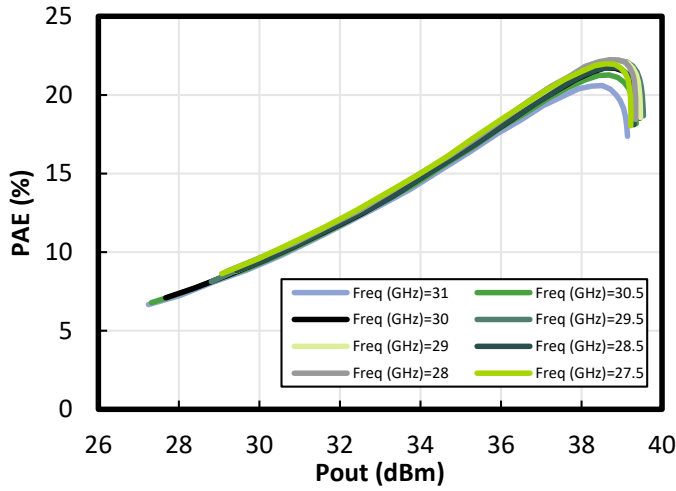


Figure 1-14. Id vs. Pout @ 24V/100mA

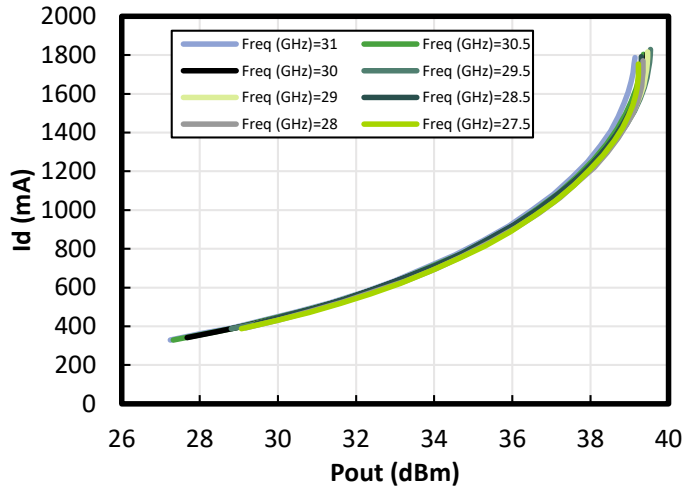


Figure 1-15. Pout vs. Freq @ 24V/110mA

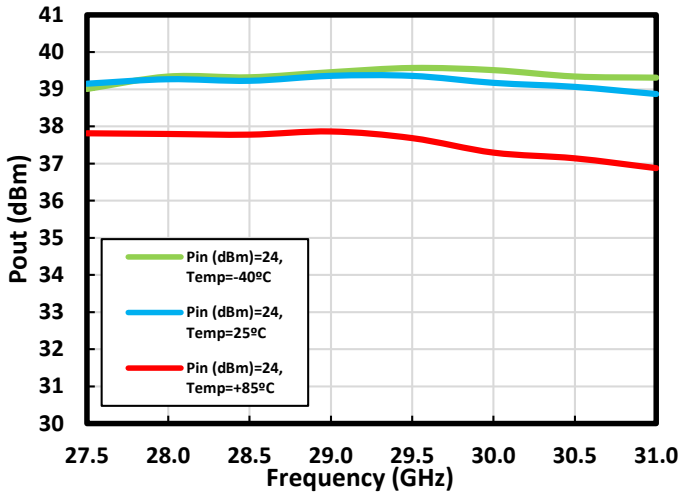


Figure 1-16. Gain vs. Freq @ 24V/110mA

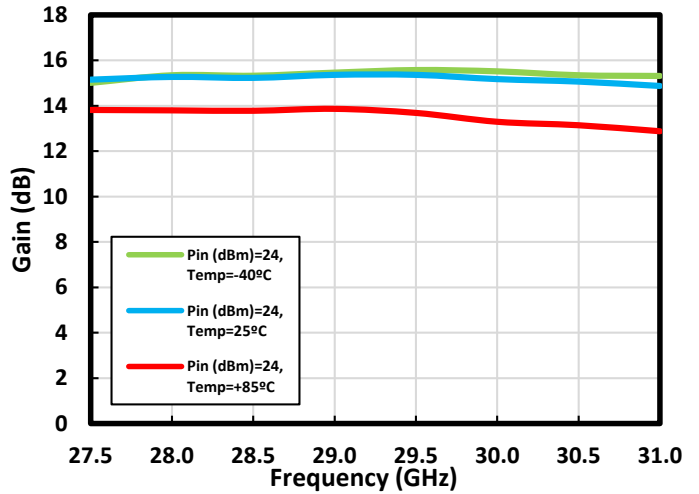


Figure 1-17. PAE vs. Freq @ 24V/110mA

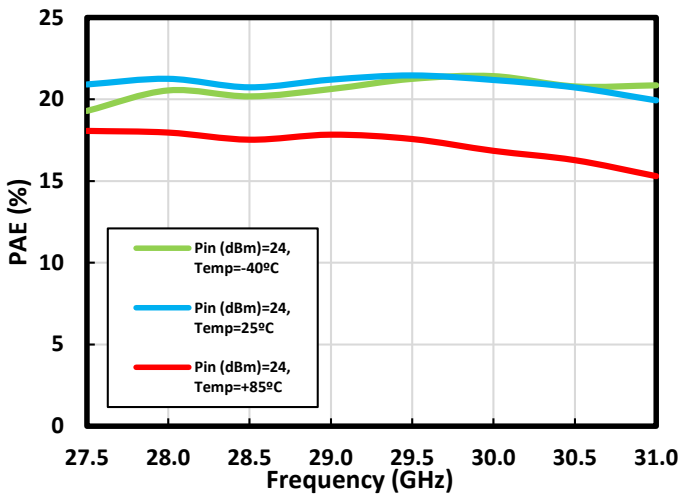


Figure 1-18. Id vs. Freq @ 24V/110mA

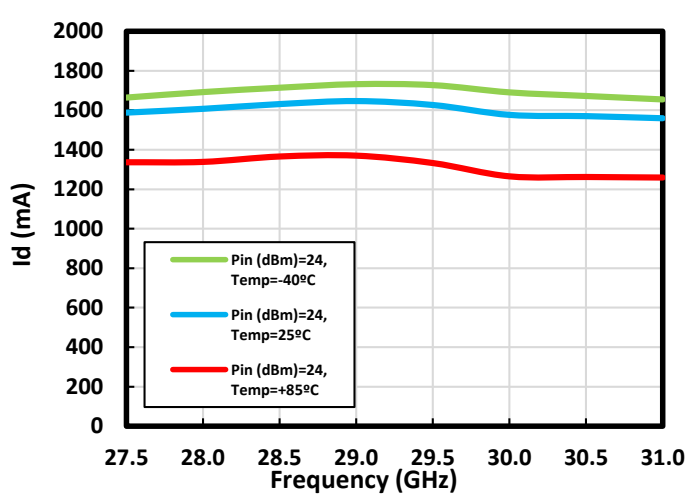


Figure 1-19. Pout vs. Pin @ 28GHz & 24V/110mA

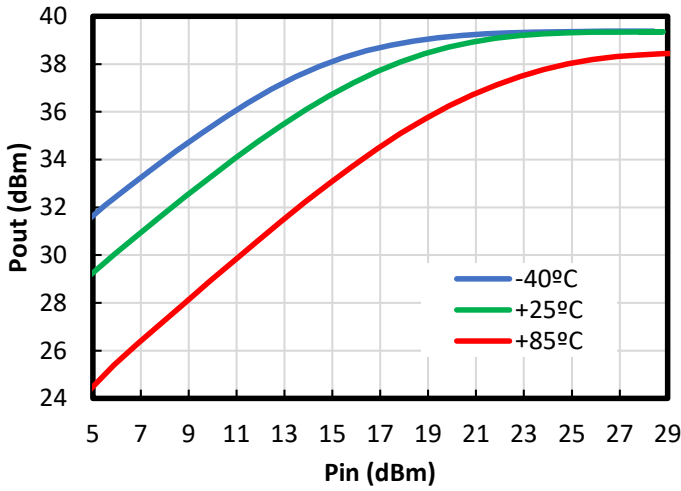


Figure 1-20. Gain vs. Pout @ 28GHz & 24V/110mA

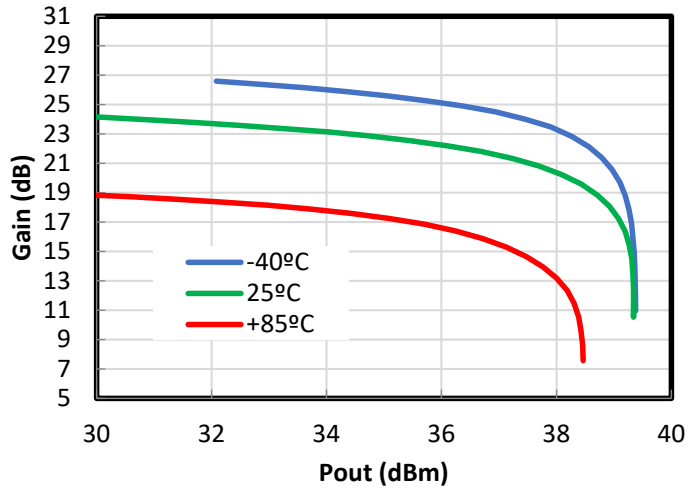


Figure 1-21. PAE vs. Pout @ 28GHz & 24V/110mA

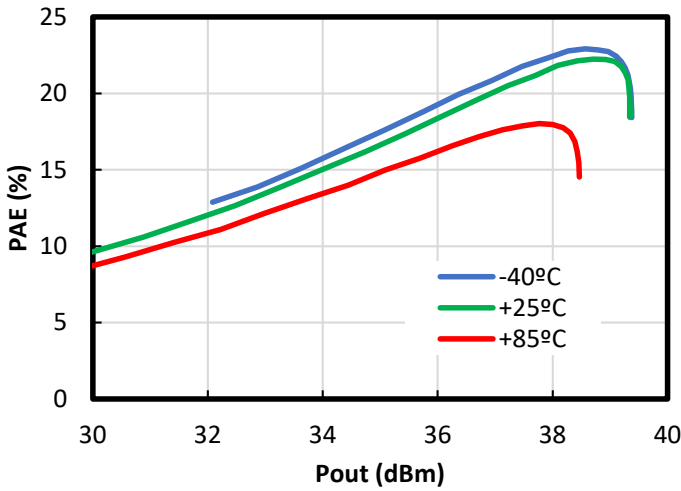


Figure 1-22. Id vs. Pout @ 28GHz & 24V/110mA

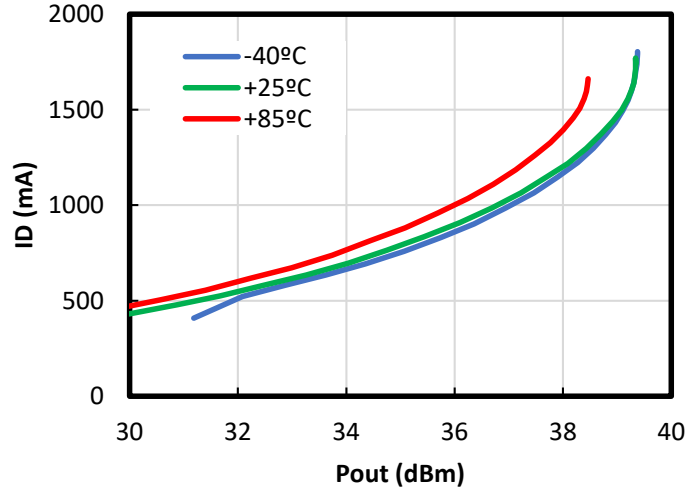


Figure 1-23. Pout vs. Pin @ 29GHz & 24V/110mA

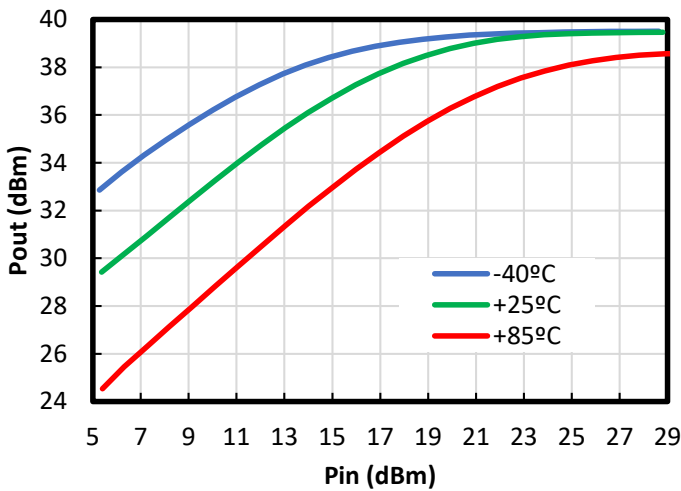


Figure 1-24. Gain vs. Pout @ 29GHz & 24V/110mA

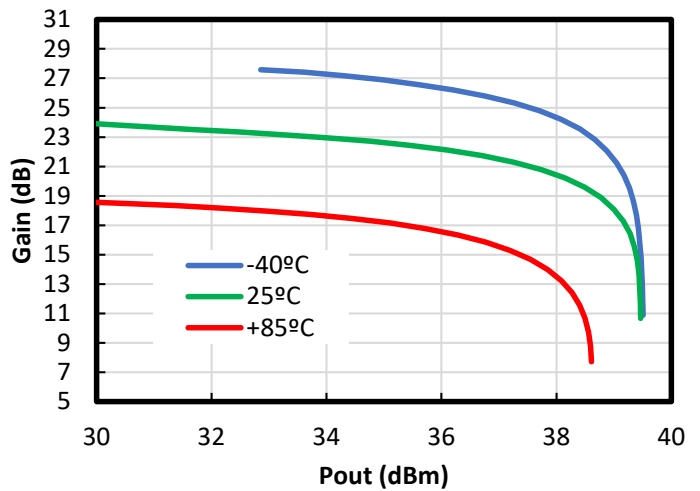


Figure 1-25. PAE vs. Pout @ 29GHz & 24V/110mA

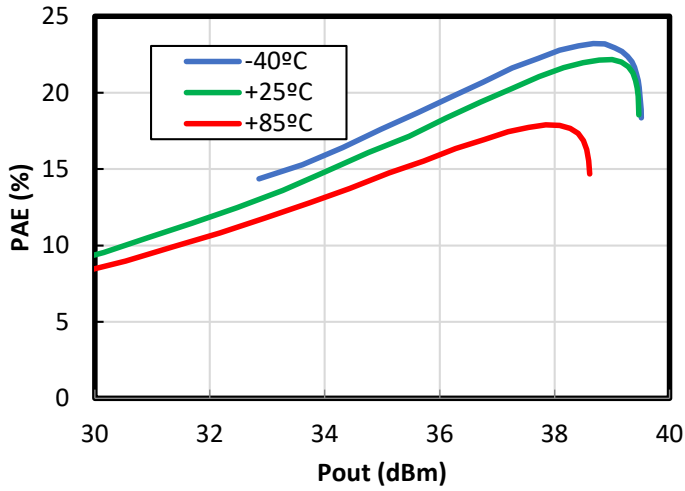


Figure 1-26. Id vs. Pout @ 29GHz & 24V/110mA

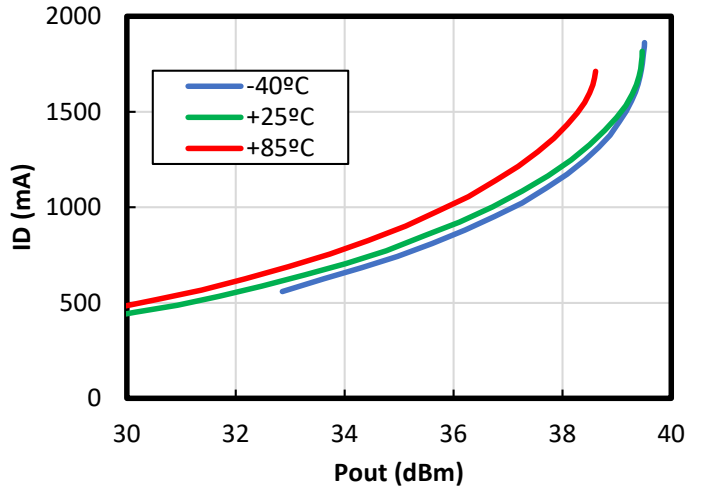


Figure 1-27. Pout vs. Pin @ 30GHz & 24V/110mA

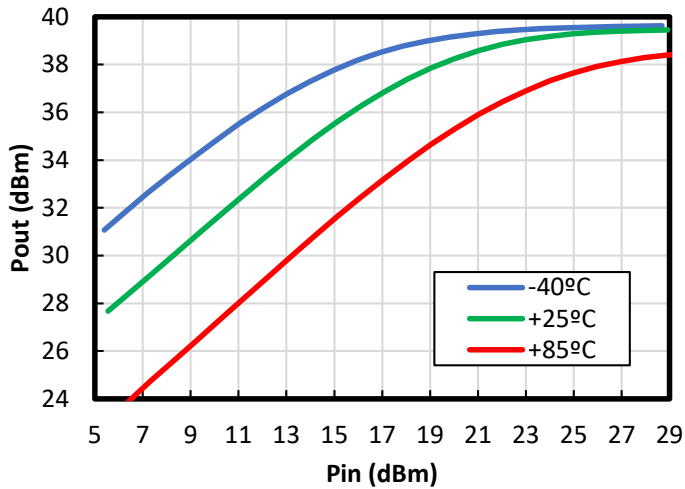


Figure 1-28. Gain vs. Pout @ 30GHz & 24V/110mA

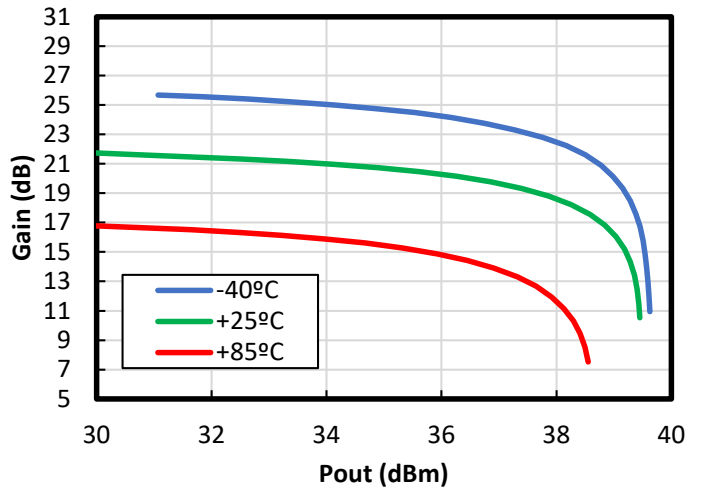


Figure 1-29. PAE vs. Pout @ 30GHz & 24V/110mA

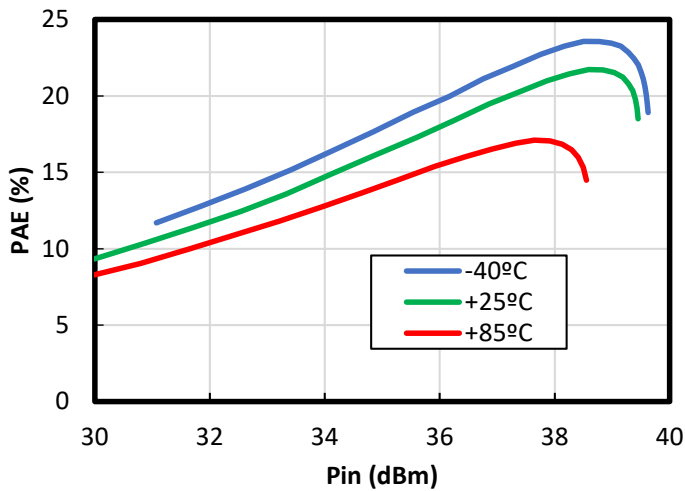
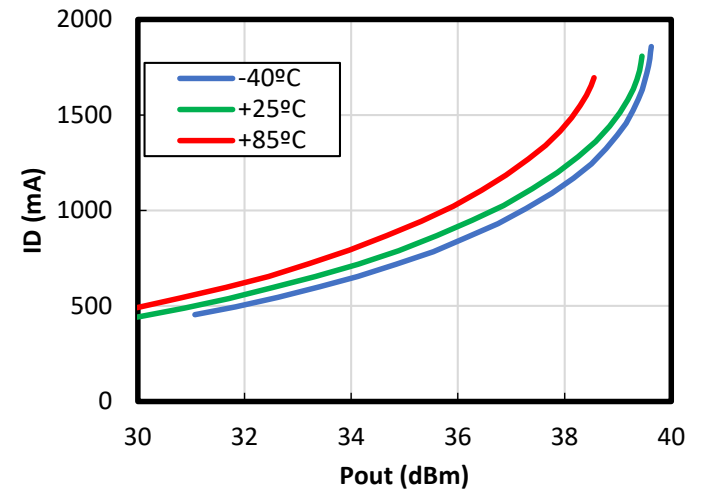


Figure 1-30. Id vs. Pout @ 30GHz & 24V/110mA



1.3.3 Typical 2-Tones RF Performance

Test Conditions (unless otherwise stated): Temp = 25 °C, VD = 20V, ID = 110 mA, CW Tone spacing of 10 MHz.

Figure 1-31. IM3 vs. Pout @ 20V & -40°C

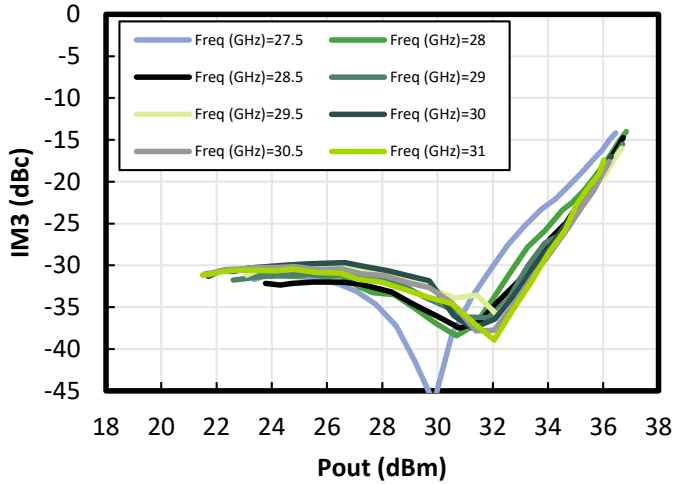


Figure 1-32. IM3 vs. Pout @ 24V & -40°C

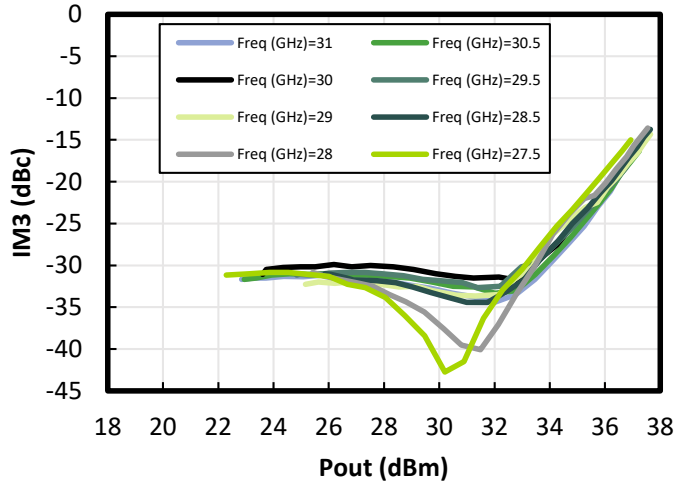


Figure 1-33. IM3 vs. Pout @ 20V & 25°C

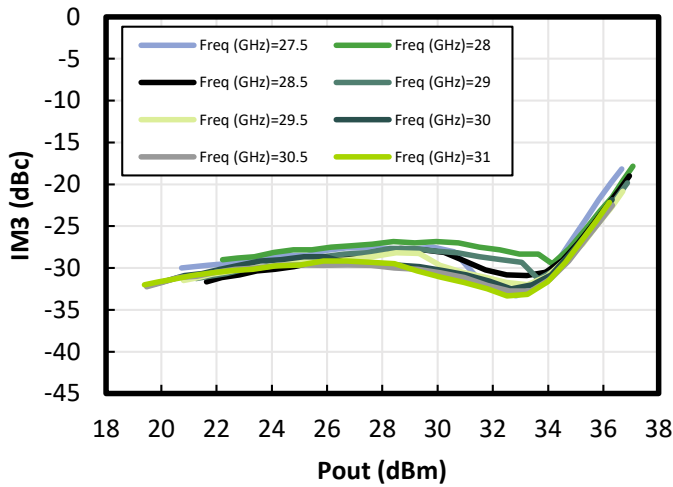


Figure 1-34. IM3 vs. Pout @ 24V & 25°C

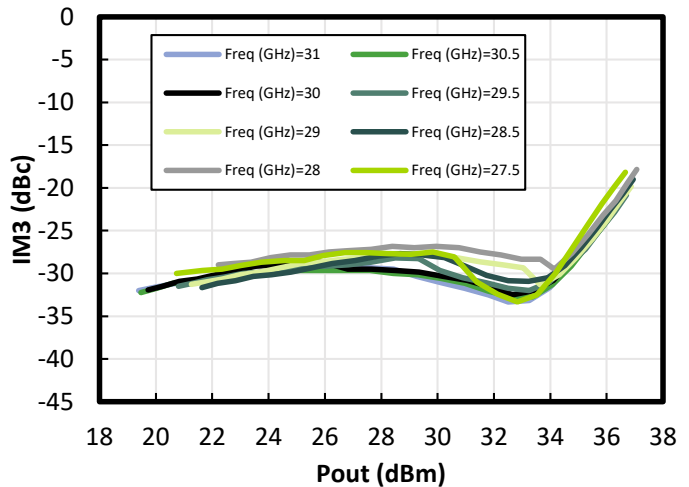


Figure 1-35. IM3 vs. Pout @ 20V & +85°C

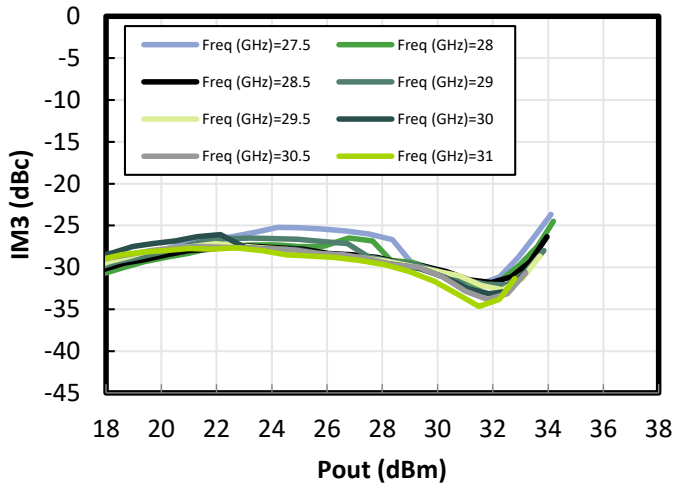
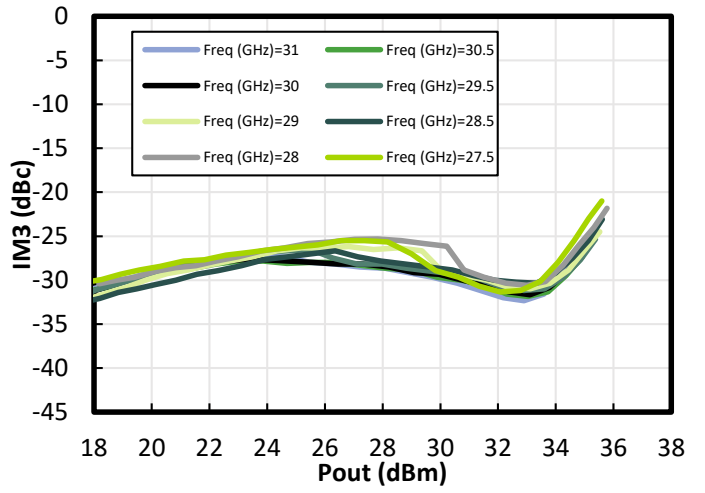


Figure 1-36. IM3 vs. Pout @ 24V & +85°C



2. Die Specifications

- Units: μm
- Thickness: 100 μm
- Die size tolerance: $\pm 50 \mu\text{m}$
- Backside is RF and DC ground
- Amplifier must be biased from both sides (N) North, (S) South

Figure 2-1. Die Outline Drawing

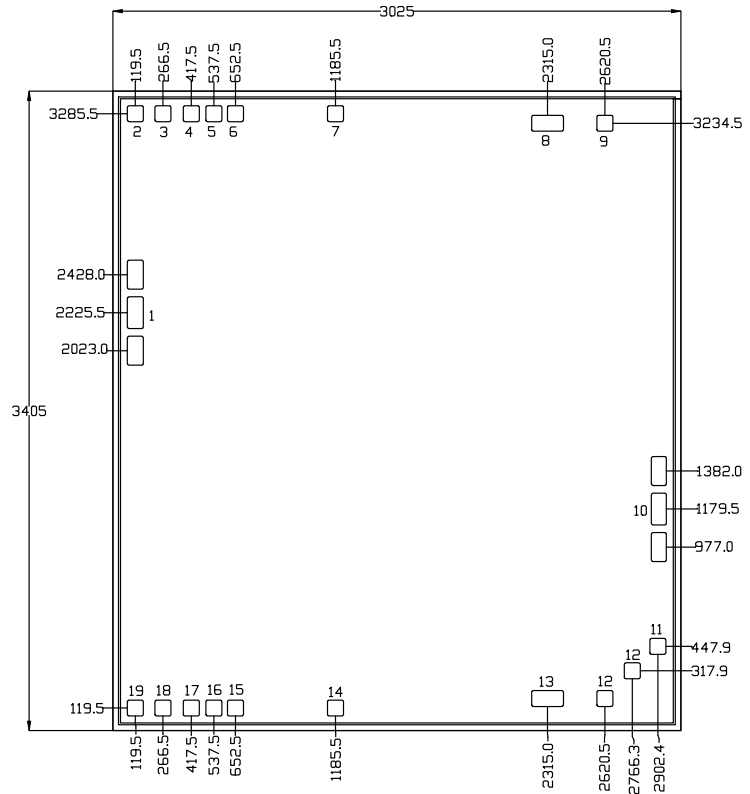


Table 2-1. I/O Description

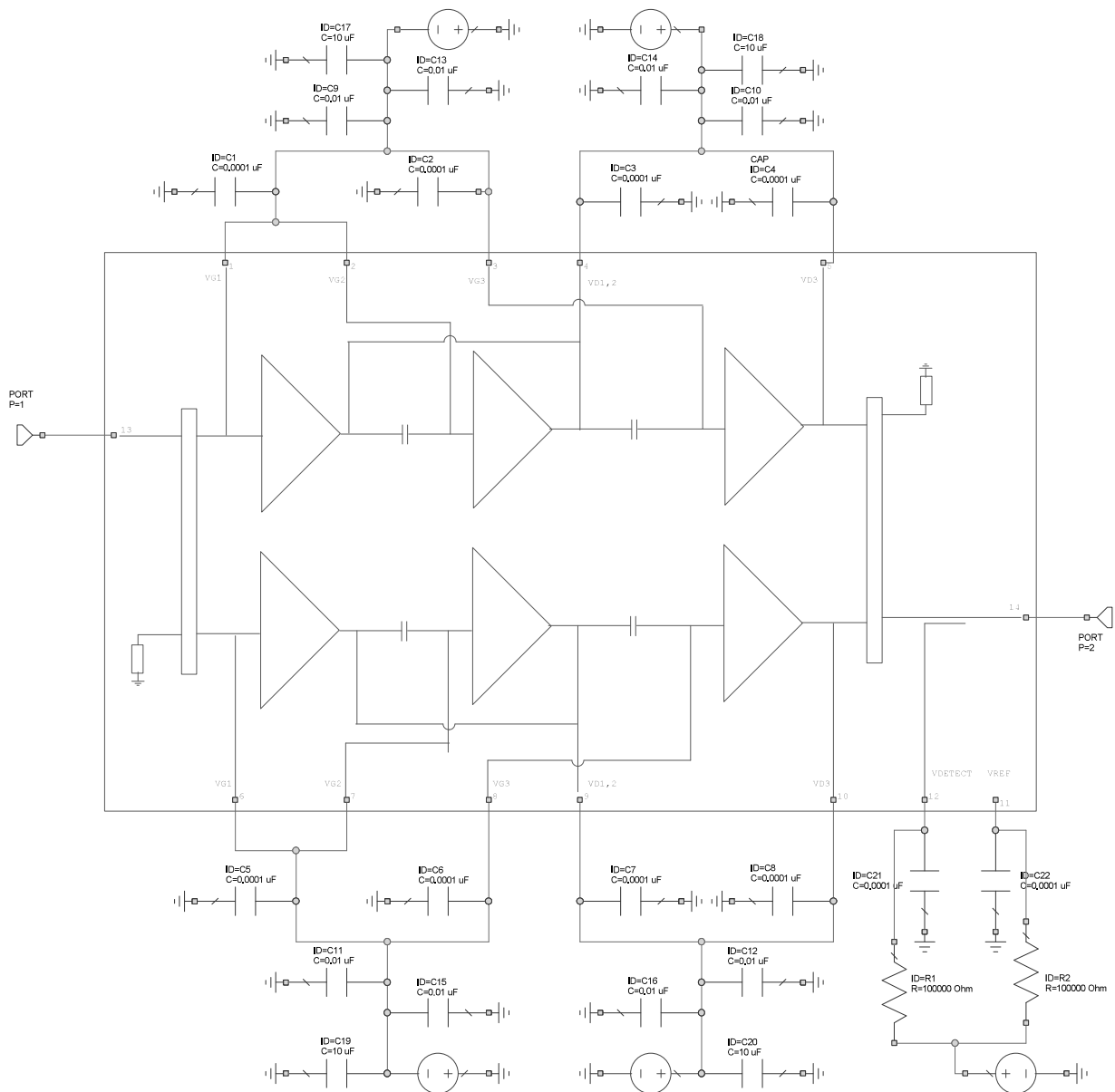
Pad No	Pad Size (μm)	Function	Description
1	85×170	RFIN	DC blocked and 50 Ω matched
2	85×85	GND	Ground Pad
3	85×85	VG1N	Gate voltage, decoupling and bypass caps required
4	85×85	VG2N	Gate voltage, decoupling and bypass caps required
5	85×85	VG3N	Gate voltage, decoupling and bypass caps required
6	85×85	GND	Ground Pad
7	85×85	VD1N & VD2N	Drain voltage, decoupling and bypass caps required
8	170×170	VD3N	Drain voltage, decoupling and bypass caps required
9	85×85	GND	Ground Pad
10	85×170	RFOUT	DC blocked and 50 Ω matched
11	85×85	VREF	Detector reference voltage

.....continued

Pad No	Pad Size (μm)	Function	Description
12	85×85	VDET	Detector reference voltage
13	85×85	GND	Ground Pad
14	170×85	VD3S	Drain voltage, decoupling and bypass caps required
15	85×85	GND	Drain voltage, decoupling and bypass caps required
16	85×85	GND	Ground Pad
17	85×85	VG3S	Gate voltage, decoupling and bypass caps required
18	85×85	VG2S	Gate voltage, decoupling and bypass caps required
19	85×85	VG1S	Gate voltage, decoupling and bypass caps required
20	85×85	GND	Ground Pad

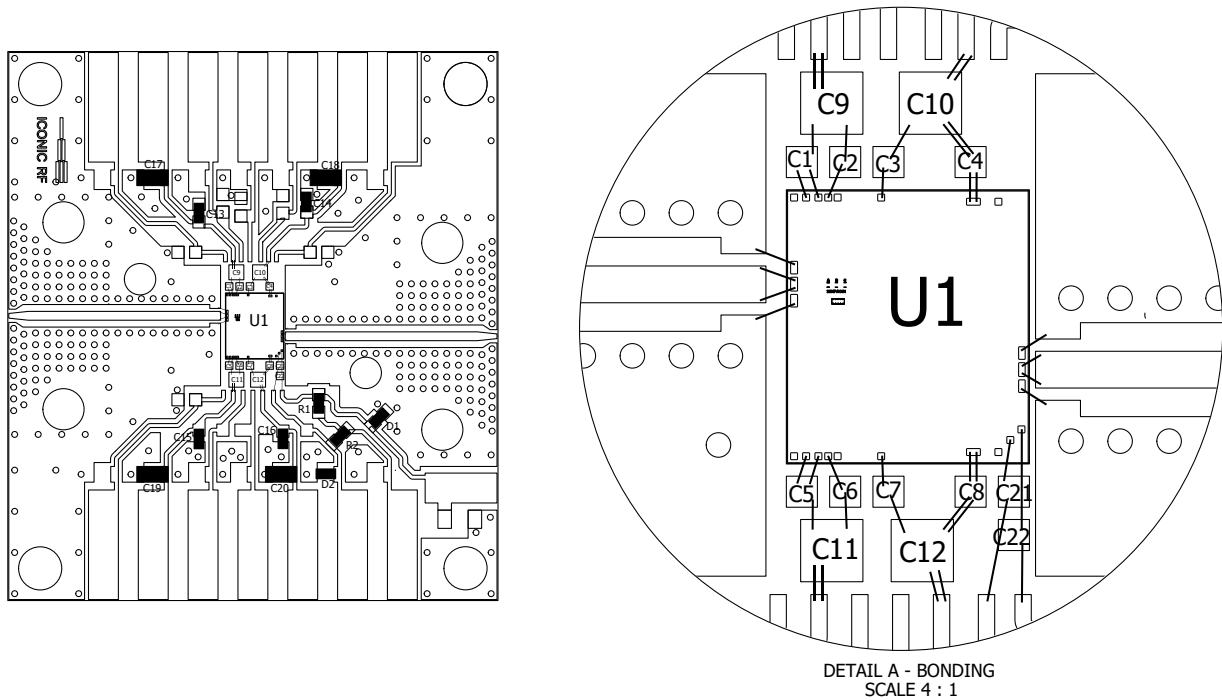
3. Application Circuits

Figure 3-1. Application Circuits



Component ID	Value	Description
C1-C8	100 pF	50V ±20% Single Layer Chip Capacitor (500U01A101MT4W)
C9-C12	10 nF	100V ±20% Single Layer Chip Capacitor (V30BZ103M1SX)
C13-C16	10 nF	50V ±5% 0402 Multilayer Ceramic Capacitor
C17-C20	10 µF	35V ±10% 0805 Multilayer Ceramic Capacitor
R1, R2	100 kΩ	±5% 0402 Resistor

Figure 3-2. Assembly Drawing



Assembly Guidance

Amplifier must be biased from both sides.

Optimum RF power performance achieved by minimizing output RF bond wire length.

Interconnect assembly notes:

- Die suitable for ball or wedge bonding.
- Force, time, and ultrasonic parameters are critical.
- Aluminum wire bonding is not recommended.
- Bond wire diameter of 1 mil is recommended.

Die attach of component using adhesive:

- Vacuum collets are the preferred method of pickup.
- Pickup method must consider the avoidance of die air bridges.
- Die suitable for eutectic and epoxy die attach.
- Where epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:
 - Namics H9890–11
 - Kyocera CT2700R7S

Reflow Process

- Maximum temperature 320 °C for 30 seconds.
- Material matching for Coefficient of thermal expansion is crucial for long-term reliability

Bias-Up Procedure

1. Set VG = -5V
2. Set VD to 20V – 24V
3. Adjust VG positive until ID quiescent is 112 mA
4. Limit ID to 2A
5. Apply RF Signal

Bias-down Procedure

1. Turn off RF.
2. Turn off VD, allow drain capacitor to discharge.
3. Turn off VG.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. Class 1A HBM (250V – 500V) ESD Classification is anticipated.

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Standard Packing Format
ICP2840	Die	Gel Pack
ICP2840-1-110I	Die	Gel Pack
ICP2840-1-100I	Die	Wafer frame

5. Revision History

Table 5-1. Revision History

Revision	Date	Description
B	12/2021	Updated part number to ICP2840 (previously GMICP2731-10).
A	06/2021	Document created.

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- Embedded Solutions Engineer (ESE)
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Technical support is available through the website at: www.microchip.com/support

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