Integrated
Circuit
Systems, Inc.

ICS1523

High-Performance Programmable Line-Locked Clock Generator

General Description

The **ICS1523** is a low-cost but very high-performance frequency generator for line-locked and genlocked high-resolution video applications. Using ICS's advanced low-voltage CMOS mixed-mode technology, the **ICS1523** is an effective clock solution for video projectors and displays at resolutions from VGA to beyond UXGA.

The **ICS1523** offers pixel clock outputs in both differential (to 250 MHz) and single-ended (to 150 MHz) formats. Dynamic Phase Adjust™ circuitry allows user control of the pixel clock phase relative to the recovered sync signal. A second differential output at half the pixel clock rate enables deMUXing of multiplexed analog-to-digital converters. The FUNC pin provides either the regenerated input from the phase-locked loop (PLL) divider chain output or a re-synchronized and sharpened input HSYNC.

The advanced PLL uses either its internal programmable feedback divider or an external divider. The device is programmed by a standard I²C-bus™ serial interface and is available in a 24-pin wide small-outline integrated circuit (SOIC) package.

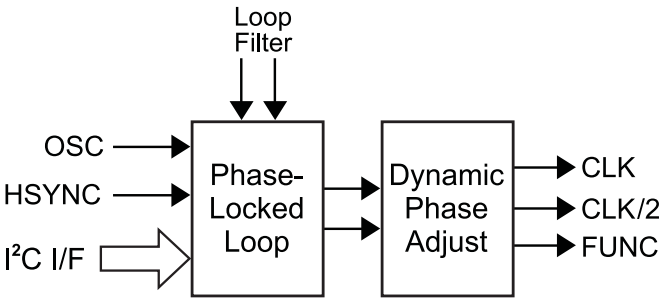
Features

- Pixel clock frequencies up to 250 MHz
- Very low jitter
- Dynamic Phase Adjust (DPA) for clock outputs
- Balanced PECL differential outputs
- Single-ended SSTL_3 clock outputs
- Double-buffered PLL/DPA control registers
- Independent software reset for PLL/DPA
- External or internal loop filter selection
- Uses 3.3Vdc. Inputs are 5V-tolerant.
- I²C-bus™ serial interface can run at either low speed (100 kHz) or high speed (400 kHz).
- Lock detection
- 24-pin 300-mil SOIC package

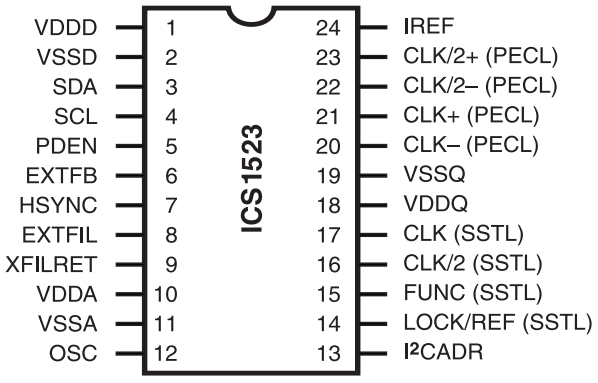
Applications

- LCD monitors and video projectors
- Genlocking multiple video subsystems
- Frequency synthesis

Block Diagram



Pin Configuration



24-Pin SOIC

I²C-bus is a trademark of Philips Corporation.
Dynamic Phase Adjust is a trademark of Integrated Circuit Systems, Inc.

Document Revision History

Rev P (First Release)

Pin Descriptions changed to add type column. (pg 3)
Added SDA and AC Input Characteristics. (pg 18)
Changed VCO Output, Intrinsic Jitter graph to show slow and fast cases (pg 19)
Timing diagram changes to reference t0 to REF and notes on test conditions added (pg 22)
Lock Renamed Lock/Ref (Throughout).
General cleanup for readability.

Rev Q

Added typical external loop filter values. (pg 17)
Added section on power supply considerations and SSTL_3 outputs. (pg 18)
Correct labels and scale on VCO Output, Intrinsic Jitter graph. (pg 20)
Correct depiction of timing diagram and added typical transition timing. (pg 23)
Added Document Revision History. (pg 25)

Rev R

Change to descriptions for pins 20 to 23. (pg 3)
Change to description for Reg 0h bits 0 and 1, added table. (pg 6)
Within table for Reg 0h bits 6 and 7, changed Osc_En to IN_SEL . (pg 6)
Moved Reg 0 bits 4 through 7 from pg 6 to new pg 7.
Change to Software Programming Flow diagram. (pg 13).
Added under Absolute Maximum Ratings ESD ratings and warning. (pg 19)
Under Recommend Operating Conditions, PECL Outputs, Output Low Voltage, added a note and added a new page. (pg 19)
Under Recommend Operating Conditions, SSTL-3 Outputs, Output Low Voltage, changed direction of symbols. (pg 19)
Change to VCO Output Frequency and Intrinsic Jitter graph to reflect correct VCO frequency (pg 20)

Rev S

Moved Revision History from last page of data sheet to second page. (pg 2)
In Layout Guideline 2, changed shunt capacitor value from 150 pF to 33 pF. (pg 19)
Changed various cross-references within Layout Guidelines. (pg 19)

Overview

The ICS1523 addresses stringent graphics system line-locked and genlocked applications and provides the clock signals required by high-performance video analog-to-digital converters. Included are a phase-locked loop (PLL) with a 500-MHz voltage controlled oscillator (VCO), a Dynamic Phase Adjust to provide a user-programmed pixel clock delay, the means for deMUXing multiplexed ADCs, and both balanced-programmable (PECL) and single-ended (SSTL_3) high-speed clock outputs.

Phase-Locked Loop

The phase-locked loop is optimized for line-locked applications, for which the inputs are horizontal sync signals. A high-performance Schmitt trigger preconditions the HSYNC input, whose pulses can be degraded if they are from a remote source. This preconditioned HSYNC signal is provided as a clean reference signal with a short transition time. (In contrast, the signal that a typical PC graphics card provides has a transition time of tens of nanoseconds.)

A second high-frequency input such as a crystal oscillator and a 7-bit programmable divider can be selected. This selection allows the loop to operate from a local source and is also useful for evaluating intrinsic jitter.

A 12-bit programmable feedback divider completes the loop. Designers can substitute an external divider.

Either the conditioned HSYNC input or the loop output (recovered HSYNC) is available at the FUNC pin, aligned to the edge of the pixel clock.

Automatic Power-On Reset Detection

The ICS1523 has automatic power-on reset detection circuitry and it resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.

Dynamic Phase Adjust™

The Dynamic Phase Adjust™ allows addition of a programmable delay to the pixel clock output, relative to the recovered HSYNC signal. The ability to add delays is particularly useful when multiple video sources must be synchronized. A delay of up to one pixel clock period is selectable in the following increments:

- 1/64 period for pixel clock rates to 40 MHz
- 1/32 period for pixel clock rates to 80 MHz
- 1/16 period for pixel clock rates to 160 MHz

Output Drivers and Logic Inputs

The ICS1523 utilizes low-voltage TTL (LVTTL) inputs as well as SSTL_3 (EIA/JESD8-8) and low-voltage PECL (pseudo-ECL) outputs, operating at 3.3-V supply voltage. The LVTTL inputs are 5 V-tolerant. The SSTL_3 and differential PECL output drivers drive resistive terminations or transmission lines. At lower clock frequencies, the SSTL_3 outputs can be operated unterminated.

I^2C-bus™ Serial Interface

The ICS1523 utilizes the industry-standard I^2C-bus™ serial interface. The interface uses 12 registers: one write-only, eight read/write, and three read-only. Two ICS1523 devices can be addressed, according to the state of the I^2CADR pin. When the pin is low, the read address is 4Dh, and the write address is 4Ch. When the pin is high, the read address is 4Fh, and the write address is 4Eh. The I^2C-bus serial interface can run at either low speed (100 kHz) or high speed (400 kHz) and provides 5V-tolerant input.

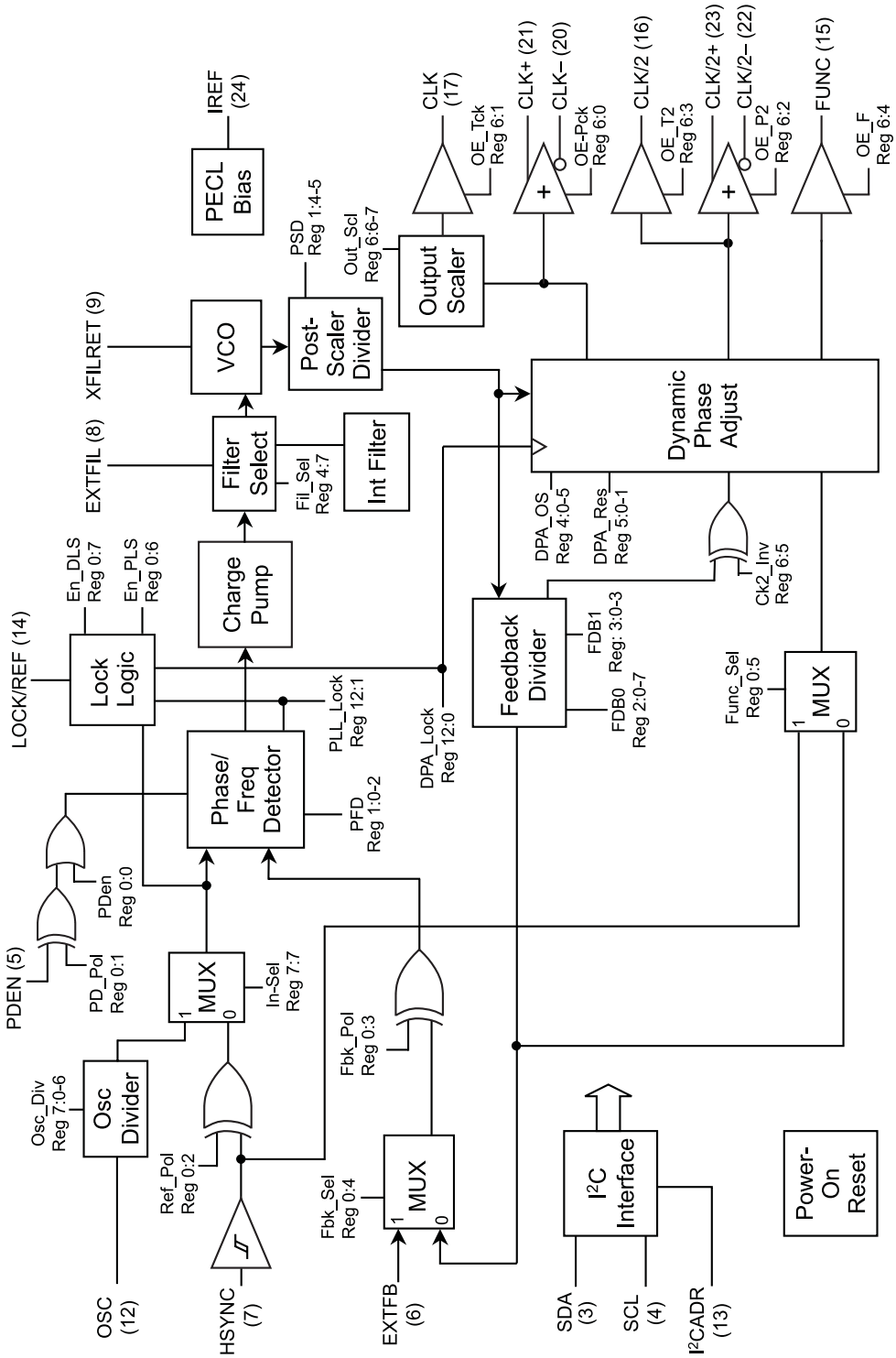
Pin Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION	COMMENTS
1	VDDD	PWR	Digital supply	3.3V to digital sections
2	VSSD	PWR	Digital ground	
3	SDA	IN/OUT	Serial data	I²C-bus[1]
4	SCL	IN	Serial clock	I²C-bus[1]
5	PDEN	IN	PFD enable	Suspends charge pump[1]
6	EXTFB	IN	External feedback in	External divider input to PFD[1]
7	HSYNC	IN	Horizontal sync	Clock input to PLL[1]
8	EXTFIL	IN	External filter	External PLL loop filter
9	XFILRET	IN	External filter return	External PLL loop filter return
10	VDDA	PWR	Analog supply	3.3V for analog circuitry
11	VSSA	PWR	Analog ground	Ground for analog circuitry
12	OSC	IN	Oscillator	Input from crystal oscillator package[1, 2]
13	I²CADR	IN	I²C address	Chip I²C address select Low = 4Dh read, 4Ch write High = 4Fh read, 4Eh write
14	LOCK/REF (SSTL)	OUT	Lock indicator/reference	Displays PLL or DPA lock or REF input
15	FUNC (SSTL)	OUT	Function output	SSTL_3 selectable HSYNC output
16	CLK/2 (SSTL)	OUT	Pixel clock/2 out	SSTL_3 driver to ADC deMUX input
17	CLK (SSTL)	OUT	Pixel clock out	SSTL_3 driver to ADC
18	VDDQ	PWR	Output driver supply	3.3V to output drivers
19	VSSQ	PWR	Output driver ground	Ground for output drivers
20	CLK– (PECL)	OUT	Pixel clock out	Inverted PECL driver to ADC. Open drain.
21	CLK+ (PECL)	OUT	Pixel clock out	PECL driver to ADC. Open drain.
22	CLK/2– (PECL)	OUT	Pixel clock/2 out	Inverted PECL driver to ADC deMUX input. Open drain.
23	CLK/2+ (PECL)	OUT	Pixel clock/2 out	PECL driver to ADC deMUX input. Open drain.
24	IREF	IN	Reference current	Reference current for PECL outputs

Notes:

1. These LVTTL inputs are 5V-tolerant.
2. Connect to ground if unused.

Block Diagram



I²C Register Map Summary

Register Index	Name	Access	Bit Name	Bit #	Reset Value	Description
0h	Input Control	R / W	PDen	0	1	Phase Detector Enable (0=External Enable, 1=Always Enabled)
			PD_Pol	1	0	Phase Detector Enable Polarity (0=Not Inverted, 1=Inverted)
			Ref_Pol	2	0	External Reference Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Pol	3	0	External Feedback Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Sel	4	0	External Feedback Select (0=Internal Feedback, 1=External)
			Func_Sel	5	0	Function Out Select (0=Recovered HSYNC, 1=Input HSYNC)
			EnPLS	6	1	Enable PLL Lock/Ref Status Output (0=Disable 1=Enable)
			EnDLS	7	0	Enable DPA Lock/Ref Status Output (0=Disable 1=Enable)
1h	Loop Control	R / W *	PFD0-2	0-2	0	Phase Detector Gain
			Reserved	3	0	Reserved
			PSD0-1	4-5	0	Post-Scaler Divider (0 = ÷2, 1 = ÷4, 2 = ÷8, 3 = ÷16)
			Reserved	6-7	0	Reserved
2h	FdBk Div 0	R / W *	FBD0-7	0-7	FF	PLL FeedBack Divider LSBs (bits 0-7) *
3h	FdBk Div 1	R / W *	FBD8-11	0-3	F	PLL Feedback Divider MSBs (bits 8-11) *
			Reserved	4-7	0	Reserved
4h	DPA Offset	R / W	DPA_OS0-5	0-5	0	Dynamic Phase Aligner Offset
			Reserved	6	0	Reserved
			Fil_Sel	7	0	Loop Filter Select (0=External, 1=Internal)
5h	DPA Control	R / W **	DPA_Res0-1	0-1	3	DPA Resolution (0=16 delay elements, 1=32, 2=Reserved, 3=64)
			Metal_Rev	2-7	0	Metal Mask Revision Number
6h	Output Enables	R / W	OE_Pck	0	0	Output Enable for PECL PCLK Outputs (0=High Z, 1=Enabled)
			OE_Tck	1	0	Output Enable for STTL_3 CLK Output (0=High Z, 1=Enabled)
			OE_P2	2	0	Output Enable for PECL CLK/2 Outputs (0=High Z, 1=Enabled)
			OE_T2	3	0	Output Enable for STTL_3 CLK/2 Output (0=High Z, 1=Enabled)
			OE_F	4	0	Output Enable for STTL_3 FUNC Output (0=High Z, 1=Enabled)
			Ck2_Inv	5	0	CLK/2 Invert (0=Not Inverted, 1= Inverted)
			Out_Scl	6-7	0	SSTL Clock Scaler (0 = ÷1, 1 = ÷2, 2 = ÷4, 3 = ÷8)
7h	Osc_Div	R / W	Osc_Div 0-6	0-6	0	Osc Divider modulus
			In-Sel	7	1	Input Select (0=HSYNC Input, 1=Osc Divider)
8h	Reset	Write	DPA	0-3	x	Writing xAh resets DPA and loads working register 5
			PLL	4-7	x	Writing 5xh resets PLL and loads working registers 1-3
10h	Chip Ver	Read	Chip Ver	0-7	17	Chip Version 23 Dec (17 Hex) as in 1523
11h	Chip Rev	Read	Chip Rev	0-7	01	Initial value 01h. Value Increments with each all-layer change.
12h	Rd_Reg	Read	DPA_Lock	0	N/A	DPA Lock Status (0=Unlocked, 1=Locked)
			PLL_Lock	1	N/A	PLL Lock Status (0=Unlocked, 1=Locked)
			Reserved	2-7	0	Reserved

* Identifies double-buffered registers. Working registers are loaded during software PLL reset.

** Identifies double-buffered register. Working registers are loaded during software DPA reset.

Detailed Register Description

Name: Input Control
Register: 0 h
Index: Read / Write

Bit Name	Bit #	Reset Value	Description
PDen	0	1	Phase/Frequency Detector Enable
PD_Pol	1	0	Phase/Frequency Detector Enable Polarity
Ref_Pol	2	0	Phase/Frequency Detector External Reference Polarity
Fbk_Pol	3	0	External Reference Feedback Polarity
Fbk_Sel	4	0	External Feedback Select
Func_Sel	5	0	Function Output Select
EnPLS	6	1	Enable PLL Lock Status Output on LOCK/REF pin
EnDLS	7	0	Enable DPA Lock Status Output on LOCK/REF pin

Bit	Name	Description
0	PDen	Phase/Frequency Detector Enable
1	PD_Pol	Phase/Frequency Detector Enable Polarity

PDen	PD_Pol	Phase/Frequency Detector Is Enabled When:
0	0	PDEN= 1
X	1	Always (Default)
1	0	PDEN = 0

2 Ref_Pol — Phase/Frequency Detector External Reference Polarity — Edge of input signal on which Phase Detector triggers.
0 = Rising Edge (default)
1 = Falling Edge

3 Fbk_Pol — External Reference Feedback Polarity — Edge of EXTFB (pin 6) signal on which Phase/Frequency Detector triggers when external feedback is used (Reg0 [4]=1).
0 = Positive Edge (default)
1 = Negative Edge

Table continues on next ppage

Name: Input Control
Register: 0h

Bit	Name	Description
4	Fbk_Sel	External Feedback Select 0 = Internal Feedback (default) 1 = External Feedback
5	Func_Sel	Function Output Select — Selects re-clocked output to FUNC (pin 15). 0 = Recovered HSYNC (default). Re-generated HSYNC output. 1 = External HSYNC. Schmitt-trigger conditioned input from HSYNC (pin 7).
6	EnPLS	Enable PLL Lock Status Output on LOCK/REF pin
7	EnDLS	Enable DPA Lock Status Output on LOCK/REF pin Bits 6,7 enable multiple functions at LOCK/REF, (pin 14)

EnPLS	EnDLS	IN_SEL	LOCK/REF(14)
0	0	N/A	0
0	1	N/A	1 if DPA locked, 0 otherwise
1	0	N/A	1 if PLL locked, 0 otherwise
1	1	0	Post Schmitt trigger HSYNC(7) XOR Ref_Pol
1	1	1	F_{osc} ÷ Osc_Div

Name: Loop Control Register
Register: 1h
Index: Read/Write*

Bit Name	Bit #	Reset Value	Description
PFD0-2	0-2	0	Phase Frequency Detector Gain
Reserved	3	0	Reserved
PSD0-1	4-5	0	Post-Scaler Divider
Reserved	6-7	0	Reserved

Bit Name Description

0-2 PFD0-2 Phase/Frequency Detector Gain

Bit 2	Bit 1	Bit 0	PFD Gain (µA/2π rad)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

3 Reserved

4-5 PSD0-1 Post-Scaler Divider — Divides the output of the VCO to the DPA and Feedback Divider.

Bit 5	Bit 4	PSD Divider
0	0	2 (default)
0	1	4
1	0	8
1	1	16

6-7 Reserved

* Double-buffered register. Actual working registers are loaded during software PLL reset. See register 8h for details.

Name: Feedback Divider 0 Register / Feedback Divider 1 Register
Register: 2h, 3h
Index: Read/Write*

Bit Name	Index	Bit #	Reset Value	Description
FBD 0-7	2	0-7	FF	PLL Feedback Divider LSBs (0-7).* When Bit 0 = 0, then the total number of pixels is even. When Bit 0 = 1, then the total number of pixels is odd.
FBD 8-11	3	0-3	F	PLL Feedback Divider MSBs (8-11)*
Reserved	3	4-7		Reserved

The value that is programmed into these two registers, plus a value of 8, defines the total number of clock periods that the ICS 1523 generates between HSYNCs. Program these registers with the total number of horizontal pixels per line minus 8.

Feedback Divider Modulus =

Reg 3				Reg 2							
3	2	1	0	7	6	5	4	3	2	1	0

+8

$12 \leq$ Feedback Divider Modulus ≤ 4103

* Double-buffered registers. Actual working registers are loaded during software PLL reset. See Register 8h for details.

Name: DPA Offset Register
Register: 4h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
DPA_OS0-5	0-5	0	Dynamic Phase Adjust Offset
Reserved	6	0	Reserved
Fil_Sel	7	0	Loop Filter Select

Bit	Name	Description
0-5	DPA_OS0-5	Dynamic Phase Adjust Offset. Selects clock edge offset in discrete steps from zero to one clock period minus one step. Resolution (number of delay elements per clock cycle) is selected by DPA_Res0-1 (Reg 5:0-1). Note: Offsets equal to or greater than one clock period are neither recommended nor supported. Example: For DPA_Res0-1=01H, the clock can be delayed from 0 to 31 steps.
7	Fil_Sel	Selects external loop filter (0) or internal loop filter (1). The use of an external loop filter is strongly recommended for all designs. Suggested component values are available from the *ICS1523 Demo Board Guide (1523DB.pdf)* or the ICS1523 Register Tool (inst1523.exe) available on our web site at: (http://www.icst.com/products/pinfo/1523.htm).

Name: DPA Control Register
Register: 5h
Index: Read/Write*

Bit Name	Bit #	Reset Value	Description
DPA_Res0-1	0-1	3	Dynamic Phase Adjust Resolution Select.
Metal_Rev	2-7	0	Metal Mask Revision Number.

Bit	Name	Description
0-1	DPA_Res0-1	Dynamic Phase Adjust (DPA) Resolution Select. It is not recommended to use the DPA above 160 MHz.

Bit 1	Bit 0	Delay Elements	CLK Range, MHz
0	0	16	48 – 160
0	1	32	24 – 80
1	0	Reserved	
1	1	64	12 – 40

2-7	Metal_Rev	Metal Mask Revision Number. After power-up, register bits 7:2 must be written with 111111. After this write, a read indicates the metal mask revision, as below.

Revision	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
A	1	1	1	1	1	1
B	0	1	1	1	1	1
C1	1	0	1	1	1	1
C2	0	0	1	1	1	1
D	1	1	0	1	1	1
E	1	1	1	0	1	1
F	1	1	1	1	0	1
G	1	1	1	1	1	0

* Double-buffered register. Actual working registers are loaded during software DPA reset. See register 8h for details.

Name: Output Enable Register
Register: 6 h
Index: Read / Write

Bit Name	Bit #	Reset Value	Description
OE_Pck	0	0	Output Enable for CLK Outputs (PECL)
OE_Tck	1	0	Output Enable for CLK Output (SSTL_3)
OE_P2	2	0	Output Enable for CLK/2 Outputs (PECL)
OE_T2	3	0	Output Enable for CLK2 Output (SSTL_3)
OE_F	4	0	Output Enable for FUNC Output (SSTL_3)
Ck2_Inv	5	0	CLK/2 Invert
Out_Scl	6-7	0	CLK Scaler

Bit	Name	Description
0	OE_Pck	Output Enable for CLK Outputs (PECL) 0 = High Z 1 = Enabled
1	OE_Tck	Output Enable for CLK Output (SSTL_3) 0 = High Z 1 = Enabled
2	OE_P2	Output Enable for CLK/2 Outputs (PECL) 0 = High Z 1 = Enabled
3	OE_T2	Output Enable for CLK/2 Output (SSTL_3) 0 = High Z 1 = Enabled
4	OE_F	Output Enable for FUNC Output (SSTL_3) 0 = High Z 1 = Enabled
5	Ck2_Inv	CLK/2 Invert 0 = Not Inverted 1 = Inverted
6-7	Out_Scl	Clock (CLK) Scaler

Bit 7	Bit 6	CLK Divider
0	0	1
0	1	2
1	0	4
1	1	8

Name: Oscillator Divider Register
Register: 7h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
Osc_Div 0-6	0-6	0	Osc Divider Modulus
In_Sel	7	1	Input Select

Bit	Name	Description
0-6	Osc_Div 0-6	Oscillator Divider Modulus. Divides the input from OSC (pin 12) by the set modulus. The modulus equals the programmed value, plus 2. Therefore, the modulus range is from 3 to 129.
7	In_Sel	Input Select — Selects the input to the Phase/Frequency Detector 0 = HSYNC 1 = Osc Divider

Name: RESET Register
Register: 8h
Index: Write

Bit Name	Bit #	Reset Value	Description
DPA Reset	0-3	x	Writing xAh to this register resets DPA working register 5
PLL Reset	4-7	x	Writing 5xh to this register resets PLL working registers 1-3

Bit	Name	Description
0-3	DPA	Writing xAh to this register resets DPA working register 5
4-7	PLL	Writing 5xh to this register resets PLL working registers 1-3

Value	Resets
xA	DPA
5x	PLL
5A	DPA and PLL

Name: Chip Version Register
Register: 10h
Index: Read

Bit Name	Bit #	Reset Value	Description
Chip Ver	0-7	17	Chip Version 23 (17h)

Name: Chip Revision Register
Register: 11h
Index: Read

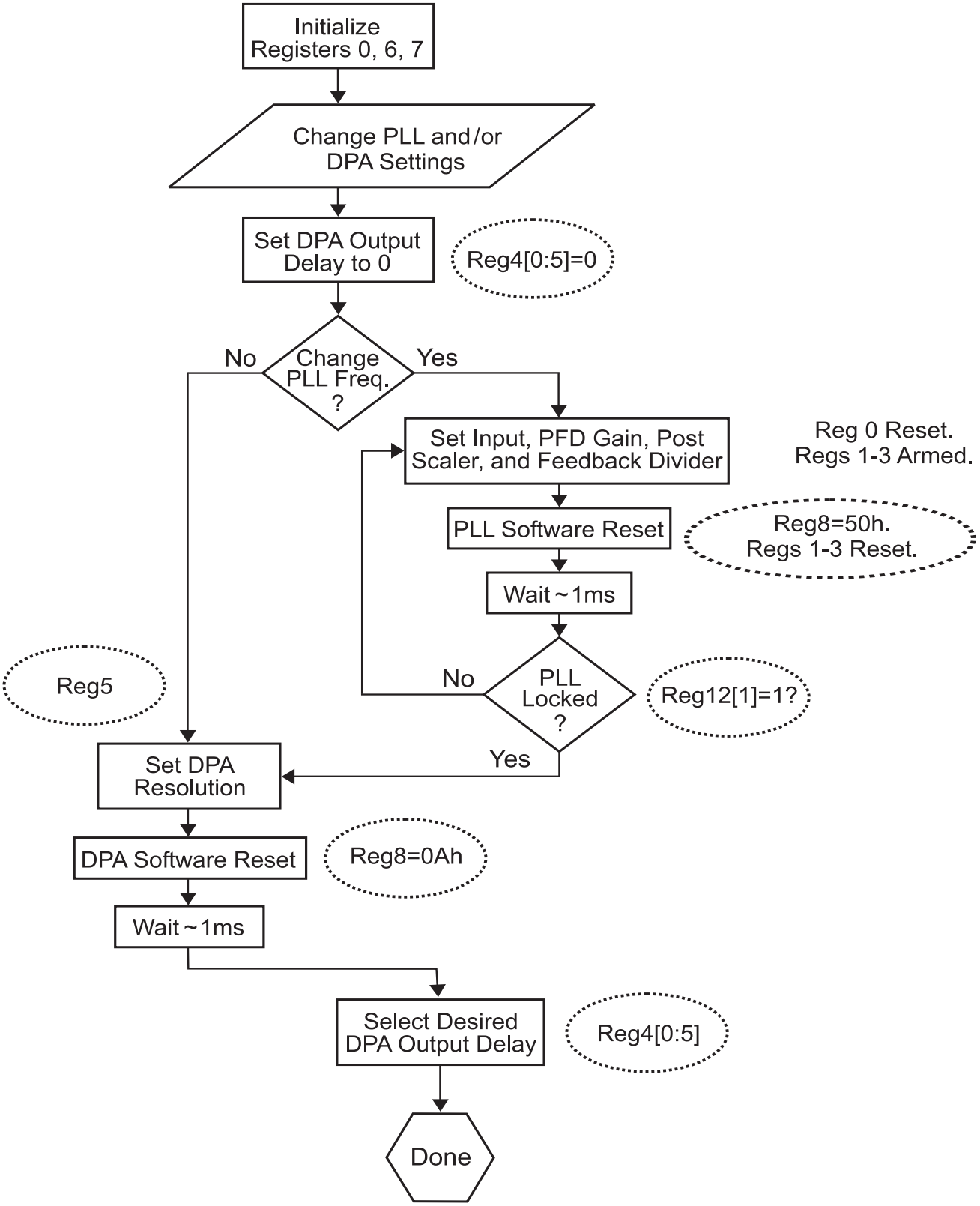
Bit Name	Bit #	Reset Value	Description
Chip Rev	0-7	01+	Initial value 01h. +Value increments with each all-layer change.

Name: Status Register
Register: 12h
Index: Read

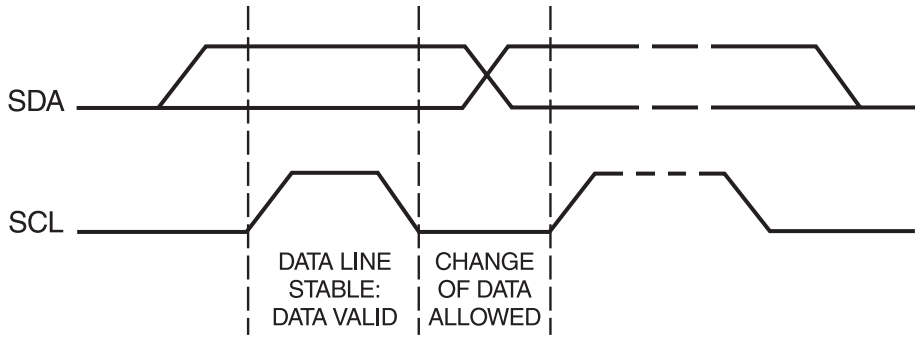
Bit Name	Bit #	Reset Value	Description
DPA_Lock	0	N/A	DPA Lock Status
PLL_Lock	1	N/A	PLL Lock Status
Reserved	2-7	0	Reserved

Bit	Name	Description
0	DPA_Lock	DPA Lock Status. (Refer to Register 0h, bits 6 and 7.) 0 = Unlocked 1 = Locked
1	PLL_Lock	PLL Lock Status. (Refer to Register 0h, bits 6 and 7.) 0 = Unlocked 1 = Locked
2-7	Reserved	

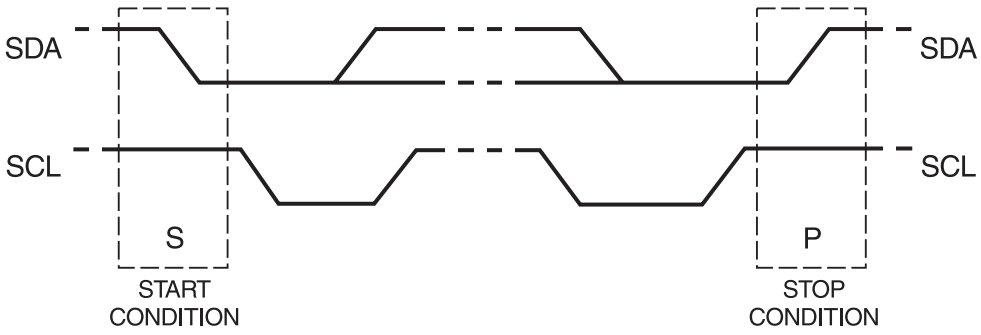
ICS1523 Software Programming Flow



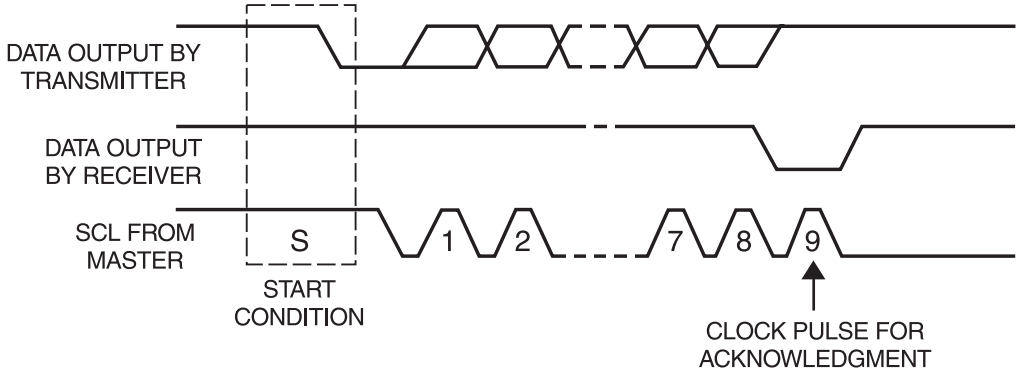
I²C Data Characteristics



Bit transfer on the I²C-bus



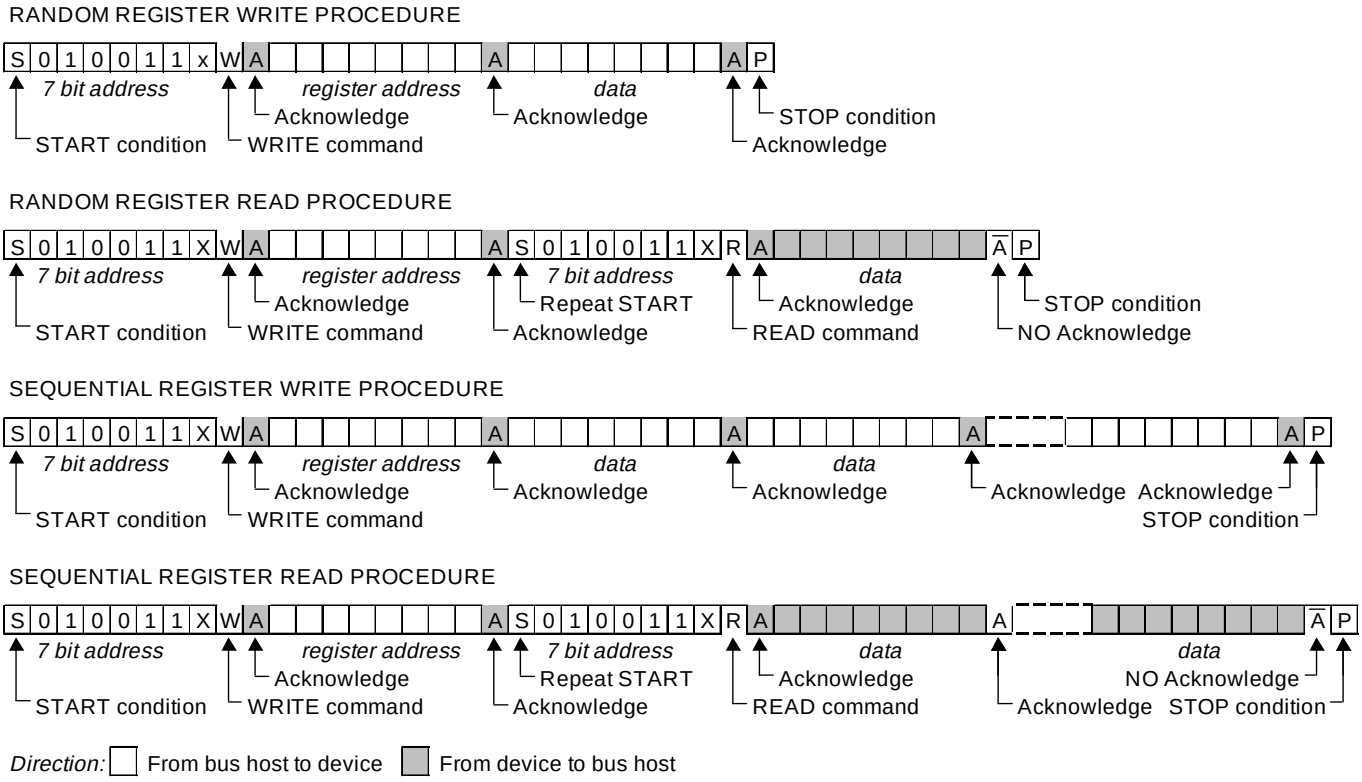
START and STOP conditions



Acknowledge on the I²C-bus

These waveforms are from "The I2C-bus and how to use it," published by Philips Semiconductor.
The document can be obtained from http://www-us2.semiconductors.philips.com/acrobat/various/i2c_bus_specification_1995.pdf

I²C Data Format



Note:

1. All values are transmitted with the most-significant bit first and the least-significant bit last.
2. The value of the X bit equals the logic state of pin 13 (I^2CADR).
3. R = READ = 1 and W = WRITE = 0

ICS1523 Video Mode Reference Table

The use of an external loop filter is strongly recommended in <u>All Designs</u>.

The ICS1523 Video Mode Reference Table (previously included in this data sheet) lists information on the various video modes that can be used with the ICS1523. To reference this table, see the *ICS1523 Demo Board Guide (1523DB.pdf)* available on our web site at: (http://www.icst.com) under the ICS1523 area.

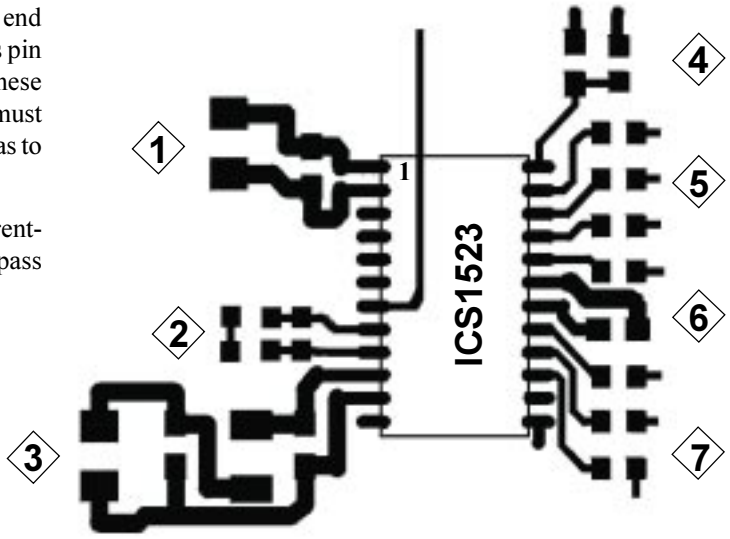
General Layout Guidelines

- Use a PC board with at least four layers: one power, one ground, and two signal.
- No special cutouts are required for power and ground planes.
- All supply voltages must be supplied from a common source and must ramp up together.
- Flux and other board surface debris can degrade the performance of the external loop filter. Ensure that the 1523 area of the board is free of contaminants.

Specific Layout Guidelines

1. **Digital Supply (VDD) –** Bypass pin 1 (VDD) to pin 2 (VSS) with 4.7-µF and 0.1-µF capacitors, located as close as possible to the pins. Traces must be maximally wide and include multiple surface-etched vias to the appropriate plane.
2. **External Loop Filter – The use of an external loop filter is strongly recommended in <u>All Designs</u>.** Locate loop filter components as close to pins 8 and 9 (EXTFIL and EXTFILRET) as possible. Typical loop filter values are 6.8K Ω for the series resistor, 3300 pF RF-type capacitor for the series capacitor, and 33 pF for the shunt capacitor. (For details, see the *Frequently Asked Questions* part of the *ICS1523 Applications Guide*, FAQ2 and FAQ3.).
3. **Analog PLL Supply (VDDA) –** Decouple pin 10 (VDDA) with a series ferrite bead. Bypass the supply end of the bead with 4.7-µF and 0.1-µF capacitors. Bypass pin 10 to pin 11 (VSSA) with a 0.1-µF capacitor. Locate these components as close as possible to the pins. Traces must be maximally wide and have multiple surface-etched vias to the power or ground planes.
4. **PECL Current Set Resistor –** Locate PECL current-set resistor as close as possible to pin 24 (IREF). Bypass pin 24 to ground with a 0.1-µF capacitor.
5. **PECL Outputs –** Implement these outputs as microstrip transmission lines. The trace widths shown are for 75 Ω characteristic impedance, presuming .067 in. between layers. Locate the optional series "snubbing" resistors as close as possible to the pins. If the termination resistors are included on-board, locate them as close as possible to the load and connect directly to the power and ground planes.

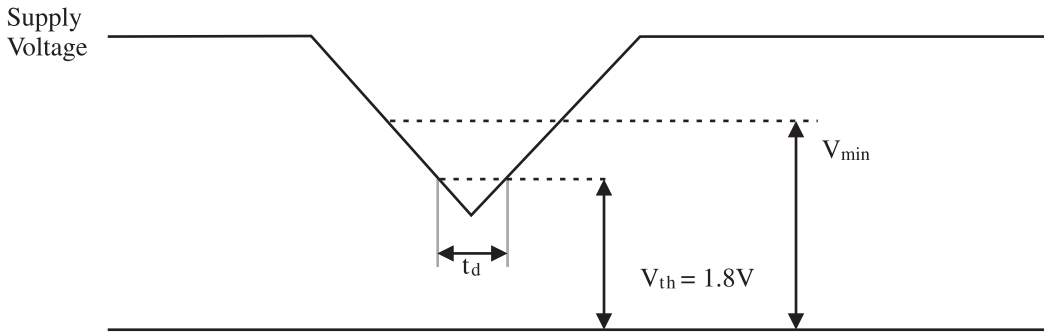
   [These termination resistors are omitted if the load device implements them internally. For details, see the ICS application note on microstrip and striplines (1572AN1) and within the *ICS1523 Applications Guide*, the application note on *Designing a Custom Interface for the ICS1523* (1523AN4.)]
6. **Output Driver Supply –** Bypass pin 18 (VDDQ) to pin 19 (VSSQ) with 4.7-µF and 0.1-µF capacitors, located as close as possible to the pins. Traces must be maximally wide and include multiple surface-etched vias to the appropriate plane.
7. **SSTL_3 Outputs –** SSTL_3 outputs can be used like conventional CMOS rail-to-rail logic or as a terminated transmission line system at higher-output frequencies. With terminated outputs, the considerations of item 5, "PECL Outputs" apply. See JEDEC documents JESD8-A and JESD8-8.



Note: Drawing is not to scale. It is for illustrative purposes only.

Power Supply Considerations

The ICS1523 incorporates special internal power-on reset circuitry that requires no external reset signal connection. The supply voltage (VDD) must remain within the recommended operating conditions during normal operation. To reset the ICS1523, the supply voltage at the part must be reduced below the threshold voltage (V_{th}) of the power-on reset circuit. The supply voltage must remain below that threshold voltage such that board power conditioning capacitors are drained and the proper reset state is latched. The amount of time (t_d) to hold the voltage in a reset state varies with the design. However, a typical value of 10 ms should be sufficient.



SSTL_3 Outputs

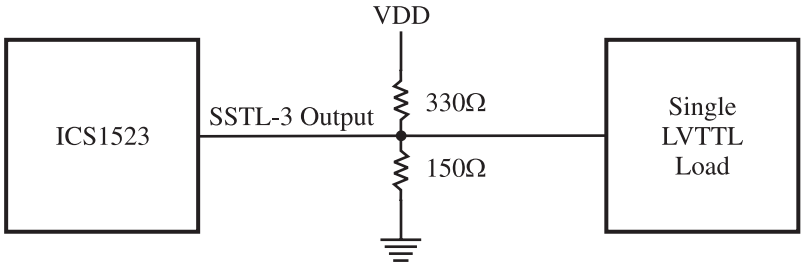
Unterminated Outputs

In the ICS1523, unterminated SSTL output pins display exponential transitions similar to those of rectangular pulses presented to RC loads. The 10-90% rise time is typically 1.6 ns, and the corresponding fall time is typically 700 ps. In turn, this asymmetry contributes to duty cycle asymmetry at higher output frequencies. In the absence of significant load capacitance (which can further increase rise and fall time), this asymmetry is the dominant factor determining high-frequency performance of these single-ended outputs. Typically, no termination is required either for the LOCK/REF, FUNC, and CLK/2 outputs or for CLK outputs up to approximately 135 MHz.

Terminated Outputs

SSTL_3 outputs are intended to terminate in low impedances to reduce the effect of external circuit capacitance. Use of transmission line techniques enables use of longer traces between source and driver without increasing ringing due to reflections. Where external capacitance is minimal and substantial voltage swing is required to meet LVTTL V_{IH} and V_{OL} requirements, the intrinsic rise and fall times of ICS1523 SSTL outputs are only slightly improved by termination in a low impedance.

The ICS1523 SSTL output source impedance is typically less than 60Ω. Termination impedance of 100Ω reduces output swing by less than 30% which is more than enough to drive a single load of LVTTL inputs.



Absolute Maximum Ratings

VDD, VDDA, VDDQ (measured to VSS)	4.3V
Digital Inputs	VSS – 0.3V to 5.5V
Analog Outputs	VSSA – 0.3V to VDDA +0.3V
Digital Outputs	VSSQ – 0.3V to VDDQ +0.3V
Storage Temperature	– 65°C to +150°C
Junction Temperature	175°C
Soldering Temperature	260°C
ESD Susceptibility*	> 2 KV

(*Electrostatic-sensitive devices. Do not open or handle except in a static-free workstation.)

Recommended Operating Conditions

VDD, VDDQ, VDDA (measured to VSS) . . 3.0 to 3.6 V
Operating Temperature (Ambient) . . . . . 0 to +70°C

DC Supply Current

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Current, Digital	IDDD	VDDD = 3.6V	—	25	mA
Supply Current, Output Drivers	IDDQ	VDDQ = 3.6V, no output drivers enabled.	—	6	mA
Supply Current, Analog	IDDA	VDDA = 3.6V	—	5	mA

Digital Inputs (SDA, SCL, PDEN, EXTFB, HSYNC, OSC, I^2CADR)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	VIH		2	5.5	V
Input Low Voltage	VIL		VSS-0.3	0.8	V
Input Hysteresis			0.2	0.6	V
Input High Current	IIH	V_{IH} = VDD	—	±10	µA
Input Low Current	IIL	V_{IL} = 0	—	±200	µA
Input Capacitance	Cin		—	10	pF

SDA (In Output Mode: SDA is Bidirectional)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Low Voltage	VOL	IOUT = 3 mA. VOH = 6.0V maximum as determined by the external pull-up resistor.		0.4	V

PECL Outputs (CLK+, CLK–, CLK/2+, CLK/2–)

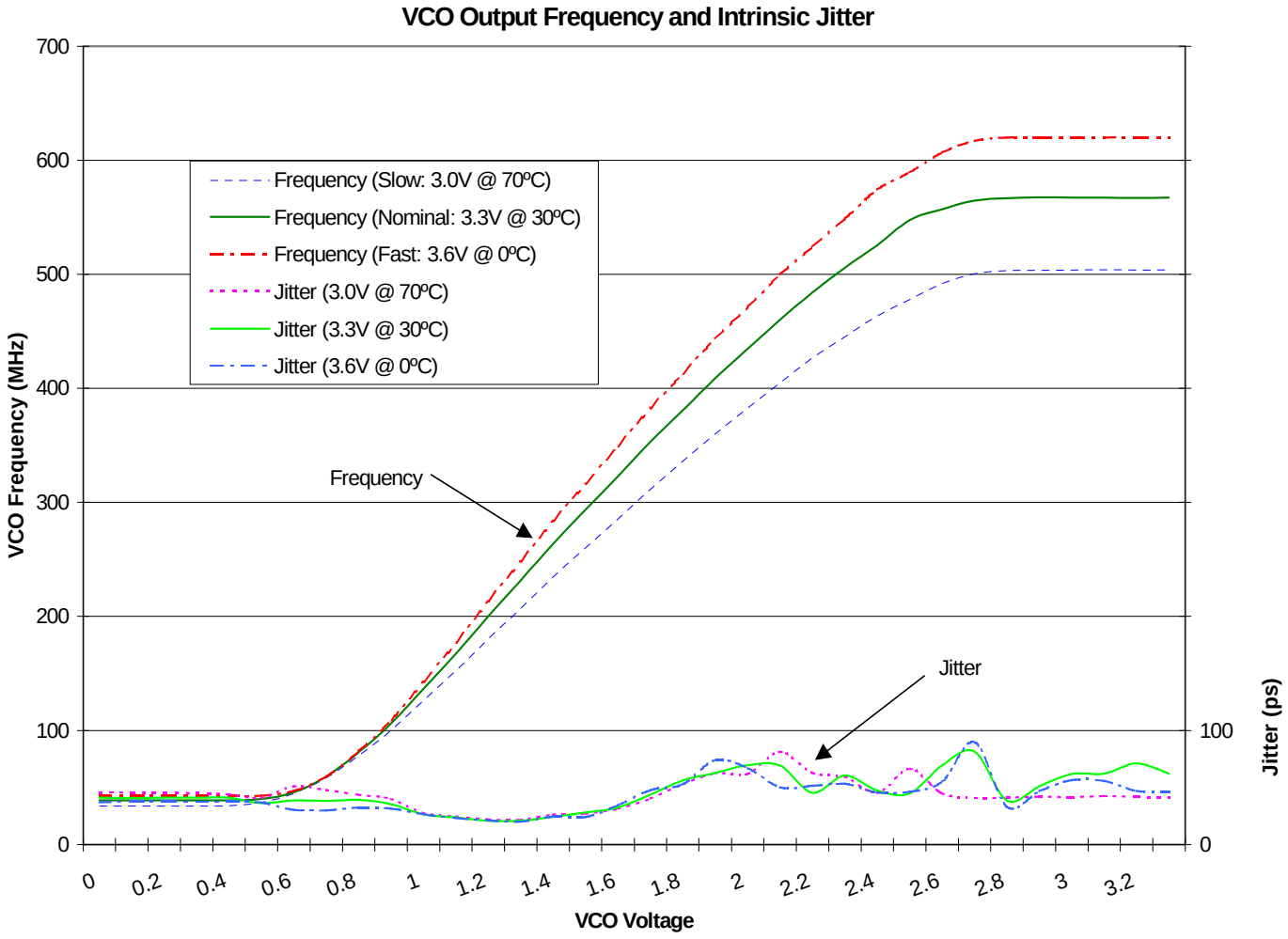
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage	VOH	IOUT = 0	—	VDD	V
Output Low Voltage (Note: VOL must not fall below the level given so that the correct value for IOUT can be maintained.)	VOL	IOUT = programmed value	1.0	—	V

SSTL-3 Outputs (CLK, CLK/2, FUNC, LOCK/REF)

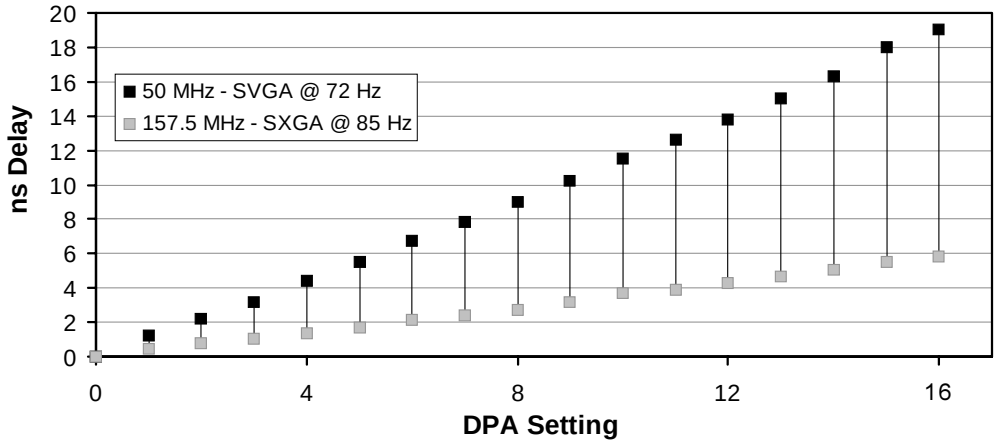
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Resistance	R_O	1 <V_O<2V	—	80	Ω

AC Input Characteristics

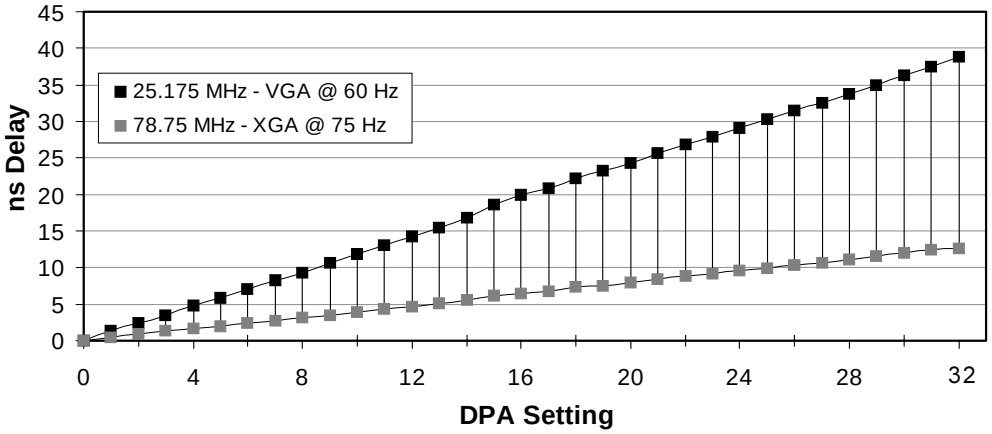
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
HSYNC Input Frequency	f_{HSYNC}	Reg 7:7 = 0	.008	10	MHz
OSC Input Frequency	f_{OSC}	Reg 7:7 = 1	.02	100	MHz


VCO Output Frequency and Intrinsic Jitter
Frequency (Slow: 3.0V @ 70ºC)
Frequency (Nominal: 3.3V @ 30ºC)
Frequency (Fast: 3.6V @ 0ºC)
Jitter (3.0V @ 70ºC)
Jitter (3.3V @ 30ºC)
Jitter (3.6V @ 0ºC)
Frequency
Jitter
VCO Frequency (MHz)
Jitter (ps)
VCO Voltage
700
600
500
400
300
200
100
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3
3.2

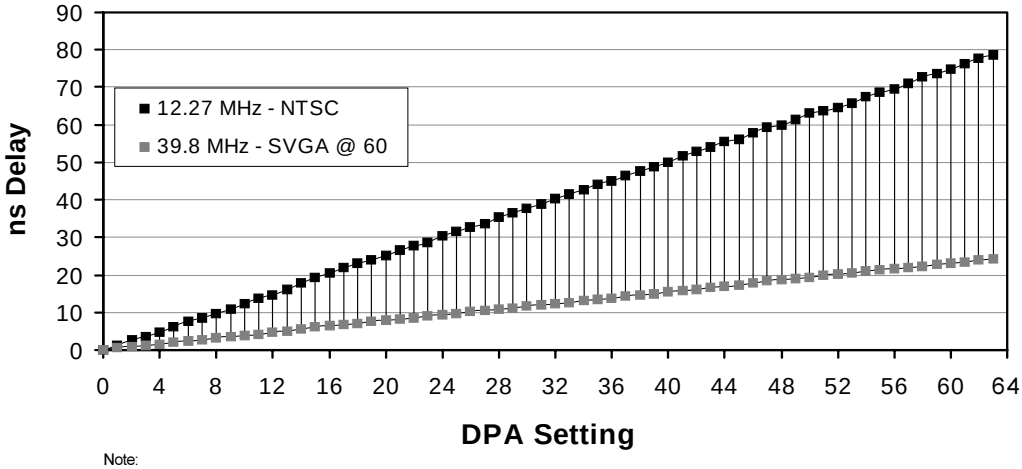
DPA Delay-16 Element Resolution



DPA Delay - 32 Element Resolution

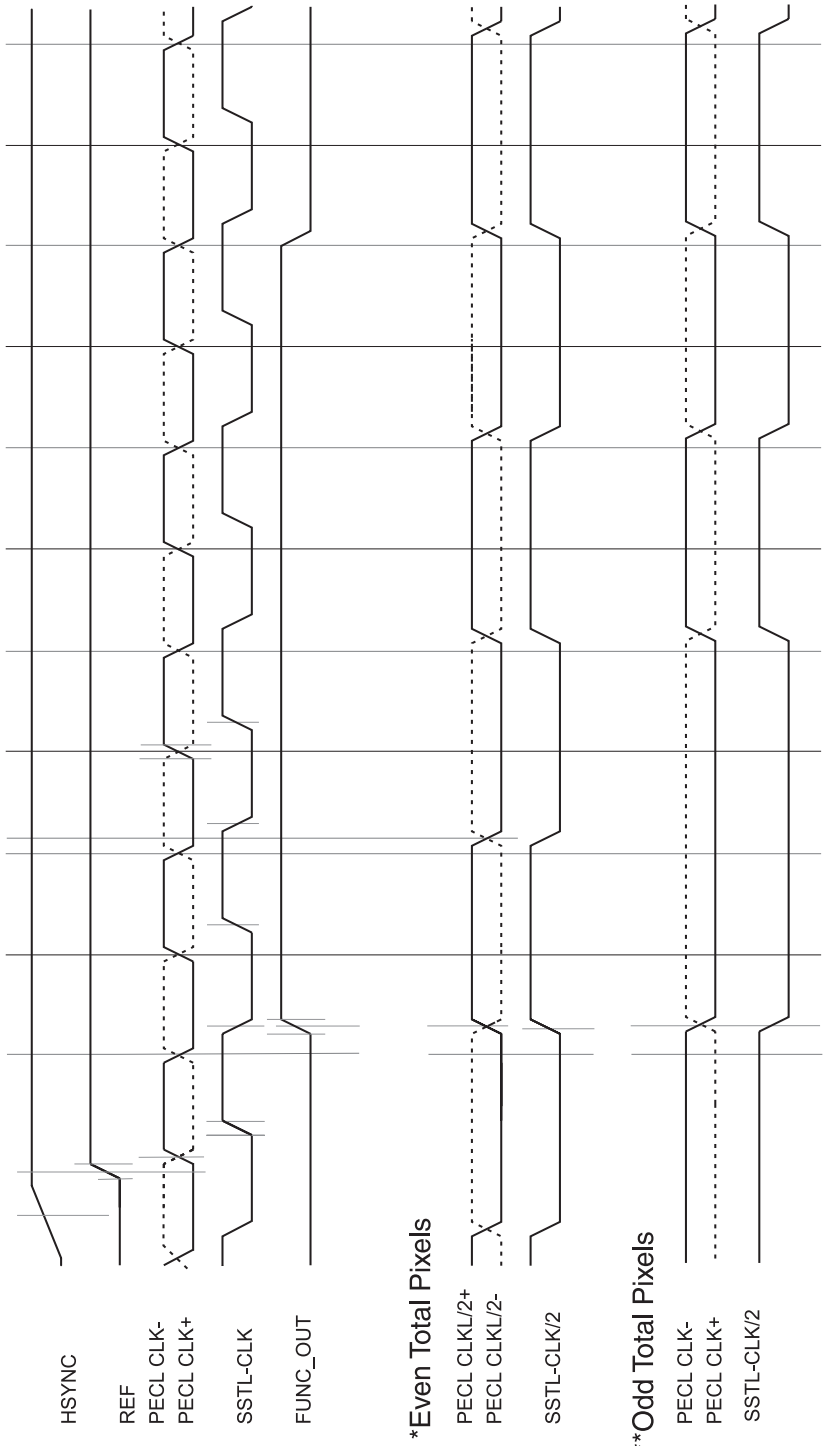


DPA Delay - 64 Element Resolution



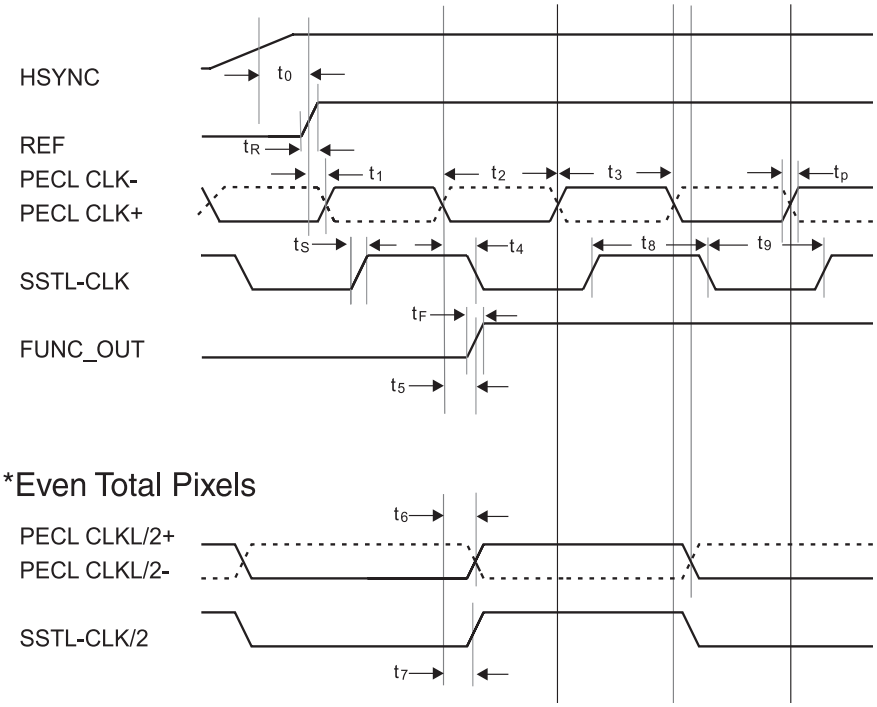
Note:
Maximum number of data points used for this graph.

AC Timing Characteristics Overview



* Timing when Register 2, Bit 0 = 0 (Total number of pixels is even.)
** Timing when Register 2, Bit 0 = 1 (Total number of pixels is odd.)

Output Timing Diagram



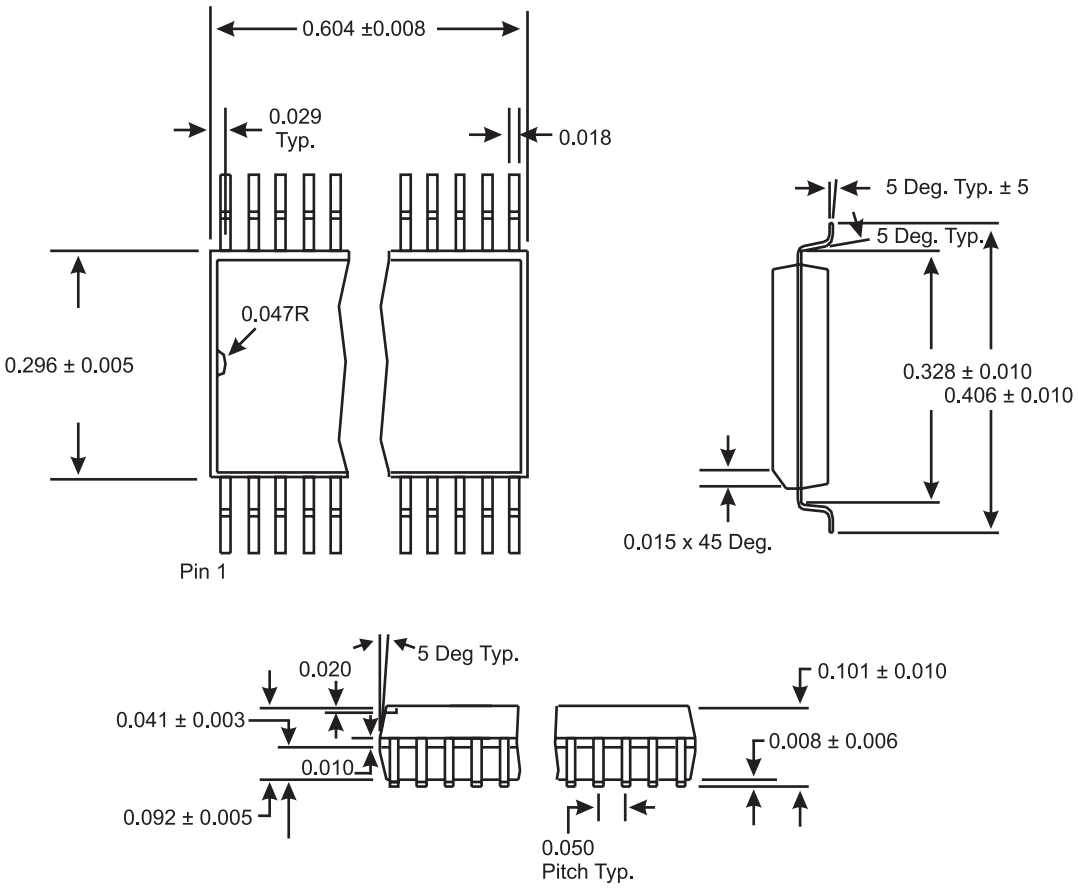
Typical Transition Times*

Symbol	Timing Description	Rise	Fall	Units
t_R	REF	2.8	1.8	ns
t_P	PECL CLK	1.0	1.2	ns
t_S	SSTL-CLK	1.6	0.7	ns
t_F	FUNC_OUT	1.2	1.0	ns

Output Timing*

Symbol	Timing Description	Min	Typ	Max	Units
t_0	HSYNC to REF delay	11.3	11.5	12	ns
t_1	REF to PECL clock delay	-1.0	0.8	2.2	ns
t_2, t_3	PECL clock duty cycle	45	50	55	%
t_4	PECL clock to SSTL_3 clock delay	0.2	0.75	1.2	ns
t_5	PECL clock to FUNC_OUT delay	1.5	1.9	2.3	ns
t_6	PECL clock to PECL/2 clock	1.0	1.3	1.5	ns
t_7	PECL clock to SSTL_3–CLK/2 delay	1.1	1.4	1.8	ns
t_8, t_9	SSTL clock duty cycle	45	50	55	%

*Note: Measured at 3.6V 0°C, 135-MHz output frequency, PECL clock lines to 75Ω termination, SSTL_3 clock lines unterminated, 20-pF load. Transition times vary based on termination.



24-Pin SOIC (wide body)

Ordering Information

ICS1523M