Integrated Circuit Systems, Inc.

User Programmable Differential Output Graphics Clock Generator

Description

The **ICS1562A** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1562A** provides a low cost solution for high-end video clock generation.

The **ICS1562A** has differential video clock outputs (CLK+ and CLK-) that are compatible with industry standard video DAC. Another clock output, LOAD, is provided whose frequency is derived from the main clock by a programmable divider. An additional clock output is available, LD/N2, which is derived from the LOAD frequency and whose modulus may also be programmed.

Operating frequencies are fully programmable with direct control provided for reference divider, prescaler, feedback divider and post-scaler.

Reset of the pipeline delay on Brooktree RAMDAC™s may be performed under register control. Outputs may also be set to desired states to facilitate circuit board testing.

Features

- Two programming options:
  ICS1562A-001 (Parallel Programming)
  ICS1562A-201 (Serial Programming)
- Supports high-resolution graphics - CLK output to 260 MHz, with 400 MHz options available
- Eliminates need for multiple ECL output crystal oscillators
- Fully programmable synthesizer capability - not just a clock multiplier
- Circuitry included for reset of Brooktree RAMDAC pipeline delay
- VRAM shift clock generation capability (-201 option only)
- Line-locked clock generation capability
- External feedback loop capability (-201 option only)
- Compact - 16-pin 0.150" skinny SOIC package
- Fully backward compatible to ICS1562

Simplified Block Diagram - ICS1562A

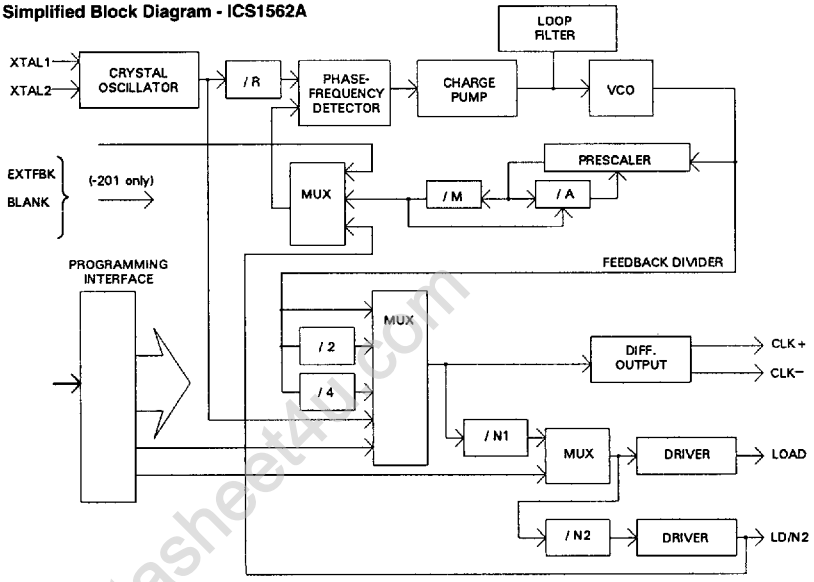
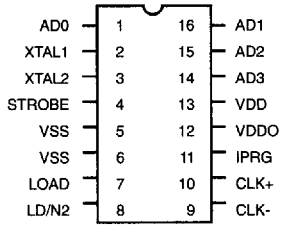


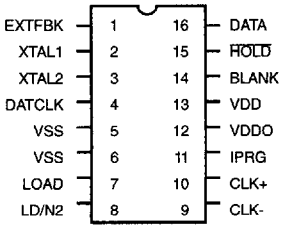
Figure 1

ICS1562A - 001 Pinout



16-Pin SOIC K-6

ICS1562A - 201 Pinout



16-Pin SOIC K-6

RAMDAC is a trademark of Brooktree Corporation.

Overview

The **ICS1562A** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1562A** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1562A** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1562A** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(VCO): = \frac{F(XTAL1) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1562A** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 448 in steps of one. Any even modulus from 448 through 896 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

Table 1 permits the derivator of "A" & "M" converter programming directly from desired modulus.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1562A**. This is useful in generating lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- Internal register bit (AUXCLK) value

Load Clock Divider

The **ICS1562A** has an additional programmable divider (referred to in Figure 1 as the N1 divider) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, 10, 12, 16 or 20 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described above. Additionally, this divider can be disabled under register control.

Digital Inputs - ICS1562A-001 Option

The AD0-AD3 pins and the STROBE pin are used to load all control registers of the **ICS1562A** (-001 option). The AD0-AD3 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. They may be driven with standard TTL or CMOS logic families.

The address of the register to be loaded is latched from the AD0-AD3 pins by a negative edge on the STROBE pin. The data for that register is latched from the AD0-AD3 pins by a positive edge on the STROBE pin. See Figure 2 for a timing diagram. After power-up, the **ICS1562A-001** requires 32 register writes for new programming to become effective. Since only 13 registers are used at present, the programming system can perform 19 "dummy" writes to address 13 or 14 to complete the sequence.

This allows the synthesizer to be completely programmed for the desired frequency before it is made active. Once the part has been "unlocked" by the 32 writes, programming becomes effective immediately.

ALL registers identified in the data sheet (0-9, 11, 12 & 15) MUST be written upon initial programming. The programming registers are not initialized upon power-up, but the latched outputs of those registers are. The latch is made transparent after 32 register writes. If any register has not been written, the state upon power-up (random) will become effective. Registers 13 & 14 physically do not exist. Register 10 does exist, but is reserved for future expansion. To insure compatibility with possible future modifications to the database, ICS recommends that all three unused locations be written with zero.

ICS1562A-001 Register Loading

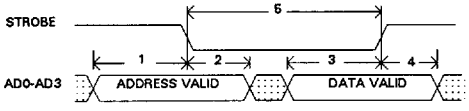


Figure 2

Digital Inputs - ICS1562A-201 Option

The programming of the **ICS1562A-201** is performed serially by using the DATCLK, DATA, and HOLD~pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the HOLD~pin is latched at the same time. When HOLD~ is low, the shift register may be loaded without disturbing the operation of the **ICS1562A**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the HOLD~ pin when the last data bit is presented. See Figure 3 for the programming sequence.

ICS1562A-201 Register Loading

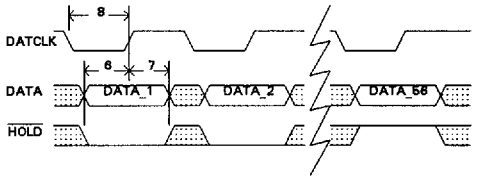


Figure 3

An additional control pin on the **ICS1562A-201**, BLANK can perform either of two functions. It may be used to disable the phase-frequency detector in line-locked applications. Alternatively, the BLANK pin may be used as a synchronous enable for VRAM shift clock generation. See sections on Line-Locked Operations and VRAM shift clock generation for details.

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Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+or CLK-, is four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. Additionally, minor adjustment to the duty factor can be achieved under register control.

The LOAD output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, 10, 12, 16 or 20. It may also be suppressed under register control. The load output may be programmed to output the VCO frequency divided by 2 (see AUX_N1 description in Register Mapping section), independent of the differential output and N1 divider modulus.

The LD/N2 output is high-current CMOS type drive whose frequency is derived from the LOAD output. The programmable modulus may range from 1 to 512 in steps of one.

Pipeline Delay Reset Function

The **ICS1562A** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs when the LOAD output is programmed for a modulus of either 3, 4, 5, 6, 8 or 10. This sequence can be generated by setting the appropriate register bit (DACRST) to a logic 1 and then resetting to logic 0.

When changing frequencies, it is advisable to allow 500 microseconds after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the video DAC to correctly execute its reset sequence. See Figure 4 for a diagram of the pipeline delay reset sequence.

Pipeline Delay Reset Timing

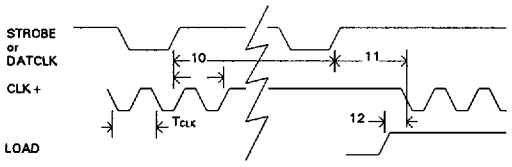


Figure 4

Reference Oscillator and Crystal Selection

The **ICS1562A** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1562A**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1562A** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1562A**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals if the REFPOL bit is set to logic 0.

Line-Locked Operation

The **ICS1562A** supports line-locked clock applications by allowing the LOAD (N1) and N2 divider chains to act as the feedback divider for the PLL.

The N1 and N2 divider chains allow a much larger modulus to be achieved than the PLL's own feedback divider. Additionally, the output of the N2 counter is accessible off-chip for performing horizontal reset of the graphics system, where necessary. This mode is set under register control (ALTLOOP bit). The reference divider (R counter) will ordinarily be set to divide by 1 in this mode, and the HSYNC signal of the external video will be supplied to the XTAL1 input. The output frequency of the synthesizer will then be:

$$F_{(CLK)} := F\ (XTAL1) \cdot N1 \cdot N2.$$

By using the phase-detector hardware disable mode, the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

ICS1562A-001 The **ICS1562A-001** supports phase detector disable via a special control mode. When the PDRSTEN (phase detector reset enable) bit is set and the last address latched is 15 (0Fh), a high level on AD3 will disable PLL locking.

ICS1562A-201 The **ICS1562A-201** supports phase detector disable via the BLANK pin. When the PDRSTEN bit is set, a high level on the BLANK input will disable PLL locking.

External Feedback Operation

The **ICS1562A-201** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the EXTFBEN bit is set to logic 1, the phase-frequency detector will use the EXTFBK pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input if the FBKPOL bit is set to logic 0.

VRAM Shift Clock Generation

The **ICS1562A-201** option supports VRAM shift clock generation and interruption. By programming the N2 counter to divide by 1, the LD/N2 output becomes a duplicate of the LOAD output. When the SCEN bit is set, the LD/N2 output may be synchronously started and stopped via the blank pin. When BLANK is high, the LD/N2 will be free-running and in phase with LOAD. When BLANK is taken low, the LD/N2 output is stopped at a low level. See Figure 5 for a diagram of the sequence. Note that this use of the **BLANK** pin precludes its use for phase comparator disable (see Line-Locked Operation).

VRAM Shift Clock Control

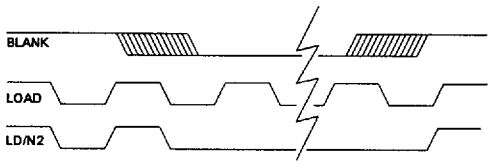


Figure 5

Power-On Initialization

The **ICS1562A** has an internal power-on reset circuit that performs the following functions:

1) Sets the multiplexer to pass the reference frequency to the CLK+ and CLK- outputs.

2) Selects the modulus of the N1 divider (for the LOAD clock) to be four.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

E

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations (i.e, pixel clock generation for hi-res displays), keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown on the following page:

VCO GAIN	MAX FREQUENCY
4	120 MHz
5	200 MHz
6	260 MHz
7	*

*SPECIAL APPLICATION. Contact factory for custom product above 260 MHz.

- Phase Detector Gain: For most graphics applications and divider ranges, set P[1, 0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During 1562 operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1562A** supports this through a register programmable mode, AUXEN. When this mode is set, two register bits directly control the logic levels of the CLK+/CLK- pins and the LOAD pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1562A** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1562A** has a VDDO pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1562A**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 6 for typical external circuitry.

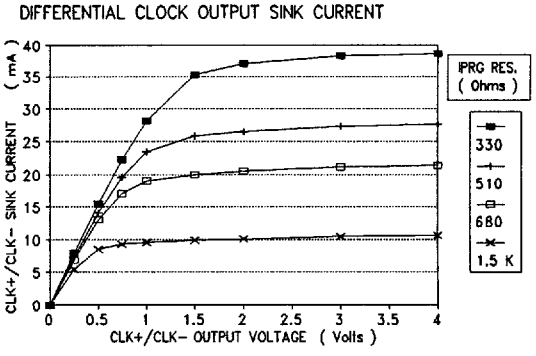
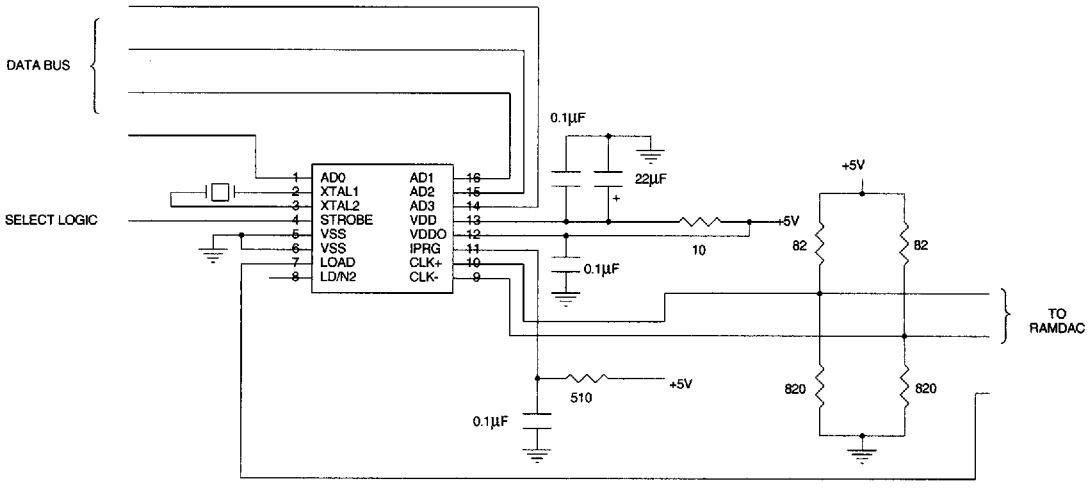


Figure 6

a)

ICS1562A-001 Typical Interface



b)

ICS1562A-201 Typical Interface

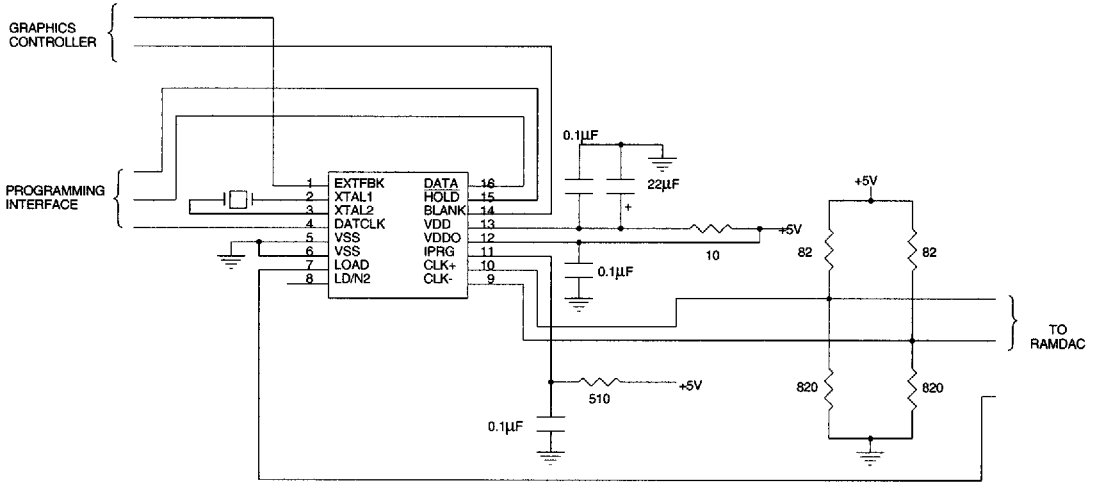


Figure 7

Register Mapping - ICS1562A-001 (Parallel Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562A. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-3	R[0]..R[3]	Reference divider modulus control bits
1	0-2	R[4]..R[6]	Modulus = value + 1
1	3	REFPOL	PLL locks to the rising edge of XTAL1 input when REFPOL=1 and to the falling edge of XTAL1 when REFPOL=0.
2	0-3	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
3	0-3	M[0]..M[3]	M counter control bits
4	0-1	M[4]..M[5]	Modulus = value + 1
4	2	FBKPOL	External feedback polarity control bit. The PLL will lock to the falling edge of EXTFBK when FBKPOL=1 and to the rising edge of EXTFBK when FBKPOL=0.
4	3	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
5	0-3	N1[0]..N1[3]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[3]	N1[2]	N1[1]	N1[0]	RATIO
0	0	0	0	3
0	0	0	1	4
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8
0	1	1	0	8
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16
1	X	1	0	16
1	X	1	1	20

X=Don't Care

REG#	BIT(S)	BIT REF.	DESCRIPTION
6	0-3	N2[0]..N2[3]	Sets the modulus of the N2 divider.
7	0-3	N2[4]..N2[7]	The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
8	3	N2[8]	
8	0-2	V[0]..V[1]	Sets the gain of the VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

9	0-1	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

9	3	[P2]	Phase detector tuning bit. Normally should be set to one.
10	1	LOADEN~	Load clock divider enable (active low). When set to logic 1, the LOAD and LD/N2 outputs will cease toggling.
10	2	SKEW-	Differential output duty factor adjust.
10	3	SKEW+	

SKEW+	SKEW-	
0	0	Default
0	1	Reduces T_{HIGH} by approximately 100 ps
1	0	Increases T_{HIGH} by approximately 100 ps
1	1	Do not use

REG#	BIT(S)	BIT REF.	DESCRIPTION
11	0-1	S[0]..S[1]	PLL post-scaler/test mode select bits

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

11	2	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
11	3	AUX_N1	When in the AUXEN clock mode, this bit controls the LOAD output (and consequently the N2 output according to its programming). When not in the AUXEN clock mode, this bit, if set to one, will override the N1 divider modulus and output the VCO frequency divided by two [F(PLL)/2] at the LOAD output.
12	0	RESERVED	Must be set to zero.
12	1	JAMPLL	Tristates phase detector outputs; resets phase detector logic, and resets R, A, M, and N2 counters.
12	2	DACRST	Set to zero for normal operation. When set to one, the CLK+output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/- 1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.
12	3	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
15	0	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
15	3	PDRSTEN	Phase-detector reset enable control bit. When this bit is set, the AD3 pin becomes a transparent reset input to the phase detector. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

Register Mapping - ICS1562A-201 (Serial Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562A. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

BIT(S)	BIT REF.	DESCRIPTION
1-4	N1[0]..N1[3]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[3]	N1[2]	N1[1]	N1[0]	RATIO
0	0	0	0	3
0	0	0	1	4
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8
0	1	1	0	8
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16
1	X	1	0	16
1	X	1	1	20

5	RESERVED	Must be set to zero.
6	JAMPLL	Tristates phase detector outputs, resets phase detector logic, and resets R, A, M, and N2 counters.
7	DACRST	Set to zero for normal operations. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/−1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.
8	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
9	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
10	SCEN	VRAM shift clock enable bit. When logic 1, the BLANK pin can be used to disable the LD/N2 output.
11	EXTFBKEN	External PLL feedback select. When logic 1, the EXTFBK pin is used for the phase-frequency detector feedback input.
12	PDRSTEN	Phase detector reset enable control bit. When this bit is set, a high level on the BLANK input will disable PLL locking. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

BIT(S)	BIT REF.	DESCRIPTION
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divder drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

15	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
16	AUX_N1	When in the AUXEN clock mode, this bit controls the N1 output (and consequently the N2 output according to its programming). When not in the AUXEN clock mode, this bit, if set to one, will override the N1 divider modulus and output the VCO frequency divided by two [F(PLL)/2] at the LOAD output.
17-24 28	N2[0]..N2[7] N2[8]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
25-27	V[0]..V[2]	Sets the gain of VCO according to this table.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

29-30	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

31	RESERVED	Set to zero.
32	P[2]	Phase detector tuning bit. Should normally be set to one.

BIT(S)	BIT REF.	DESCRIPTION
33-38	M[0]..M[5]	M counter control bits Modulus = value +1
39	FBKPOL	External feedback polarity control bit. The PLL will lock to the falling edge of EXTFBK when FBKPOL=1 and to the rising edge of EXTFBK when FBKPOL=0.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
45	RESERVED	Set to zero.
46	LOADEN~	Load clock divider enable (active low). When set to logic 1, the LOAD and LD/N2 outputs will cease toggling.
47 48	SKEW- SKEW+	Differential output duty factor adjust.

SKEW+	SKEW-	
0	0	Default
0	1	Reduces T_{HIGH} by approximately 100 ps
1	0	Increases T_{HIGH} by approximately 100 ps
1	1	Do not use

49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	REFPOL	PLL locks to the rising edge of XTAL1 input when REFPOL=1 and to the falling edge of XTAL1 when REFPOL=0.

E

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A=0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \leq M$

Pin Descriptions - ICS1562A-001

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
1	AD0	Address/Data Bit 0 (LSB)
16	AD1	Address/Data Bit 1
15	AD2	Address/Data Bit 2
14	AD3	Address/Data Bit 3 (MSB)
8	LD/N2	Divided LOAD output. See text.
4	STROBE	Control for address/data latch
13	VDD	PLL system power (+5V. See application diagram.)
12	VDDO	Output stage power (+5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected to the same ground potential.

Pin Descriptions - ICS1562A-201

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
4	DATCLK	Data Clock (Input)
16	DATA	Serial Register Data (Input)
15	HOLD~	$\overline{\text{HOLD}}$ (Input)
14	BLANK	Blanking (Input). See Text.
8	LD/N2	Divided LOAD output/shift clock. See text.
1	EXTFBK	External feedback connection for PLL (input). See text.
13	VDD	PLL system power (+5V. See application diagram.)
12	VDDO	Output stage power (+5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected.

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS}) ..... 7.0 V
Digital Inputs ..... V_{SS}-0.5 to V_{DD} + 0.5 V
Digital Outputs ..... V_{SS}-0.5 to V_{DDO} + +0.5 V
Ambient Operating Temperature ..... -55 to 125°C
Storage Temperature ..... -65 to 150°C
Junction Temperature ..... 175°C
Soldering Temperature ..... 260°C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS}) ..... 4.75 to 5.25 V

Operating Temperature (Ambient) ..... 0 to 70°C

DC Characteristics

TTL-Compatible Inputs
001 Option - (AD0-AD3, STROBE),
201 Option - (DATCLK, DATA, HOLD, BLANK, EXTFBK)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih}=VDD	-	10	uA
Input Low Current	I_{il}	V_{il}=0.0	-	200	uA
Input Capacitance	C_{in}		-	8	pf
Hysteresis (STROBE/DATCLK)	V_{hys}	V_{DD}=5V	.20	.60	V

XTAL1 Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

LOAD, LD/N2 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh = 4.0mA)			2.4	-	V
Output Low Voltage (Iol = 8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency (see Note 1)	40		260	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pf
F_{load}	LOAD Frequency			80	MHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current		15	t.b.d.	mA
I_{ddo}	VDDO Supply Current (excluding CLK+/– termination)		20	t.b.d.	mA
T_{high}	Differential Clock Output Duty Cycle (see Note 2)	45		55	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 3)		<0.06		pixel
	DIGITAL INPUTS - ICS1562A-001				
1	Address Setup Time	10			ns
2	Address Hold Time	10			ns
3	Data Setup Time	10			ns
4	Data Hold Time	10			ns
5	STROBE Pulse Width (T_{hi} or T_{lo})	20			ns
	DIGITAL INPUTS - ICS1562A-201				
6	DATA/HOLD~ Setup Time	10			ns
7	DATA/HOLD~ Hold Time	10			ns
8	DATCLK Pulse Width (T_{hi} or T_{lo})	20			ns
	PIPELINE DELAY RESET				
9	Reset Activation Time			2*Tclk	ns
10	Reset Duration	4*Tload			ns
11	Restart Delay			2*Tload	ns
12	Restart Matching	-1*Tclk		+1.5*Tclk	ns
	DIGITAL OUTPUTS				
13	CLK+/CLK– Clock Rate			260	MHz
14	LOAD To LD/N2 Skew (Shift Clock Mode)	-2	0	+2	ns

Note 1: Use of the post-divider is required for frequencies lower than 40 MHz on CLK+ & CLK- outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.

Note 2: Using load circuit of Figure 6. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

Note 3: Cumulative jitter is defined as the maximum error (in the domain) if any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Ordering Information

ICS1562AM-001 or ICS1562AM-201

Example: