Description

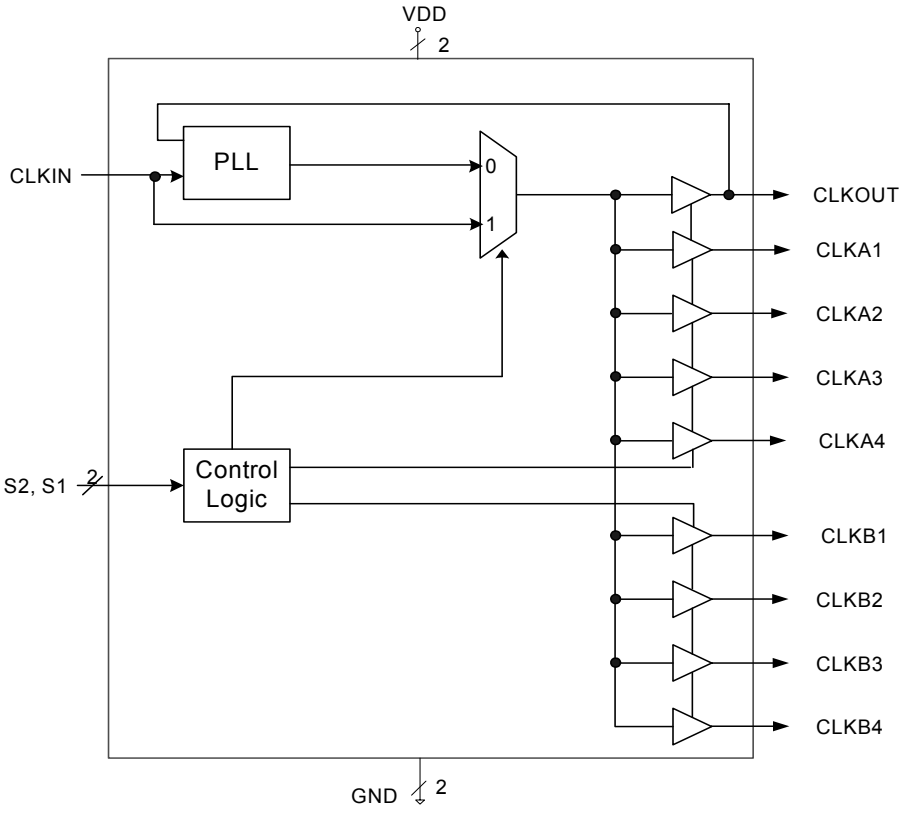
The ICS2309 is a low phase noise, high-speed PLL based, low-skew zero delay buffer. Based on ICS' proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides eight low skew outputs at speeds up to 133 MHz at 3.3 V. The outputs can be generated from the PLL (for zero delay), or directly from the input (for testing), and can be set to tri-state mode or to stop at a low level. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The ICS2309 is available in two different versions. The ICS2309-1 is the base part. The ICS2309-1H is a high drive version with faster rise and fall times.

Features

- Clock outputs from 10 to 133 MHz
- Zero input-output delay
- Eight low skew (<250 ps) outputs
- Device-to-device skew <700 ps
- Full CMOS outputs with 25 mA output drive capability at TTL levels
- 5 V tolerant CLKIN
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V
- Industrial temperature range available
- Packaged in 16-pin SOIC and TSSOP (-1H version only)
- Pb (lead) free package available for -1H version (16-pin TSSOP only)

Block Diagram



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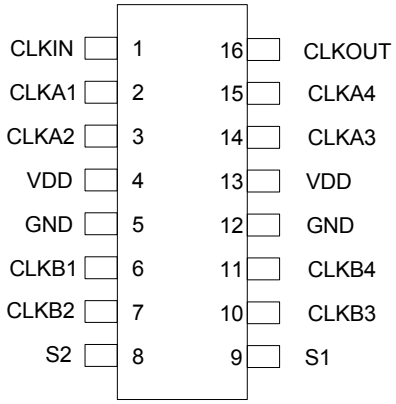
Pin Assignment



16 pin narrow (150 mil) SOIC

Output Clock Mode Select Table

S2	S1	CLKA1:A4	CLKB1:B4	A & B Source	PLL Status
0	0	Tri-state (note 1)	Tri-state (note 1)	PLL	OFF
0	1	Running	Tri-state (note 1)	PLL	ON
1	0	Running	Running	CLKIN (note 2)	OFF
1	1	Running	Running	PLL	ON

Note 1. Outputs are in high impedance state
Note 2. Buffer mode only; not zero delay between input and output

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Clock input (5 V tolerant).
2 - 3	CLKA1:A4	Output	Clock outputs A1:A4. See table above.
4	VDD	Power	Power supply. Connect to 3.3 V.
5	GND	Power	Connect to ground.
6 - 7	CLKB1:B4	Output	Clock outputs B1:B4. See table above.
8	S2	Input	Select input 2. See table above. Internal pull-up.
9	S1	Input	Select input 1. See table above. Internal pull-up.
10 - 11	CLKB1:B4	Output	Clock outputs B1:B4. See table above.
12	GND	Power	Connect to ground.
13	VDD	Power	Power supply. Connect to 3.3 V.
14 - 15	CLKA1:A4	Output	Clock outputs A1:A4. See table above.
16	CLKOUT	Input	Buffered output. Internall feedback on this pin.

External Components

The ICS2309 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 mF should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33Ω may be used to each clock output pin to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS2309. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
CLKIN and FBIN inputs	-0.5 V to 5.5 V
Electrostatic Discharge (HBM)	2000 V
Ambient Operating Temperature (Commercial)	0 to +70°C
Ambient Operating Temperature (Industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Industrial)	-40		+85	°C
Ambient Operating Temperature (Commercial)	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

ICS2309M-1, **VDD = 3.3 V ±10%,** Ambient Temperature -40 to +85°C(Industrial), (0-70°C Commercial)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Low Current	I_{IL}	VIN = 0V			50	µA
Input High Current	I_{IH}	VIN = VDD			100	µA
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	No Load			32	mA
Power Down Supply Current		CLKIN = 0, Note 1			12	µA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance	C_{IN}	S2, S1, CLKIN		5		pF

Note 1: When there is no clock signal present at CLKIN, the ICS2309 will enter power down mode. The PLL is stopped and the outputs are tri-state.

AC Electrical Characteristics

ICS2309M-1, **VDD=3.3 V ±10%,** Ambient temperature -40 to +85°C(Industrial), (0-70°C Commercial),

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Frequency	f_{IN}	10 pF load, See table on page 2	10		133	MHz
Output Clock Frequency		30 pF load, See table on page 2	10		100	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, outputs loaded			2.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, outputs loaded			2.5	ns
Output Clock Duty Cycle	t_{DC}	measured at 1.4V, Fout=66.67 MHz	40	50	60	%
Output Clock Duty Cycle	t_{DC}	measured at 1.4V, Fout=50 MHz	45	50	55	%
Device to Device Skew		rising edges at VDD/2			700	ps
Output to Output Skew		rising edges at VDD/2			250	ps
Input to Output Skew		rising edges at VDD/2			±350	ns
Input to Output Skew		rising edges at VDD/2, S2= 1, S1 = 0	1	5	8.7	ns
Cycle to Cycle Jitter		measured at 66.67M, outputs loaded			200	ps
PLL Lock Time		Note 2			1.0	ms

Note 2: With VDD at a steady rate and valid input at CLKIN

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ICS2309M-1H, **VDD=3.3 V ±10%,** Ambient temperature -40 to +85°C(Industrial), (0-70°C Commercial),

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Frequency	f_{IN}	10 pF load, See table on page 2	10		133	MHz
Output Clock Frequency		30 pF load, See table on page 2	10		100	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, outputs loaded			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, outputs loaded			1.5	ns
Output Clock Duty Cycle	t_{DC}	measured at 1.4V, Fout=66.67 MHz	40	50	60	%
Output Clock Duty Cycle	t_{DC}	measured at 1.4V, Fout=50 MHz	45	50	55	%
Device to Device Skew		rising edges at VDD/2			700	ps
Output to Output Skew		rising edges at VDD/2			250	ps
Input to Output Skew		rising edges at VDD/2			±350	ps
Input to Output Skew		rising edges at VDD/2, S2= 1, S1 = 0	1	5	8.7	ns
Cycle to Cycle Jitter		measured at 66.67M, outputs loaded			200	ps
PLL Lock Time		Note 3			1.0	ms

Note 3: With VDD at a steady rate and valid input at CLKIN

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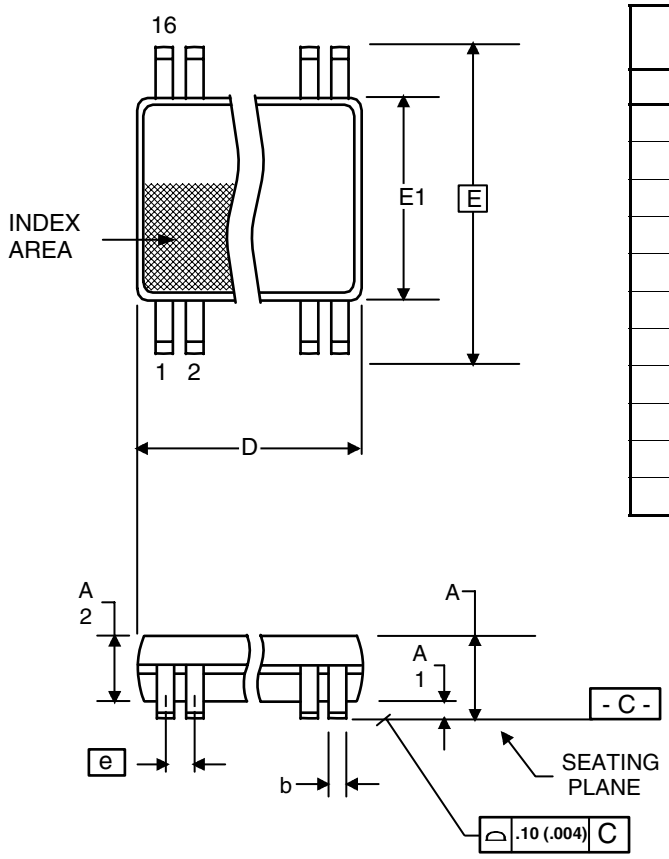
Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°

Thermal Characteristics for 16TSSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

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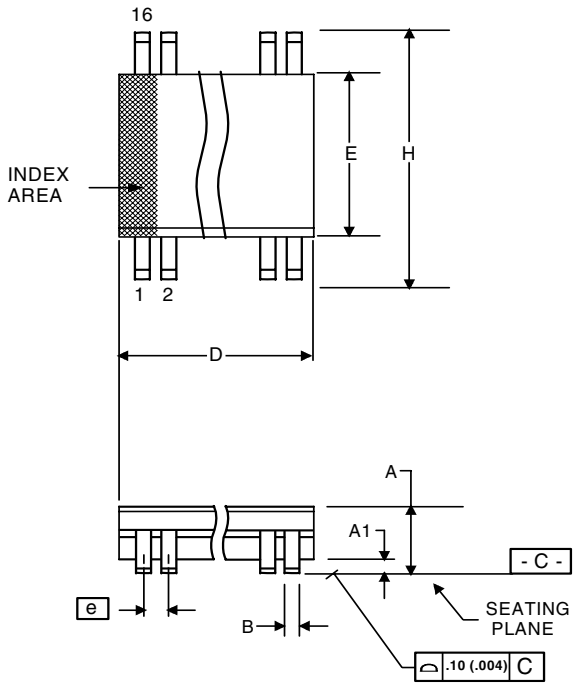
Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Thermal Characteristics for 16SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS2309MI-1	ICS2309MI-1	Tubes	16-pin SOIC	-40 to +85° C
ICS2309MI-1T	ICS2309MI-1	Tape and Reel	16-pin SOIC	-40 to +85° C
ICS2309M-1	ICS2309M-1	Tubes	16-pin SOIC	0 to +70° C
ICS2309M-1T	ICS2309M-1	Tape and Reel	16-pin SOIC	0 to +70° C
ICS2309MI-1H	ICS2309MI-1H	Tubes	16-pin SOIC	-40 to +85° C
ICS2309MI-1HT	ICS2309MI-1H	Tape and Reel	16-pin SOIC	-40 to +85° C
ICS2309M-1H	ICS2309M-1H	Tubes	16-pin SOIC	0 to +70° C
ICS2309M-1HT	ICS2309M-1H	Tape and Reel	16-pin SOIC	0 to +70° C
ICS2309GI-1H	2309GI1H	Tubes	16-pin TSSOP	-40 to +85° C
ICS2309GI-1HT	2309GI1H	Tape and Reel	16-pin TSSOP	-40 to +85° C
ICS2309GI-1HLF	309GI1HL	Tubes	16-pin TSSOP	-40 to +85° C
ICS2309GI-1HLFT	309GI1HL	Tape and Reel	16-pin TSSOP	-40 to +85° C
ICS2309G-1H	2309G-1H	Tubes	16-pin TSSOP	0 to +70° C
ICS2309G-1HT	2309G-1H	Tape and Reel	16-pin TSSOP	0 to +70° C
ICS2309G-1HLF	2309G1HL	Tubes	16-pin TSSOP	0 to +70° C
ICS2309G-1HLFT	2309G1HL	Tape and Reel	16-pin TSSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
A	P. Griffith	12/01/04	New device/datasheet; Prelminary.
B	P. Griffith	12/27/04	Add TSSOP package. Made corrections to IDD, IDDP, input capacitance and duty cycle specs/test conditions. Removed jitter specs for CL=15 pF. Added I/O skew spec for bypass mode and duty cycle spec for Fout=50 MHz.
C	P. Griffith	1/25/05	Made corrections to test conditions for output rise time, fall time, duty cycle and cycle-to-cycle jitter. Moved from Preliminary to Final.
D	P. Griffith	5/24/05	Added LF ordering info to 16-pin TSSOP (-1H version only); added Thermal Chars for 16-pin TSSOP package

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