

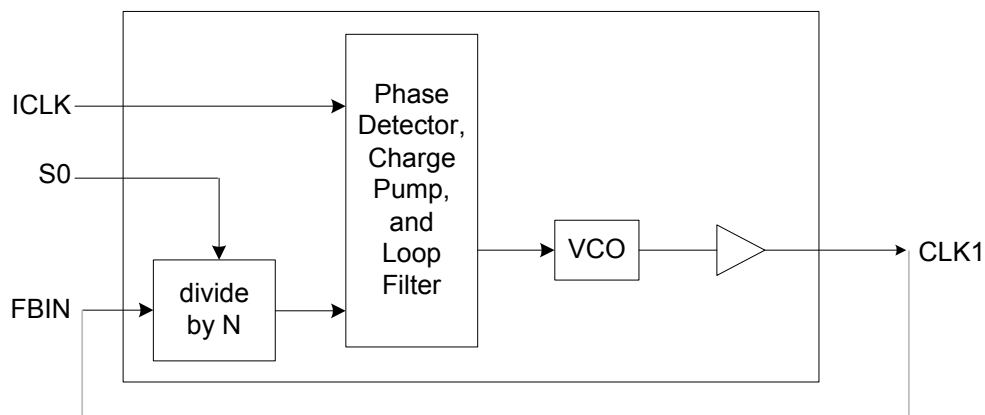
MULTIPLIER AND ZERO DELAY BUFFER
ICS2402
Description

The ICS2402 is a high-performance Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase-Locked Loop (PLL) techniques. The chip is part of IDT's ClockBlocks™ family and was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both output clocks, giving the appearance of no delay through the device.

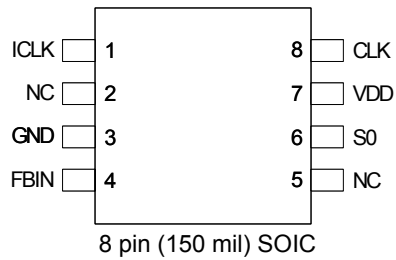
The ICS2402 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to graphics/video. By allowing off-chip feedback paths, the device can eliminate the delay through other devices.

Features

- 8-pin SOIC package – Pb-free, RoHS compliant
- Absolute jitter ± 100 ps
- Propagation Delay of ± 600 ps
- Output multiplier of 2X
- Output clock frequency up to 80 MHz
- Can recover degraded input clock duty cycle
- Output clock duty cycle of 45/55
- Full CMOS clock swings with 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3 V or 5 V

Block Diagram


Pin Assignment



Clock Multiplier Decoding Table 1

(Multiplies Input clock by shown amount)

| S0 | CLK |
|----|----------|
| 0 | 2 X ICLK |
| 1 | ICLK |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | ICLK | Input | Reference clock input. |
| 2 | NC | — | No connect. Do not connect to anything. |
| 3 | GND | Power | Connect to ground. |
| 4 | FBIN | Input | Feedback clock input. |
| 5 | NC | — | No connect. Do not connect to anything. |
| 6 | S0 | Input | Select pin for Clock Multiplier Decoding Table above. |
| 7 | VDD | Power | Connect to +3.3 V or +5.0 V. |
| 8 | CLK | Output | Clock output per table above. |

External Components

The ICS2402 requires a 0.01 μ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the part to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω series terminating resistor can be used next to each output pin.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS2402. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Temperature under Bias | -55 to 125° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Power Dissipation | 0.5 W |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +4.5 | +5.0 | +5.5 | V |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V |

DC Electrical Characteristics

VDD = 3.3 V \pm 5%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------------|--------------------------|------|----------|------|-------|
| Operating Voltage | VDD | | 3.15 | | 3.45 | V |
| Operating Current | IDD | | | 20 | | mA |
| Input High Voltage | V _{IH} | ICLK, FBIN, S0 | 2 | | | V |
| Input Low Voltage | V _{IL} | ICLK, FBIN, S0 | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |
| Short Circuit Current | I _{OS} | CLK | | \pm 50 | | mA |
| Input Capacitance | C _{IN} | S0 | | 5 | | pF |

VDD = 5 V \pm 10%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------------|--------------------------|---------|----------|---------|-------|
| Operating Voltage | VDD | 5 V | 4.5 | | 5.5 | V |
| Operating Current | IDD | | | 30 | | mA |
| Input High Voltage | V _{IH} | ICLK, FBIN, S0 | 0.7xVDD | | | V |
| Input Low Voltage | V _{IL} | ICLK, FBIN, S0 | | | 0.2xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 4.5 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.5 | V |
| Short Circuit Current | I _{SC} | Each output | | \pm 80 | | mA |
| Input Capacitance | C _{IN} | S0 | | 5 | | pF |

AC Electrical Characteristics

VDD = 3.3 V \pm 5%, or 5 V \pm 10%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|--------|--------------------|------|-----------|------|-------|
| Input Frequency, ICLK | | S0=1 | 10 | | 80 | MHz |
| | | S0=0 | 10 | | 40 | MHz |
| Output Frequency, CLK | | | 10 | | 80 | MHz |
| Input to Output Jitter | | CLK>20 MHz, Note 2 | | 200 | | ps |
| Absolute Short-term Jitter, peak-to-peak | | Note 2 | | \pm 100 | | ps |
| Input to Output Skew | | Note 1 | -600 | | 600 | ps |
| Output Clock Rise Time | | 20% to 80%, Note 2 | | 1.5 | | ns |
| Output Clock Fall Time | | 80% to 20%, Note 2 | | 1.5 | | ns |
| Output Clock Duty Cycle | | At VDD/2, Note 2 | 45 | 50 | 55 | % |

Note 1: Assumes clocks with same rise time, measured from rising edges at VDD/2

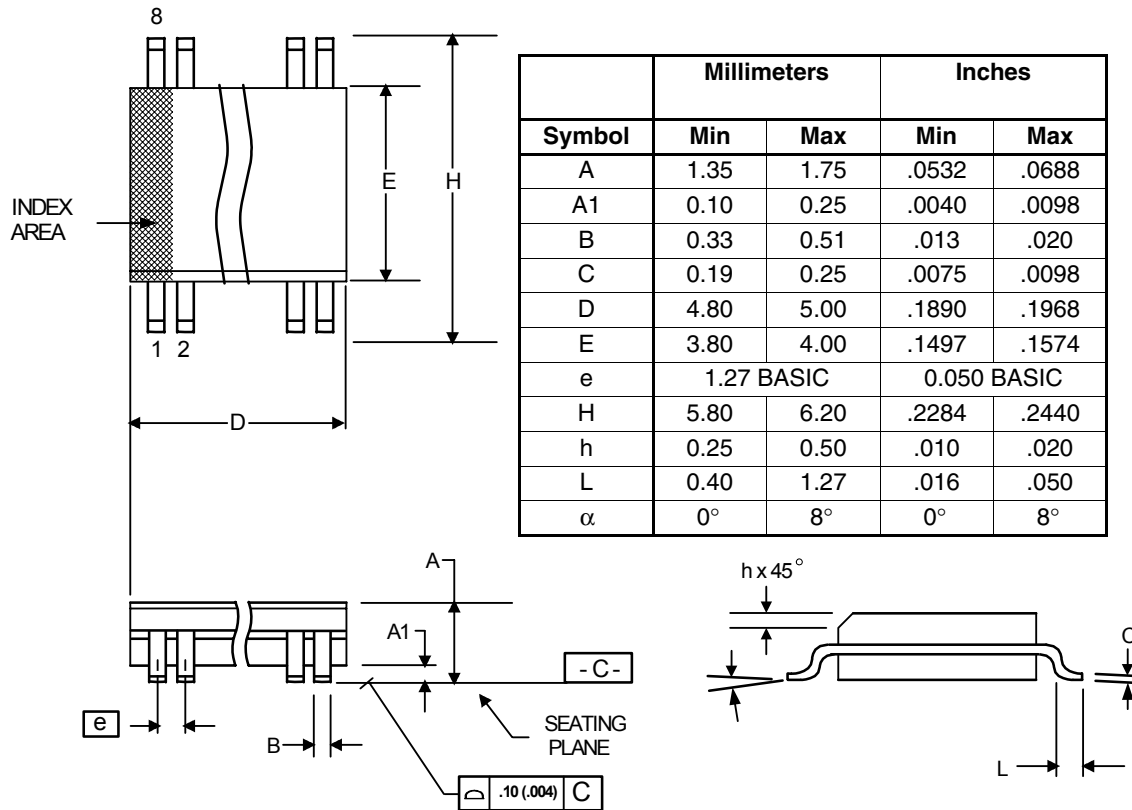
Note 2: Measured with a 15 pF load.

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 140 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | °C/W |

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------|--------------------|------------|-------------|
| 2402MLF | 2402MLF | Tubes | 8-pin SOIC | 0 to +70° C |
| 2402MLFT | 2402MLF | Tape and Reel | 8-pin SOIC | 0 to +70° C |

“LF” denotes Pb (lead) free package, RoHS compliant.

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Revision History

| Rev. | Originator | Date | Description of Change |
|------|------------|----------|---|
| B | P.Griffith | 10/05/04 | New device/datasheet for HP. |
| C | S. Gardner | 11/04/04 | Changed values for Abs. Jitter, Prop. Delay, and Output Clock Freq. in "Features" section; removed secondary Input High/Low and Output High (CMOS) voltage specs in DC chars; multiple updates to AC chars and added 5 V +/-10% rating; move from Preliminary to Release. |
| D | P.Griffith | 12/21/04 | Added LF packaging and ordering information. Released from custom to standard device. |
| E | — | 08/18/09 | Added EOL note per PDN U-09-01. |
| F | — | 05/13/10 | Removed EOL note and non-green orderables. |

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