Integrated Circuit Systems, Inc.

ICS2595

Not recommended for new designs

User-Programmable Dual High-Performance Clock Generator

Description

The **ICS2595** is a dual-PLL (phase-locked loop) clock generator specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines **FS0-FS3**. Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the **MS0 & MS1** lines.

A unique feature of the **ICS2595** is the ability to redefine frequency selections in both the VCLK and MCLK synthesizers after power-up. This permits complete set-up of the frequency table upon system initialization.

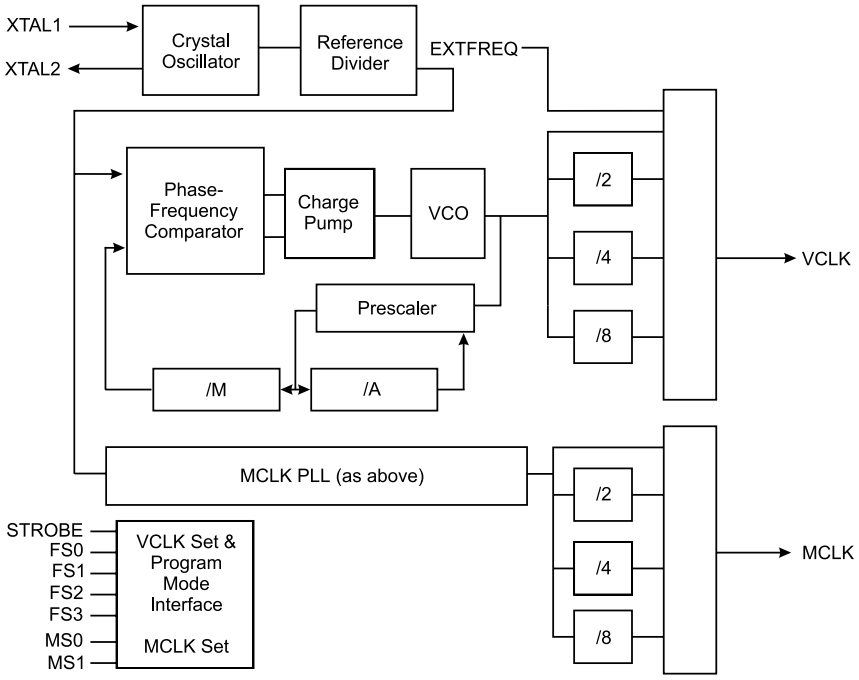
Features

- Advanced ICS monolithic phase-locked loop technology for extremely low jitter
- Supports high-resolution graphics - **VCLK** output to 145 MHz
- Completely integrated - requires only external crystal (or reference frequency and decoupling)
- Power-down modes support portable computing
- Sixteen selectable **VCLK** frequencies (all user re-programmable)
- Four selectable **MCLK** frequencies (all user re-programmable)

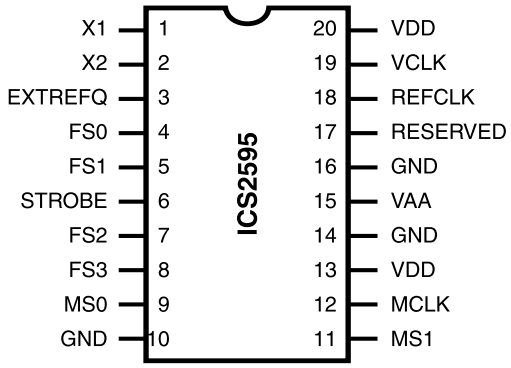
Applications

- PC Graphics
- VGA/Supper VGA/XGA Applications

Block Diagram



Pin Configuration



20-Pin DIP or SOIC

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	IN	Quartz crystal connection 1/Reference Frequency Input
2	X2	OUT	Quartz crystal connection2
3	EXTFREQ	IN	External Frequency Input
4	FS0	IN	VCLK PLL Frequency Select LSB
5	FS1	IN	VCLK PLL Frequency Select Bit
6	STROBE	IN	Control for Latch of VCLK Select its (FS0-FS3)
7	FS2	IN	VCLK PLL Frequency Select Bit
8	FS3	IN	VCLK PLL Frequency Select MSB
9	MS0	IN	MCLK PLL Frequency Select LSB
10,14,16	GND	PWR	Device Ground. All pins must be connected
11	MS1	IN	MCLK PLL Frequency Select MSB
12	MCLK	OUT	MCLK Frequency Output
13,20	VDD	PWR	Output Stage VDD. All pins must be connected
15	VAA	PWR	Synthesizer VDD
17	RESERVED	N/C	Must be connected to GND
18	REFCLK	OUT	Buffered Referenced Clock Output
19	VCLK	OUT	VCLK Frequency Output

Digital Inputs

The **FS0-FS3** pins and the **STROBE** pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed/user-programmed selections in the **ICS2595**. These pins are also used to load new frequency data into the registers.

The standard interface for the **ICS2595** matches the interface of the industry standard ICS2494. That is, the FS0-FS3 inputs access the device internals transparently when the STROBE pin is high.

The digital interface for the **ICS2595** (i.e. the **FS0-FS3** inputs) may be optionally configured for edge-triggered or level-activated operation of the **STROBE** pin. Example timing requirements for each of the four options are shown in Figure 1.

The programming sequence has been designed in such a way that **STROBE** pin need not be used (as in situations where the device is connected to the frequency select port of some VGA chips).

VCLK Output Frequency Selection

To change the **VCLK** output frequency, simply write the appropriate data to the **ICS2595 FS** inputs. The synthesizer will output the new frequency programmed into that location after a brief delay (see time-out specifications).

Upon device power-up, the selected frequency will be the frequency pre-programmed into address 0 until a device write is performed.

MCLK Output Frequency Selection

The MS0-MS1 pins are used to directly select the desired operating frequency of the MCLK output from the four pre-programmed/user-programmed selections in the **ICS2595**. These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

In order to ensure that reliable programming under all circumstances, we require that two "nibble" writes be added to the beginning of the programming sequence that was previously specified. The new sequence is shown in Table 1. Note that the FS3 data is "0" for these first two writes.

Because the same pins are used for both VCLK frequency selection and re-programming the device frequency table, a specific procedure must be observed for selection between these modes. Device programming is accomplished by executing a "programming sequence". The latched FS2 input functions as a data input, and the latched FS3 input functions as a data clock when this mode is activated. As the latched FS3 data transitions from 0 to 1, the latched FS2 data is shifted into the register. Note that it is the

Table 1: Programming Sequence

Nibble	FS0	FS1	FS2	FS3
1	X	X	0	0
2	X	X	1	0
3	X	X	START bit (must be "0")	0
4	X	X	"	1
5	X	X	R/W* control bit (must be "0")	0
6	X	X	"	1
7	X	X	LO (location LSB)	0
8	X	X	"	1
9	X	X	L1	0
10	X	X	"	1
11	X	X	L2	0
12	X	X	"	1
13	X	X	L3	0
14	X	X	"	1
15	X	X	L4 (location MSB)	0
16	X	X	"	1
17	X	X	N0 (feedback LSB	0
18	X	X	"	1
19	X	X	N1	0
20	X	X	"	1
21	X	X	N2	0
22	X	X	"	1
23	X	X	N3	0
24	X	X	"	1
25	X	X	N4	0
26	X	X	"	1
27	X	X	N5	0
28	X	X	"	1
29	X	X	N6	0
30	X	X	"	1
31	X	X	N7(feedback MSB)	0
32	X	X	"	1
33	X	X	EXTFREQ (select if "1")	0
34	X	X	"	1
35	X	X	D0 (post-divder MSB)	0
36	X	X	"	1
37	X	X	D1 (post-divder MSB)	0
38	X	X	"	1
39	X	X	STOP1 bit (must be "1")	0
40	X	X	"	1
41	X	X	STOP2 bit (must be '1")	0
42	X	X	"	1

LATCHED FS inputs, not the FS inputs themselves, that are interpreted by the internal logic. Interface logic resides between the FS input pins and the programming/frequency select logic. The appropriate "data write" procedure must be observed. See the section "Digital Interface" in this supplement for more information.

These rules must be followed:

- Calculate *Tmax* and *Tmin* in seconds (where R is the modulus of the reference divider and Fref is the reference frequency in Hz) by the following formulas:

$$T\text{min} = \frac{6^* R}{F\text{ref}}$$

$$T\text{max} = \frac{4096^* R}{F\text{ref}}$$

- A programming sequence consists of 42 successive data writes to the device as shown in table 1: no delay greater than *Tmax* or less than *Tmin* may occur between any two successive writes.

- A readback sequence consists of 64 successive data writes to the device as shown in table 2: no delay greater than *Tmax* or less than *Tmin* may occur between any two successive writes.

- Programming or readback sequences must be preceded by a "quiet" period of at least 2* *Tmax* with no data writes to the device unless it was immediately preceded by another legal programming (or readback) sequence (nothing else in between)

- To change the active VCLK frequency selection, simply write that data to the device; the last data written to the part will always become VCLK frequency select after a delay of approximately 2* *Tmax*. The internal shift register is cleared at this time also.

The FS0 & FS1 inputs are not used for programming, so it is possible to use a two-pin interface for programming and frequency selection (any bank of four VCLK addresses).

The reference frequency source must be operational for proper execution of the programming sequence. If the on-chip crystal oscillator is, allow at least 4* *Tmax* after the device has valid power before attempting to program it.

Data Description

Location Bits (l0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 3 - Location Bit Programming

L(4.0)	LOCATION
00000	VCLK Address 0
00001	VCLK Address 1
00010	VCLK Address 2
00011	VCLK Address 3
00100	VCLK Address 4
00101	VCLK Address 5
00110	VCLK Address 6
00111	VCLK Address 7
01000	VCLK Address 8
01001	VCLK Address 9
01010	VCLK Address 10
01011	VCLK Address 11
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10000	MCLK Address 0
10001	MCLK Address 1
10010	MCLK Address 2
10011	MCLK Address 4

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 4 - Post-Divider Programming

D(1-0)	POST-DIVIDER
00	8
01	4
10	2
11	1

Read/Write* Control Bit

When set to a “0,” the **ICS2595** shift register will transfer its contents to the selected memory register at the completion of the programming sequence.

When this bit is a “1,” the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

"Readback" of a location in the frequency table may be performed by execution the 64 step readback sequence. The readback sequence is shown in Table 2. Note that the readback sequence is essentially the programming sequence (with the R/W* bit set high) followed by the actual data readback.

The bi-directional FS0 pin will convert to output mode after the 42nd nibble write and the logic level output will be that of the first data bit (N0). Subsequent "clocking" by latching FS3 to "0" and then to "1" will shift out the remaining data bits. The last two writes will return the FS0 pin to input mode.

EXTFREQ Input

The **EXTFREQ** input allows an externally generated frequency to be routed to the VCLK or MCLK output pins under device programming control. If the EXTFREQ bit is set (logic “1”) at the selected address location, the frequency applied to the **EXTFREQ** input will be routed to the output instead of the frequency generated by the **VCLK** (or MCLK) PLL.

When setting the EXTFREQ bit to a “1,” be sure that the D0 and D1 bits are not both set to “1” also, unless it is intended that the phase-locked loop be shutdown as well.

Power Conservation

The **ICS2595** supports power conservation by permitting either or both of the phase-locked loops to be disabled. This can be done by programming a particular address to have EXTFREQ, D0, & D1 bits set to a logic “1.” Any frequency applied to the EXTFREQ pin will still be passed through the output multiplexer and appear at the respective output.The crystal oscillator is not affected by this power-down function and will continue to operate normally.

Frequency Synthesizer Description

Refer to the block diagram of the **ICS2595**. The **ICS2595** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency pro-vided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO} = F_{XTAL1} * \frac{N}{R}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.
The feedback divider on the **ICS2595** may be set to any integer value from 257 to 512. This is done by the setting of the **N0**-**N7** bits. The standard reference divider on the **ICS2595** is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The **ICS2595** is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8,
therefore, the VCO frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The output frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired fre-quency within that range will be 0.2%.
If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz (but the upper end is first limited to 145 MHz by the **ICS2595** output driver).

Programming Example

Suppose that we want differential CLK output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz.

The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feed-

back divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818}*43=274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43}*14.31818*\ \frac{1}{2}=45.784\ \text{MHz}$$

The value of the **N** programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the **N** value will be set to 18 (275-257) or 000100102. The **D** bit programming is set to 10 (from Table 4).

Reference Oscillator & Crystal Selection

The **ICS2595** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode). See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2595**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phaselocked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2595** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the X1 pin of the **ICS2595**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The **ICS2595** has three GND pins to reduce the effects of package inductance. All pins are connected to the same potential on the die (the ground bus). All of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2595** has two **VDD** pins which supply of +5 volt power to the output stages. These pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2595**.

The VAA pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin. This will allow the PLL to “track” through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply Voltage ..... -5V to +7 V
Logic inputs ..... 5V to VDD +.5V
Ambient operating temp ..... 0° to 70°C
Storage temperature ..... -85°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs			-	-	-	-
(VS0-3, MS0-1, STROBE):			-	-	-	-
Input High Voltage	Vih		2.0	-	VDD=0.5	V
Input Low Voltage	Vil		VSS-0.5	-	0.8	V
Input High Current	Iih		-	-	10	µA
Input Low Current	Iil		-	-	200	µA
Input capacitance	Cin		-	-	8	pF
XTAL1:			-	-	-	-
Input High Voltage	Vxh		VDD*0.75	-	VDD+0.5	V
Input Low Voltage	Vx1		VSS-0.5	-	VDD*0.25	V
VCLK, MCLK Outputs:			-	-	-	-
Output High Voltage	Voh		2.4	-	-	V
@Ioh=0.4mA			-	-	-	-
Output Low Voltage	Vol		-	-	0.4	V
@Iol=8.0mA			-	-	-	-

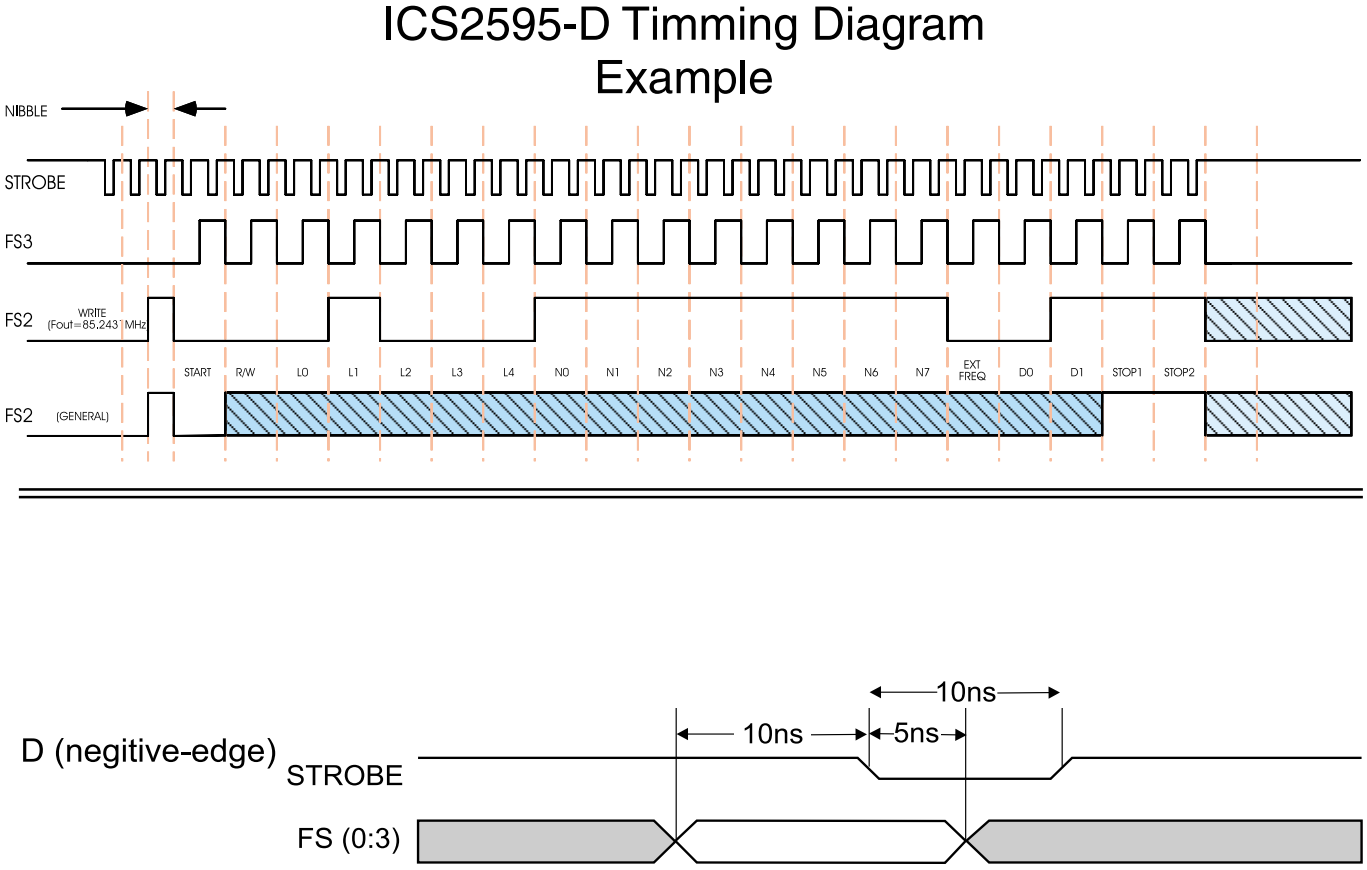
AC Characteristics

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:			-	-	-	-
VCLK, MCLK VCO Frequency	Fvco		60	-	185	MHz
PLL Acquire Time	Tlock		-	500	-	µSec
Crystal Oscillator			-	-	-	-
Crystal Frequency Range	Fxtal		5	-	25	MHz
Parallel Loading Capacitance			-	20	-	pF
XTAL1 Minimum High Time	Txhi		8	-	-	ns
XTAL1 Minimum Low Time	Txlo		8	-	-	ns
Power Supplies:			-	-	-	-
VDD Supply Current	idd		-	-	35	mA
VAA Supply Current	Iaa		-	-	10	mA
Digital Outpluts:			-	-	-	-
VCLK, MCLK, XTALOUT Rise Time @Cload=20pF	Tr		-	-	2	ns
VCLK, MCLK, STALOUT Fall Time @Cload=20pF	Tf		-	-	2	ns

Table 2: Readback Sequence

Nibble	FS0	FS1	FS2	FS3
1	X	X	0	0
2	X	X	1	0
3	X	X	START bit (must be "0")	0
4	X	X	"	1
5	X	X	R/W* control bit (must be "0")	0
6	X	X	"	1
7	X	X	LO (location LSB)	0
8	X	X	"	1
9	X	X	L1	0
10	X	X	"	1
11	X	X	L2	0
12	X	X	"	1
13	X	X	L3	0
14	X	X	"	1
15	X	X	L4 (location MSB)	0
16	X	X	"	1
17	X	X	X	0
18	X	X	X	1
19	X	X	X	0
20	X	X	X	1
21	X	X	X	0
22	X	X	X	1
23	X	X	X	0
24	X	X	X	1
25	X	X	X	0
26	X	X	X	1
27	X	X	X	0
28	X	X	X	1
29	X	X	X	0
30	X	X	X	1
31	X	X	X	0
32	X	X	X	1
33	X	X	X	0
34	X	X	X	1
35	X	X	X	0
36	X	X	X	1
37	X	X	X	0
38	X	X	X	1
39	X	X	STOP1 bit (must be "1")	0
40	X	X	"	1
41	X	X	STOP2 bit (must be '1")	0
42	X	X	"	1
			FS0 becomes output after write #42	
43		X	X	0
44	"	X	X	1
45	N1	X	X	0
46	"	X	X	1
47	N2	X	X	0
48	"	X	X	1
49	N3	X	X	0
50	"	X	X	1
51	N4	X	X	0
52	"	X	X	1
53	N5	X	X	0
54	"	X	X	1
55	N6	X	X	0
56	"	X	X	1
57	N7	X	X	0
58	"	X	X	1
59	EXT-FRE	X	X	0
60	"	X	X	1
61	D0	X	X	0
62	"	X	X	1
63	D1	X	X	0
64	"	X	X	1
	X	X	FS0 returns to input mode after write #64	

"X" = don't care

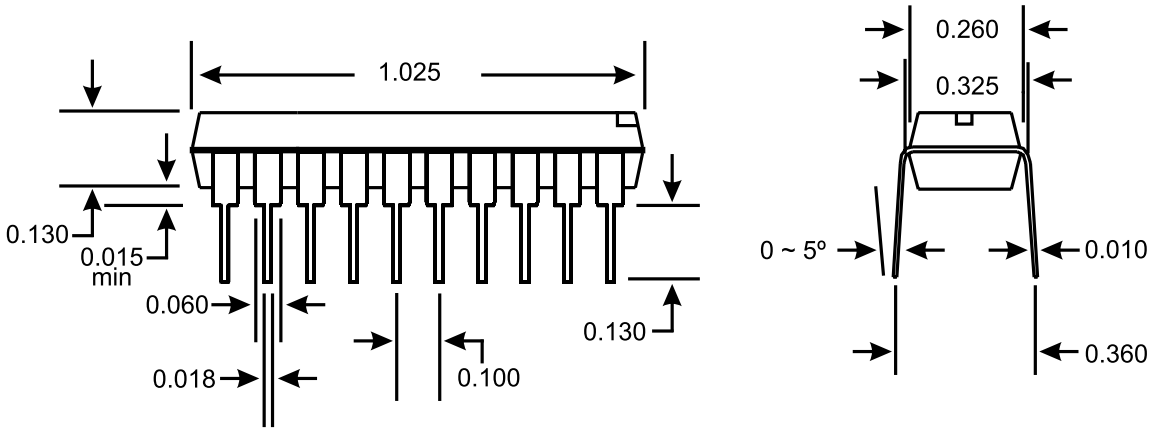


All times shown are minimums.

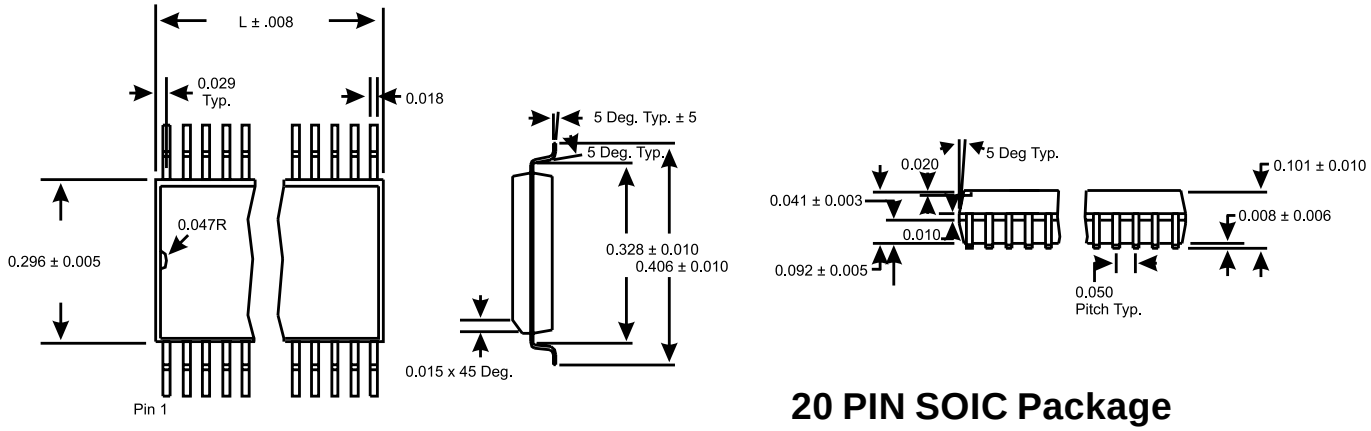
Figure 1. ICS2595 Digital Interface Timing

Frequency Table

PATTERN	ICS2595-02	ICS2595-04
Reference Divider	46	43
VCLK ADDR	VCLK	VCLK
0	100.27	50.28
1	125.90	56.60
2	93.06	64.93
3	36.27	71.92
4	50.76	80.08
5	57.03	89.90
6	External Frequency	62.93
7	45.28	74.92
8	135.99	25.14
9	32.20	28.30
A	110.51	31.46
B	80.21	35.96
C	40.11	40.04
D	45.28	44.95
E	75.51	49.94
F	65.49	64.93
MCLK ADDR	MCLK	MCLK
0	40.42	40.20
1	45.59	41.54
2	N/A	44.54
3	N/A	49.61



20 PIN DIP Package



20 PIN SOIC Package

Ordering Information

ICS2595

Example:

ICS XXXX N-SXX

S=Strobe Option/XX=Default Freq2uencies

Package T ype
N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Where:
"S" denotes strobe option:
"XX"denotes default frequencies:

D - Negative edge triggered