Triple PLL Field Programmable VCXO Clock Synthesizer

Description

The ICS270 field programmable VCXO clock synthesizer generates up to eight high-quality, high-frequency clock outputs including multiple reference clocks from a low-frequency crystal input. It is designed to replace crystals and crystal oscillators in most electronic systems.

Using ICS' VersaClock™ software to configure PLLs and outputs, the ICS270 contains a One-Time Programmable (OTP) ROM for field programmability. Programming features include VCXO, eight selectable configuration registers and up to two sets of four low-skew outputs.

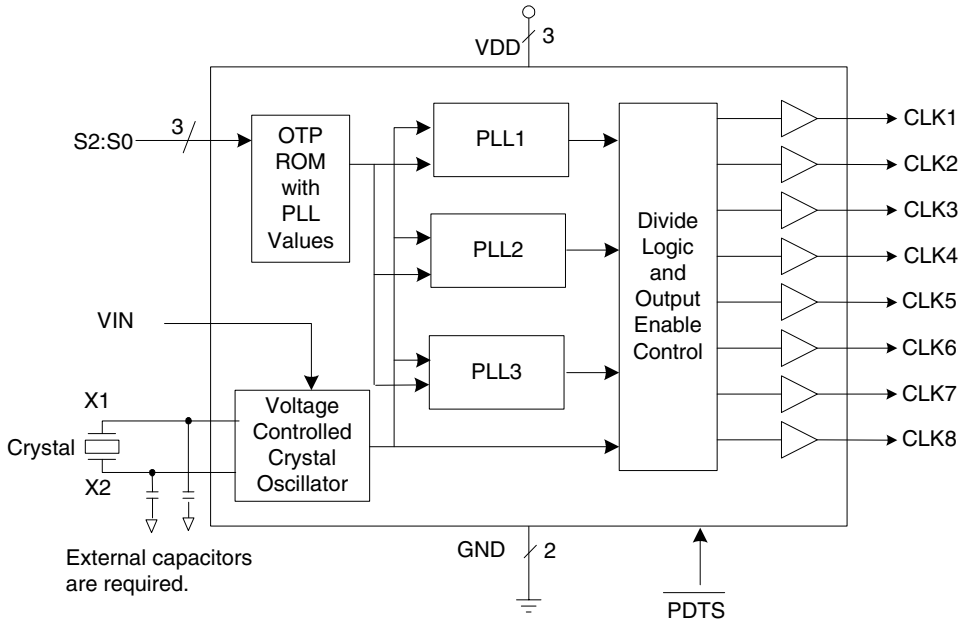
Using Phase-Locked Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace VCXOs, multiple crystals and oscillators, saving board space and cost.

The ICS270 is also available in factory programmed custom versions for high-volume applications.

Features

- Packaged as 20-pin TSSOP
- Eight addressable registers
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3 V
- Input crystal frequency of 5 to 27 MHz
- Up to eight reference outputs
- Up to two sets of four low-skew outputs
- Operating voltages of 3.3 V
- Controllable output drive levels
- Advanced, low-power CMOS process
- Available in Pb (lead) free packaging

Block Diagram



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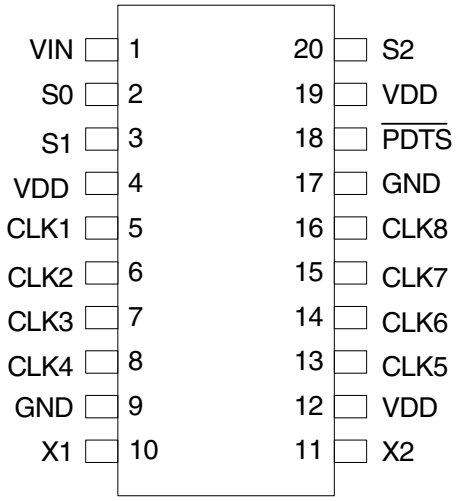
Pin Assignment



20 pin (173 mil) TSSOP

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VIN	Input	Voltage input to VCXO. Zero to 3.3 V signal which controls the VCXO frequency
2	S0	Input	Select pin 0. Internal pull-up resistor.
3	S1	Input	Select pin 1. Internal pull-up resistor.
4	VDD	Power	Connect to +3.3 V.
5	CLK1	Output	Output clock 1. Weak internal pull-down when tri-state.
6	CLK2	Output	Output clock 2. Weak internal pull-down when tri-state.
7	CLK3	Output	Output clock 3. Weak internal pull-down when tri-state.
8	CLK4	Output	Output clock 4. Weak internal pull-down when tri-state.
9	GND	Power	Connect to ground.
10	X1	XI	Crystal input. Connect this pin to a crystal.
11	X2	XO	Crystal Output. Connect this pin to a crystal.
12	VDD	Power	Connect to +3.3 V.
13	CLK5	Output	Output clock 5. Weak internal pull-down when tri-state.
14	CLK6	Output	Output clock 6. Weak internal pull-down when tri-state.
15	CLK7	Output	Output clock 7. Weak internal pull-down when tri-state.
16	CLK8	Output	Output clock 8. Weak internal pull-down when tri-state.
17	GND	Power	Connect to ground.
18	$\overline{\text{PDTS}}$	Input	Power-down tri-state. Powers down entire chip and tri-states clock outputs when low. Internal pull-up resistor.
19	VDD	Power	Connect to +3.3 V.
20	S2	Input	Select pin 2. Internal pull-up resistor.

External Components

The ICS270 requires a minimum number of external components for proper operation.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS270 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias on the decoupling circuit.

Quartz Crystal

The ICS270 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS270 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS270 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

Recommended Crystal Parameters:

Initial Accuracy at 25°C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS270. There should be no via’s between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. See application note MAN05.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the ICS270 to 3.3 V. Connect pin 1 of the ICS270 to the second power supply. Adjust the voltage on pin 1 to 0V. Measure and record the frequency of the CLK output.

2. Adjust the voltage on pin 1 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Error} = 10^6 \times \left[\frac{(f_{3.0V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}} \right] - \text{error}_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by: External Capacitor = 2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25 ppm).

ICS270 Configuration Capabilities

The architecture of the ICS270 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 1024 and N = 1 to 32,895.

The ICS270 also provides separate output divide values, from 2 through 63, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$OutputFreq = REFFreq \cdot \frac{M}{N}$$

Output Drive Control

The ICS270 has two output drive settings. Low drive should be selected when outputs are less than 100 MHz. High drive should be selected when outputs are greater than 100 MHz. (Consult the AC Electrical Characteristics for output rise and fall times for each drive option.)

ICS VersaClock Software

ICS applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS270. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V

Parameter	Condition	Min.	Typ.	Max.	Units
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (ICS270PG/PGLF)	0		+70	°C
Ambient Operating Temperature (ICS270PGI/PGILF)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V
Power Supply Ramp Time			4	ms
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Operating Supply Current Input High Voltage	IDD	Config. Dependent - See VersaClock™ Estimates				mA
		Eight 33.3333 MHz outs, $\overline{PDTS}$ = 1, no load, Note 1		27		mA
		$\overline{PDTS}$ = 0, no load, Note 1		500		µA
Input High Voltage	V_{IH}	S2:S0	VDD/2+1			V
Input Low Voltage	V_{IL}	S2:S0			0.4	V
Input High Voltage, $\overline{PDTS}$	V_{IH}		VDD-0.5			V
Input Low Voltage, $\overline{PDTS}$	V_{IL}				0.4	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA (Low Drive); I_{OH} = -12 mA (High Drive)	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA (Low Drive); I_{OL} = 12 mA (High Drive)			0.4	V
Short Circuit Current	I_{OS}	Low Drive		±40		mA
		High Drive		±70		
Nom. Output Impedance	Z_O			20		Ω

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Internal Pull-up Resistor	R_{PUS}	S2:S0, $\overline{PDTS}$		190		kΩ
Internal Pull-down Resistor	R_{PD}	CLK outputs		220		kΩ
Input Capacitance	C_{IN}	Inputs		4		pF

Note 1: Example with 25 MHz crystal input with eight outputs of 33.$\overline{3}$ MHz, no load, and VDD = 3.3 V.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental crystal	5		27	MHz
Output Frequency			0.314		200	MHz
Crystal Pullability	F_P	0V≤ VIN ≤ 3.3 V, Note 1	100			ppm
VCXO Gain		VIN = VDD/2 ± 1 V, Note 1		110		ppm/V
Output Rise/Fall Time	t_{OF}	80% to 20%, high drive, Note 2		1.0		ns
Output Rise/Fall Time	t_{OF}	80% to 20%, low drive, Note 2		2.0		ns
Duty Cycle		Note 3	40	49-51	60	%
Power-up time		PLL lock-time from power-up		4	10	ms
		$\overline{PDTS}$ goes high until stable CLK output		0.6	2	ms
One Sigma Clock Period Jitter		Configuration Dependent		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from Mean, Configuration Dependent		±200		ps
Pin-to-Pin Skew		Low Skew Outputs	-250		250	ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

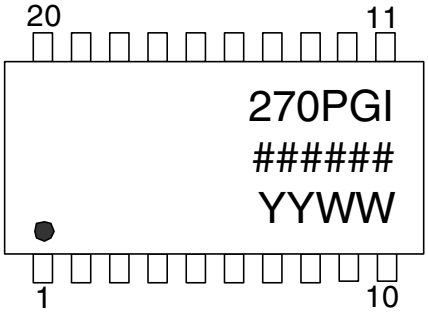
Note 2: Measured with 15 pF load.

Note 3: Duty Cycle is configuration dependent. Most configurations are min 45% / max 55%.

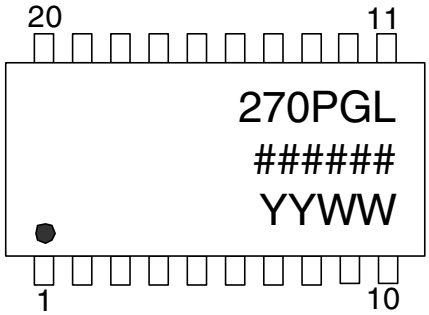
Thermal Characteristics

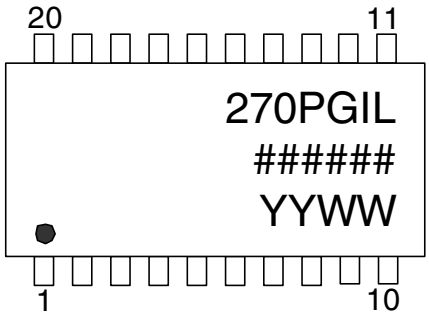
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

Marking Diagrams



Marking Diagrams (Pb free)



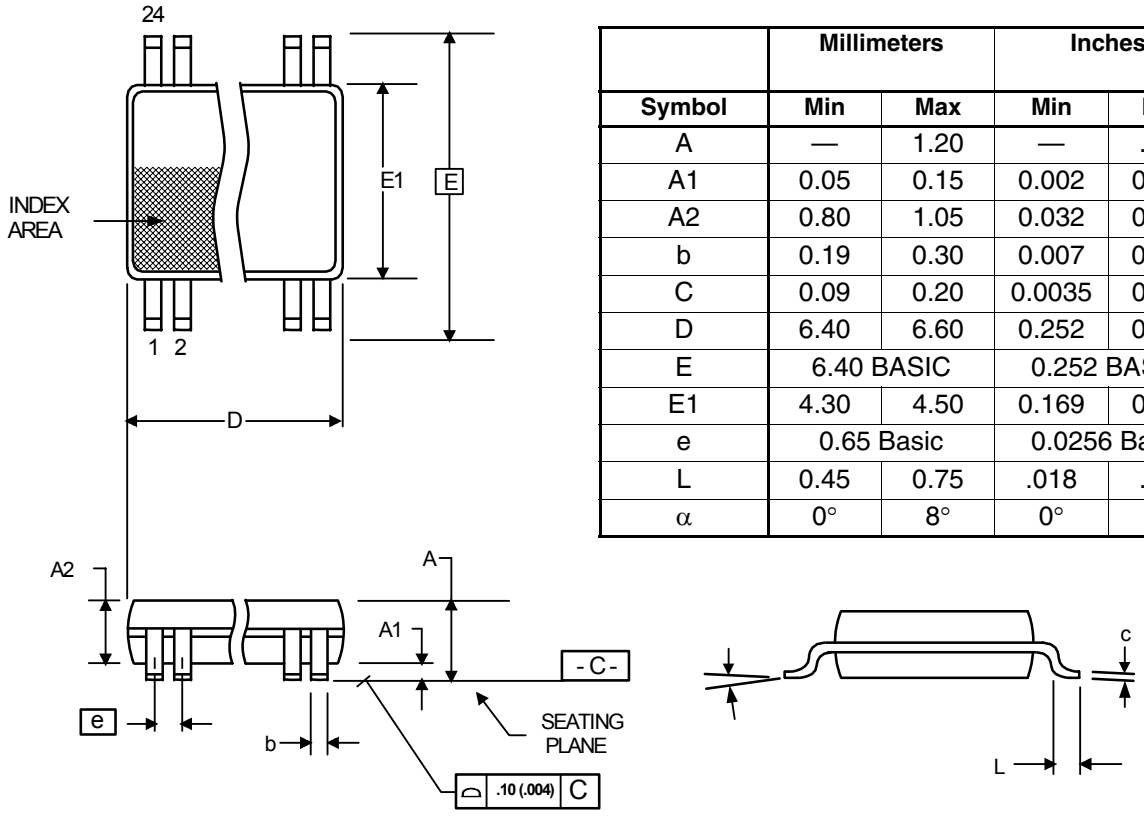


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “I” denotes industrial temperature range (if applicable).
4. “L” denotes Pb (lead) free package.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (20-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	1.20	—	.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	6.40	6.60	0.252	0.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS270PG	See page 7	Tubes	20-pin TSSOP	0 to +70°C
ICS270PGI		Tubes	20-pin TSSOP	-40 to +85°C
ICS270PGLF		Tubes	20-pin TSSOP	0 to +70°C
ICS270PGILF		Tubes	20-pin TSSOP	-40 to +85°C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.