Integrated Circuit Systems, Inc.

ICS31202

Preliminary Product Preview

Dual Frequency Synthesizer

General Description

The **ICS31202** is an integrated Dual Frequency Synthesizer designed for RF Personal Communication systems requiring two independent frequencies. It is one of the lowest cost and smallest size solutions for 900MHz applications.

The **ICS31202** contains two dual modulus prescalers. A 32/33 prescaler can be selected for each RF synthesizer. A common reference divider chain is included for required frequency resolution. Combined with a high quality reference oscillator and loop filter, the **ICS31202** provides the tuning voltages for the external VCO's to generate very stable, low noise RF Local Oscillator signals. Serial data is transferred using a three wire interface. **ICS31202** allows synchronous loading of counters via data line. Crystal inputs are in parallel mode.

The **ICS31202** is fabricated using state-of-the art CMOS process. It is available in a 16-pin 4.4mm TSSOP package with 0.65mm pitch. The **ICS31202** is a direct replacement for Toshiba TB31202.

Features

- Smallest Size Dual RF Sythesizer in the market.
- Integrated Dual PLL with prescalers
- Dual Modulus Prescaler: 32/33
- Provides excellent isolation between Tx, Rx signals.
- Input frequency range of 200-600 MHz
- 2.7V to 4.5V operation
- Software controlled Power Down Mode
- Selectable charge pump current levels (100 to 800 µA)
- Current consumption, 3mA per channel @ 2.7V/500MHz
- Synchronous loading of counters
- High Input sensitivity, 87-100dBµV (-24dBm)
- 16-pin TSSOP Package

Applications

- 900MHz Cordless telephone systems (DCT, ISM, PHS, CT2)
- Personal communications systems (GSM, PDC, PCS)
- Cellular telephone systems
- CATV, Cable Modems
- Other RF/wireless communication systems

Block Diagram

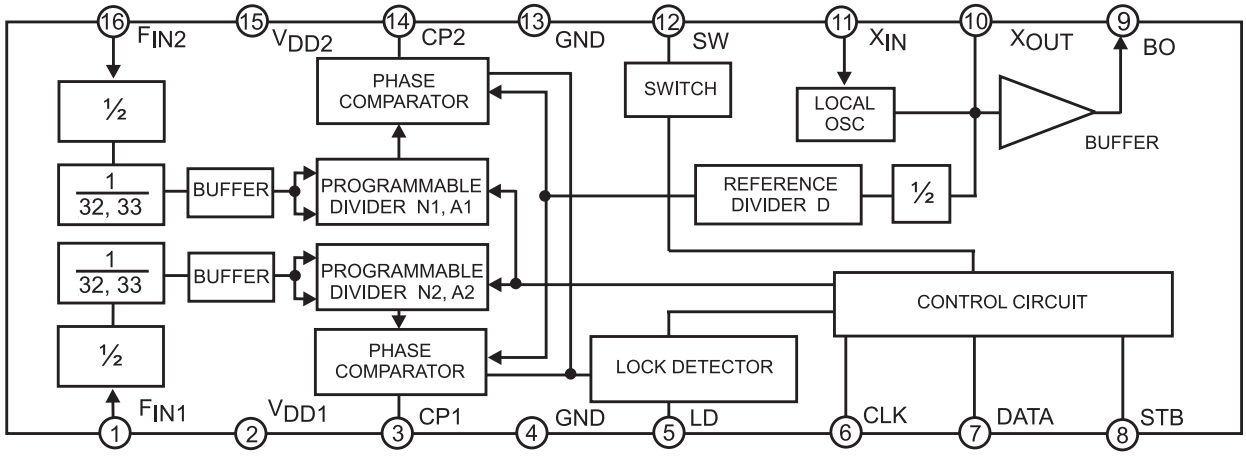


Figure 1

$$F_{IN1} = \frac{F_{XIN} \cdot (32N1 + A1)}{D}$$, D= 4 to 4068, N1 ≤ 4068, A1=0 to 31, Channel Spacing = 2x $\frac{F_{XIN}}{D}$

$$F_{IN2} = \frac{F_{XIN} \cdot (32N2 + A2)}{D}$$, D= 4 to 4068, N2 ≤ 4068, A2=0 to 31, Channel Spacing = 2x $\frac{F_{XIN}}{D}$

Pin Description

Pin No.	Pin Name	Function	
1	F_{IN1}	RF Input 1	
2	V_{DD1}	Supply input for Channel 1 prescalers, dual mode and Charge Pump.	
3	CP1	Charge pump 1 output pin. Charge pump is a constant current output circuit, and output current is varied by serial data input.	
4	GND	Ground pin	
5	LD	Lock detection output pin. LD is an open drain output.	
6	CLK	Clock input pin	3-wire Serial Input Pins
7	DATA	Serial data input pin	
8	STB	Strobe input pin	
9B	O	Buffer amplifier output pin. The signal of on chip oscillator is output through the buffer amplifier.	
10	X_{OUT}	On-chip oscillator signal output pin	
11	X_{IN}	On-chip oscillator signal input.External oscillator signal should be connected to this pin.	
12	SW	External loop filter component select pin. Default mode tristate can be programmed to go to gnd.	
13	GND	Ground input pin. Pin 4 and pin 13 are connected in IC.	
14	CP2	Charge pump 2 output pin.	
15	V_{DD2}	Supply input for Channel 2 prescalers, dual mode and Charge Pump.	
16	F_{IN2}	RF Input 2	

Maximum Ratings (T a = 25ºC)

Characteristics	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	6V	
Power Dissipation*	PD	97	°C/W
Operating Temperature	T_{opr}	-0 to +85	ºC
Storage Temperature	T_{stg}	-55 to +150	ºC

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 2.7V, Ta = 25ºC)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Operating Power Supply Voltage	V_{DD}	Fig. 5	Ta= 0-85ºC	2.7	3	3.3	V
Operating Current Consumption	I_{CC0}	Fig. 5	CH1=300MHz, CH2=300MHz (i) XTAL low power mode 102dBµV		81	1	mA
		Fig. 5	(ii) XTAL high drive mode		8.35	12	mA
Standby Current	I_{CCQ}	Fig. 5	At standby mode, RF Input OFF	---	---	10	µA
F_{IN} Operating Frequency	F_{IN1}	Fig. 7	V_{IN1}=93dBuV	200	---	520	MHz
	F_{IN2}	Fig. 7	V_{IN2}=93dBuV	200	---	520	
F_{in} Input Sensitivity	V_{IN1}	Fig. 7	f_{IN}= 200~520MHz	93	---	107	dBuV
	V_{IN2}	Fig. 7	f_{IN2}= 200~520MHz	93	---	107	
X_{IN} Operating Frequency	f_{XI}	Fig. 7	V_X= 0.5Vp-p, Sinewave	4	---	25	MHz
X_{IN} Input Volltage	V_{XI}	Fig. 7	f_{XI}= 4MHz	102	---	112	dBuV
Input Voltage	V_{IH}	Fig. 5	STB, DATA, CLK	V_{DD}x 0.8	---	---	V
	V_{IL}	Fig. 5	STB, DATA, CLK	---	---	V_{DD}x0.2	
CLK Input Frequency	f_{CLK}	Fig. 5	CLK	---	---	1	MHz
Charge Pump Output Current	I_{CP1}	Fig. 5	"CP1"= 0, "CP2"= 0, V_{CP}=1.1V	---	±100	---	µA
	I_{CP2}	Fig. 5	"CP1"= 0, "CP2"= 1, V_{CP}=1.1V	---	±200	---	
	I_{CP3}	Fig. 5	"CP1"= 1, "CP2"= 0, V_{CP}=1.1V	---	±400	---	
	I_{CP4}	Fig. 5	"CP1"= 1, "CP2"= 1, V_{CP}=1.1V	---	±800	---	
Charge Pump OFF Leakage Current	CP_{OFF}	Fig. 5	Standby mode, V_{CP}= 1.1V	---	---	±1.0	µA
SW Terminal ON Resistance	R_{SW}	Fig. 5	SWON	---	500	---	Ohms
LD Terminal ON Resistance	R_{LD}	Fig. 5	LDON	---	500	---	Ohms
SW Terminal; OFF Leakage Current	SW_{OFF}	Fig. 5	SWOFF	---	---	±1.0	µA
LD Terminal OFF Leakage Current	LD_{OFF}	Fig. 5	LDOFF	---	---	±1.0	µA

Note: Test setup as shown in Fig. 5

Functional Description and Operation

1.0 Entry of Serial Data

1 The 31202 is serially programmed through a 3-wire interface:

1. Falling edge of strobe sets counters to receive data. This is done on Power On reset (POR) too.
2. On the rising edge of CLK, DATA is serially shifted in from the least significant bit to the most significant bit.
3. After all data bits have been shifted serially the rising edge of STB loads the data if 14 or 19 clocks are received.
4. On the rising edge of the STB, the serial data is internally loaded in parallel, if a correct group code is detected again. Data counters internally prevent the loading of data that does not have the valid length and group code.
5. On the falling edge of STB, the internal data counters are reset.

2 Serial Interface Timing

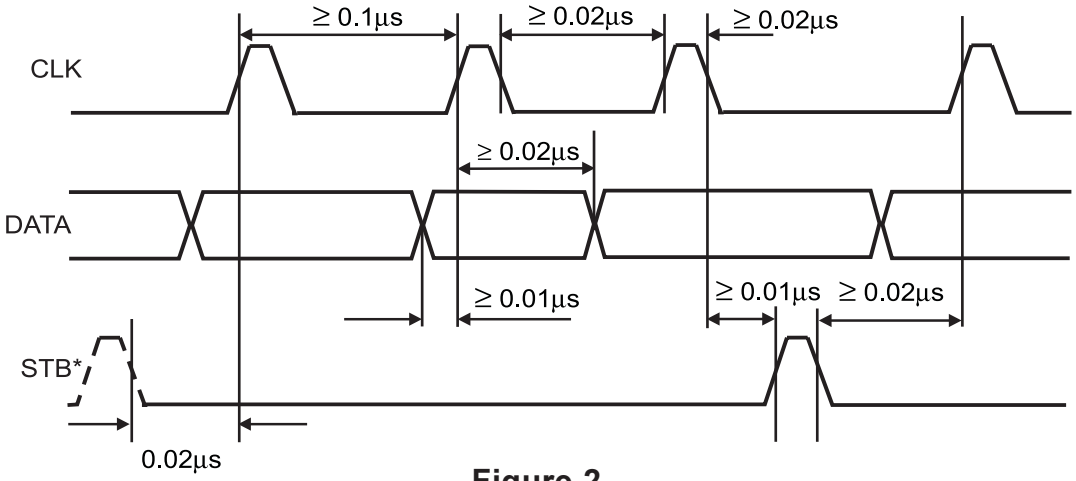


Figure 2

*Although a starting strobe is shown, it is not mandatory if a POR comes.

2.0 Group Code Definiton

The **ICS31202** has four independent control groups. Each group is identified by a 2-bit code attached at the end of the data, as shown in table below.

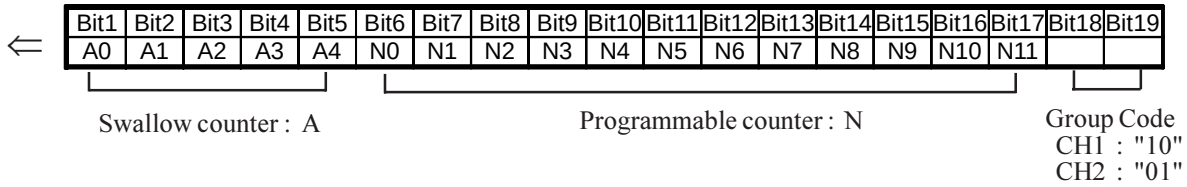
Group Code

CODE	ITEM
10	Selects A1, N1 dividers for CH1
01	Selects A2, N2 dividers for CH2
11	Selects reference divider
00	Selects Mode

Table 1

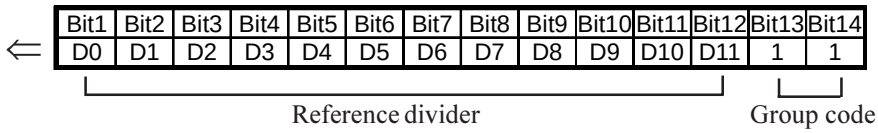
3.0 Programmable Dividers (CH1, CH2)

- CH1 and CH2 are each composed of a 5 bit swallow counter (A), a 12 bit programmable counter (N), and 64/66 Dual Modulus Prescalers.
- The swallow and programmable counters provide division ratios from 2048 to 262,142 in even multiples.
- The group code "10" enables CH1 programming. The group code "01" enables CH2 programming.



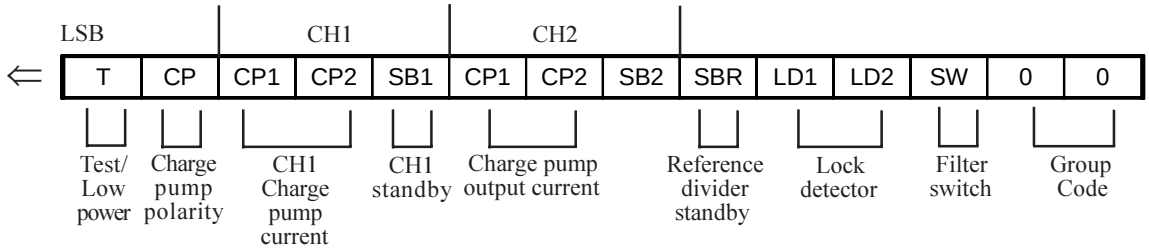
4.0 Reference Divider

- This block sets the reference frequency of the PLL.
- The reference divider is composed of a 12 bit programmable divider and a fixed divide by two divider
- The reference divider is programmable from 16 to 8192 in even multiples.



5.0 Control Register

The Control Register can be programmed to the following modes of operation:



T	: Bit for test mode
CP	: Toggle bit for charge pump output polarity reversal
CP1, 2	: Select bits for charge pump output current
SB1,2	: Standby control bit for CH1, CH2
SBR	: Standby control bit for reference divider
LD1, 2	: Control bit for lock detector output
SW	: Control bit for filter switch

Example:

F_{xtal}= 12MHz
Step = 50KHz
(Phase Dector Rate 25KHz)

$$F_{ref} = \frac{F_{xtal}}{2 \cdot D}$$

$$2D = \frac{F_{xtal}}{F_{ref}} = \frac{12 \times 10^6}{25 \times 10^3} = 480$$

Therefore,
D = (240)d = (111100000)b
A = (21)d = (10101)b
N = (279) = (100010111)b

Assume F_{IN1} = 447.45MHz

$$F_{IN1} = \frac{F_{xtal}}{2D} 2 \cdot (32N+A)$$

$$F_{IN1} = 2 \cdot (32N+A)$$

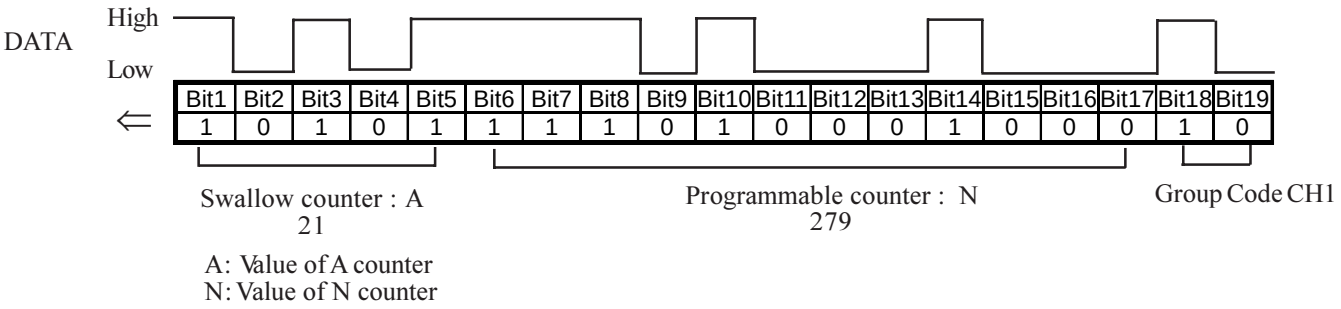
$$\frac{F_{IN1}}{Freq} = \frac{447450}{25} = 17898$$

2 (32N+A) = 17898

N = Quotion (8949/32) = 279

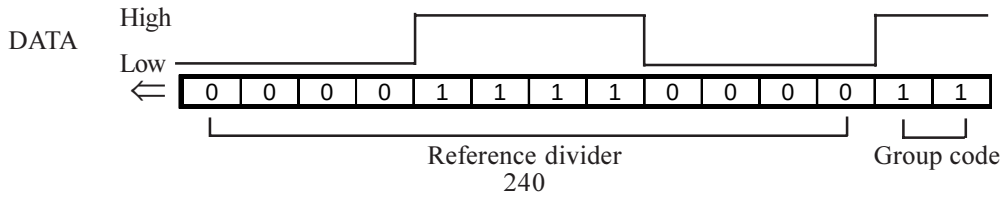
A = Remainder $\frac{(8949)}{32}$ = 21

The Bit patterns for programming CH1 to this frequency would be:

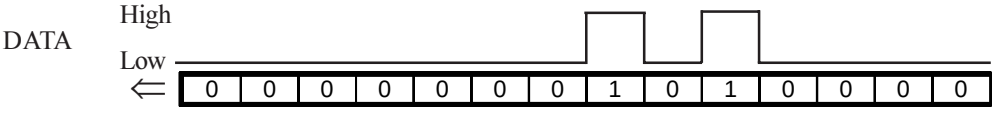


A: Value of A counter
N: Value of N counter

Reference Divider (14 bits)



Control Register (14bits)



As explained later this elects CH1 with 100µA of Charge Pump current.
Note: The evaluation board in Fig 7 implements this example.

5.1 Power on Reset Mode

This section covers the state machine defining the mode of operation at power-on, and the programming of all registers.

On power-on, default condition isTest Mode, T=1 and all dividers are programmed to half their maximum value.

T=1 Test Mode:

Output pins are tapped to internal points in the PLL:

SW⇒ CH2 (F_{IN2} Feedback) Frequency = F_{IN1}/131, 072

LD⇒ CH1 (F_{IN1} Feedback) Frequency = F_{IN2}/131, 072

BO⇒ Reference divider output. Frequency = F_{X2}/4094

Registers in this mode are set as follows:

Bit 1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14
1	000			000			001			100			0
T	CP	CP1	CP2	SB1	CP1	CP2	SB2	SBR	LD1	LD2	SW	Group Code	

Control Registers
Reference Registers

Bit	1Bit2B	it3B	it4B	it5B	it6	Bit7B	it8B	it9	Bit10	Bit11	Bit12
0	0	0	0	0	0	0	0	0	0	0	1

A0	A1	A2	A3	A4	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

CH1 Registers
CH2 Registers

A0	A1	A2	A3	A4	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

T=0 Low Power Mode:

* After Register = 1
* XTAL in Low power mode
* A low phase noise crystal is expected across Xin and Xout. In addition, the crystal should be cut to operate in parallel resonance with low series resistance.
* Alternately Xin expects a minimum signal of 102dBµVAC coupled through a 10nf capacitor.

T=1 High

* XTAL circuit goes into high drive mode - (Maybe required for start up of low frequency crystals)

Note:

On power up, there is an internal signal which is generated to reset dividers and registers to a default state. This signal is active for about 25µs to 30µs. No programming should be performed during this interval.

Once the device is programmed to come out of theTest mode it cannot go back to test mode without a hard POR.

5.2 Charge Pump Output Current: The following settings for each channel determines the charge pump current.

Charge Pump Output Current

CONTROL BIT		CHARGE PUMP OUTPUT CURRENT
CP1	CP2	
00		±100μA
01		±200μA
10		±400μA
11		±800μA

Table 2

5.3 Charge Pump Polarity (CP)

Bit "CP" can be reversed to change charge pump output polarity. Default CP=0

Charge Pump Polarity

CP	OUTPUT POLARITY
0	Positive slope VCO ie . Frequency increases W/Control voltage
1	Negative slope VCO ie . Frequency decreases W/Control voltage

5.4 Lock Detector Output

CONTROL BIT				LOCK DETECTOR OUTPUT STATE
SB1	SB2	LD1	LD2	
0	0	00		L
		0	1	CH2 only detect
		1	0	CH1 only detect
		1	1	CH1 and CH2
01		00		L
		01		H
		1	0	CH1 only detect
		1	1	CH1 only detect
10		00		L
		0	1	CH2 only detect
		10		H
		1	1	CH2 only detect
11		00		L
		01		H
		10		H
		11		H

SB1, SB2 bit:
- 0 : Normal operation
- 1 : Standby

Table 3

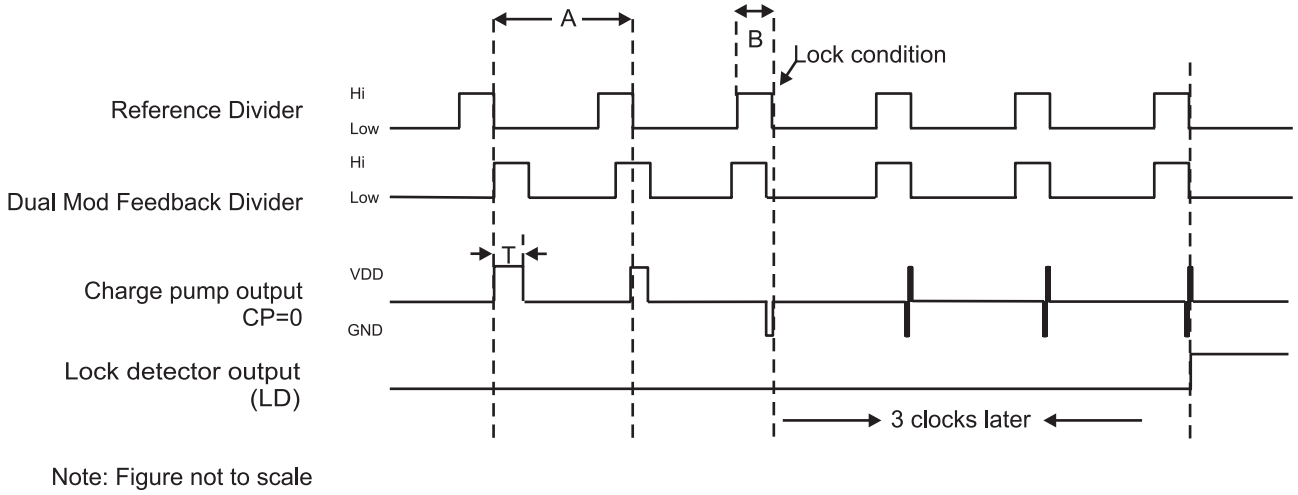


Figure 3

$$A = \frac{\text{Number of divisions by reference divider}}{F_{XI}} \text{ (S)}$$

$$B = 2 / F_{XI} \text{ (S)}$$

Where f_{XI} is the crystal input frequency and T is the difference between the reference counter and channel counter.

In case where T is less than 2 / f_{XI} (T<2 / f_{XI}) continues for more than three cycles of reference counter output, lock detector outputs "H", when appropriately programmed.

5.6 Standby Control

CONTROL BIT			STATE		
SB1	SB2	SBR	CH1	CH2	REF
0	0	*	ON	ON	ON
0	1	*	ON	OFF	ON
1	0	*	OFF	ON	ON
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF

Interlocking mode

REF ON mode

Table 4

5.6 Filter Switch Control

The SW signal is used to modify the loop filter parameters (See Figure 1). When SW bit is set to 1, the open drain output pin 12 goes low. This way an additional loop component can be switched in to alter the loop dynamics.

Filter Switch Control

SW	OUTPUT
0O	FF
1O	N

Table 5

6.0 Crystal Oscillator Ciruitry

Figure 4A shows a schematic of the ICS crystal oscillator circuitry in external Xtal mode. Combined with the external crystal, this implements a Pierce oscillator circuit. Figure 4B shows an AC coupled, low power mode topology using an external signal. The advantage of the ICS crystal driver is that it provides higher circuit gain, which guarantees crystal start-up and provides a wider frequency range. (On chip tuning capacitors (C1, C2) as shown in Figs. 4A and 4B, eliminate the need for external capacitors.) With proper choice of quality crystals at higher frequencies the low power mode can also sustain oscillations.

Guidelines for Crystal Selection

The ICS crystal oscillator circuitry operates the crystal in parallel-resonant mode.

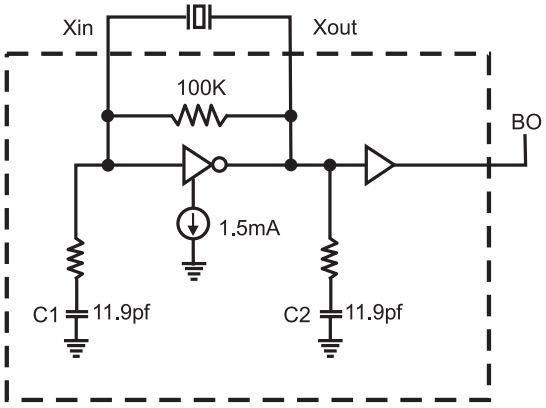


Figure 4A
XTAL Input Mode
T=1

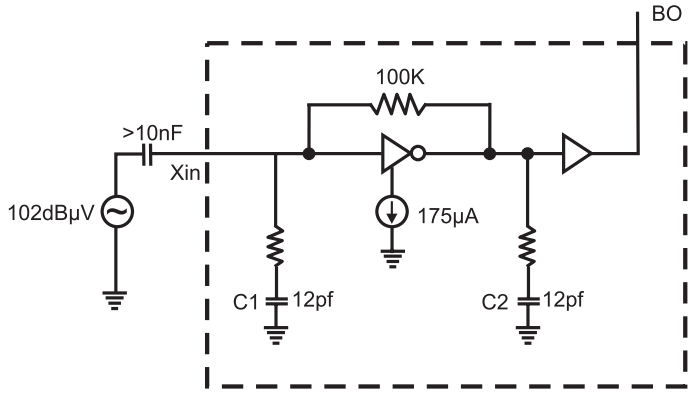


Figure 4B
AC Coupled Signal Input-Low Power Mode
T=0

7.0 Reference Dat a (Typ.) $V_{DD}=3V, F_{in1}, F_{in2}=500MHz$

CH1	CH2	Reference Divider	Low Power Mode	Unit
NN		On	<9.5	mA
NS		On	<5.5	mA
SN		On	<5.5	mA
SS		On	<700	µA
SS		OFF	<10	µA

N : Normal
S : Standby state

8.0 Test Circuit

Test Circuit shown in Figure 5 is used to generate the characterization plots.

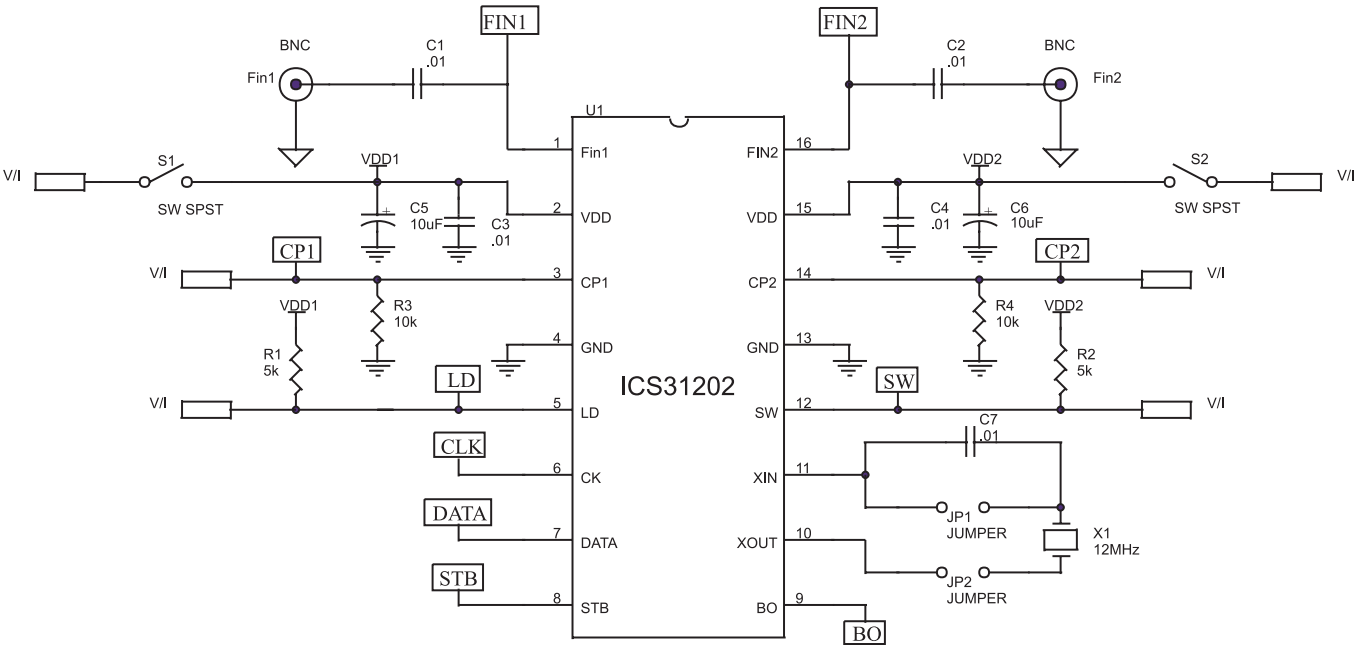


Figure 5
DC/AC Parametric Test Circuit

9.0 Input Impedance Matching

Table 6 shows the input impedance for the Fin1 and Fin2 pins looking into the 10nf capacitor

Frequency (MHz)	Resistor (K Ohms)	Phase Angle (Degrees)
200	1.3	-89.7
300	0.88	-89.7
400	0.65	-89.7
500	0.52	-89.6
600	0.44	-89.6
700	0.38	-89.6

Table 6

Application Circuit for Cordless Phones.

The basic PLL configuration is shown in Figure 6A & 6B. The **ICS31202** provides 2 independent Local Oscillator signals for various wireless applicatons. Each signal provides frequencies up to 600 MHz. The **ICS31202** is ideally suited for 900 MHz applications, such as cordless phones, GSM cellular phones. A low cost frequency doubler allows the LO signals to be increased to the GHz range. This also prevents the pulling of VCO through antenna feedback.

The Phase-Lock Loop consists of an on-chip high stability Reference Ocsillator, Prescalers, Programmable Dividers, Phase Detectors and Charge Pumps. External circuitry includes VCO's and passive loop filter components.

The **ICS31202** phase detector current sources pump charge into the loop filters, which then convert the charge into the VCO's control voltage. When the feedback signals match the reference signals, the phase-lock condition is detected by the LD pin. The VCO will then provide the desired frequency. Loop filter bandwidth can be adjusted to provide faster lock up times initially and return to standard low-noise operation through the use of SW. Figure 6A is actually implemented on the evaluation board described later.

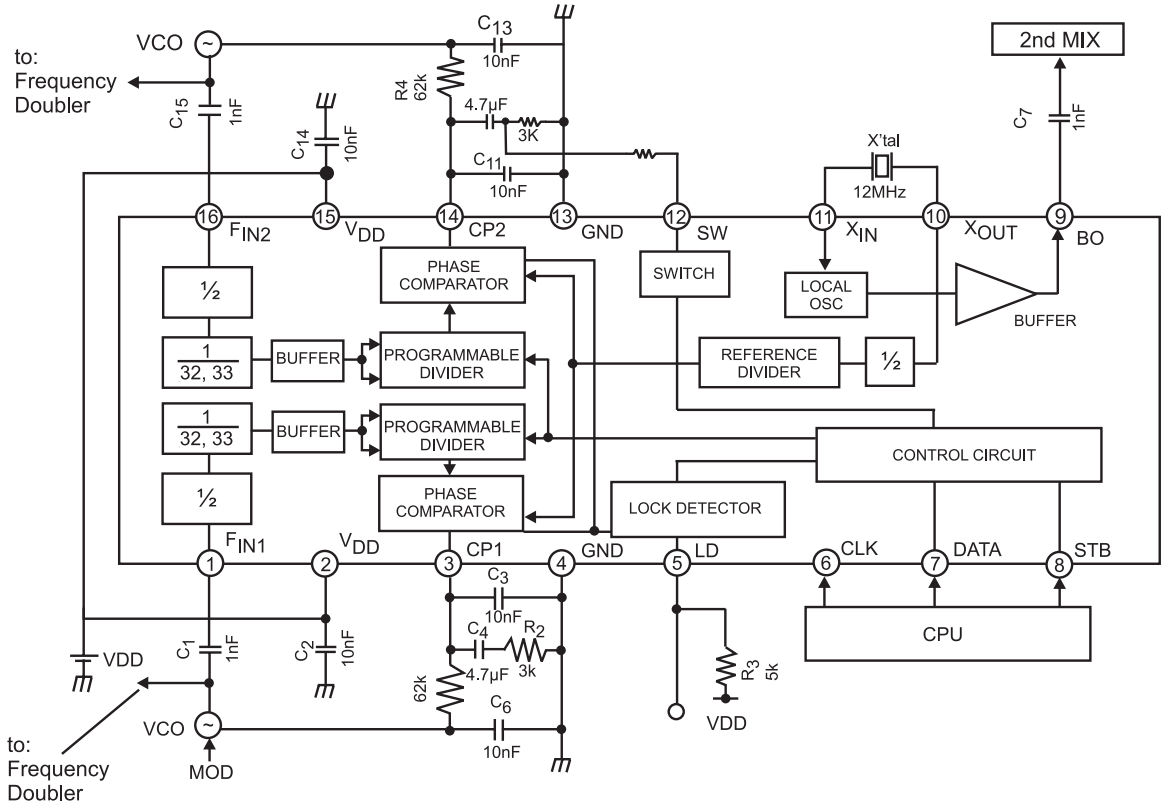


Figure 6A

Figure 6B configuration shows the XIN input being supplied by a 4MHz, 500mV signal.

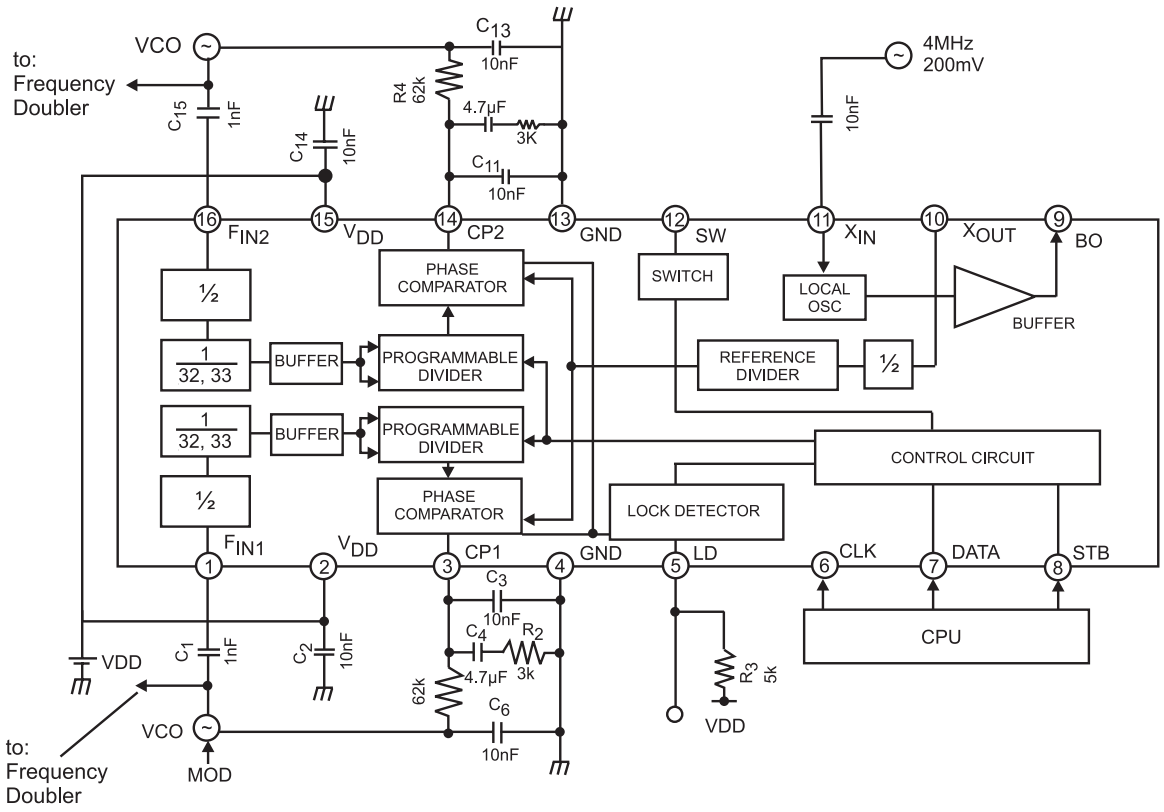


Figure 6B

ICS Evaluation Board

The **ICS31202** Evaluation Board available from ICS allows for a complete evaluation of the chip. It is used in conjunction with the **ICS31202** Programming Tool to simplify the evaluation over the complete frequency range.

The evaluation board with it's frequency doublers has the capability to show the complete spectrum for 900 MHz. applications. The Programming Tool is available on floppy disk and is very simple to install onWindows based PC. The only external equipment needed is a SpectrumAnalyzer. An Excel spreadsheet is also provided to help optimize the loop filter components.

The device is programmed via parallel connector on the evaluation board. It can also be powered through the PC keyboard connector.

Schematic and board layout are included in this data sheet. (Figs 7A, 7B, 7C and 7D)
(Parts list available)

Fig 8 shows Ch 1/Ch 2 output generated on the evaluation board.
The phase noise is less than -95dBc/Hz. @20KHz
The Spurs are less than -65 dBc

Although an integrated VCO IC, MAX2620 has been used in this application, more cost effective discrete VCO's may be used in cost-sensitive applications.

The evaluation circuit is not intended to be used directly in any application, but is hoped to provide a good starting point.

ICS 31202 Evaluation Board Schematic

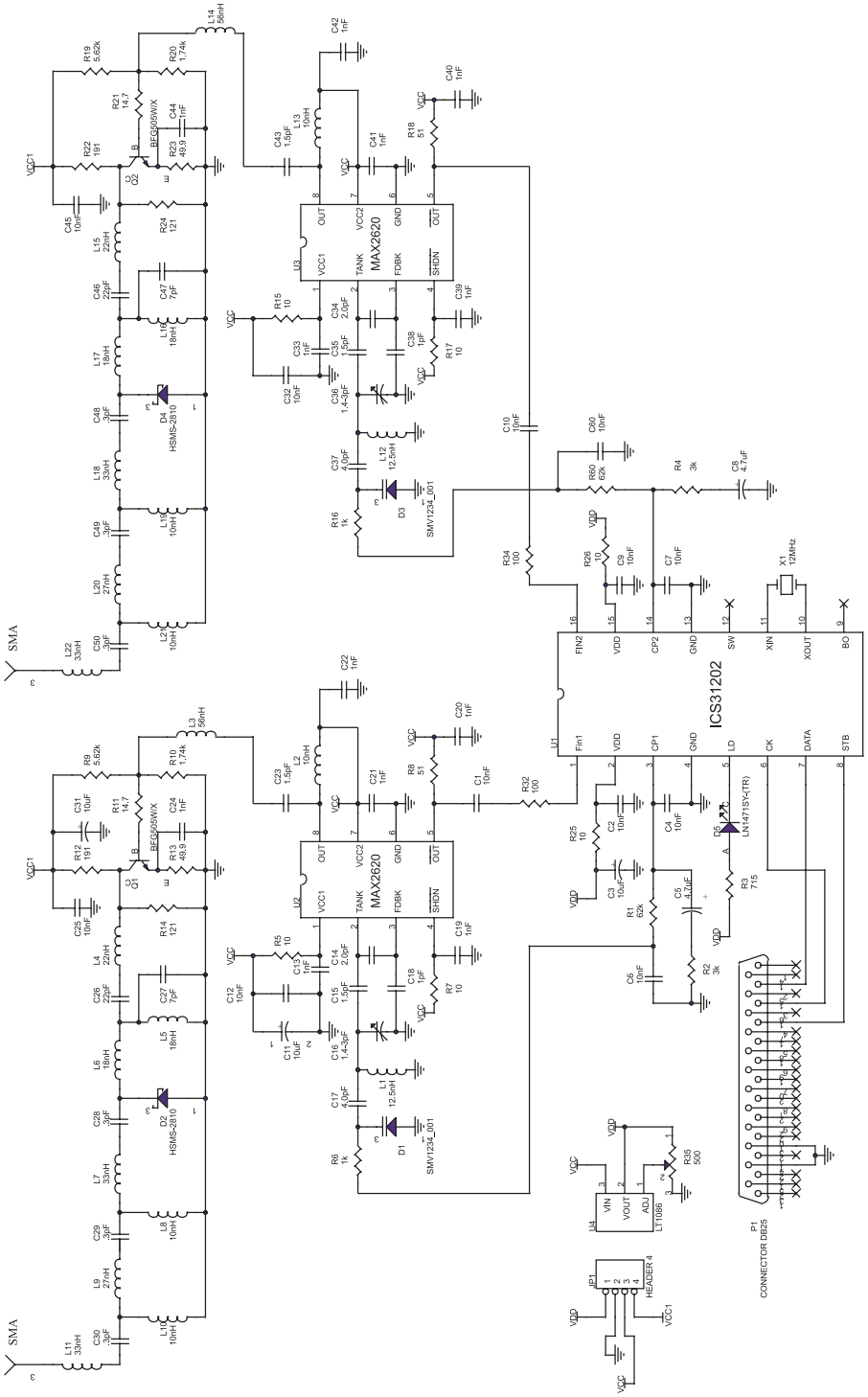


Fig 7A

ICS 31202 Evaluation Board Silkscreen

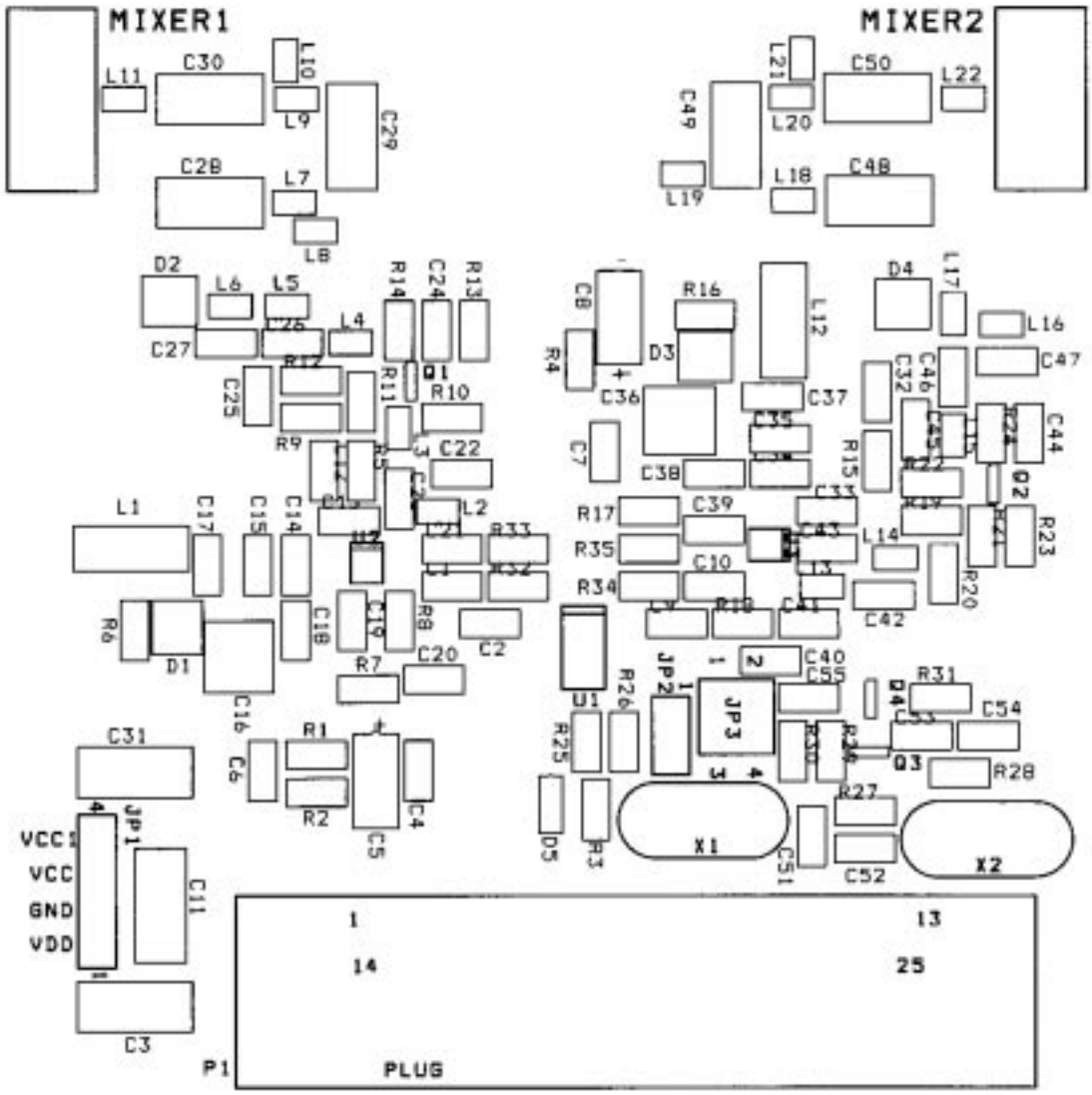


Fig 7B

ICS 31202 Evaluation Board Top Layer

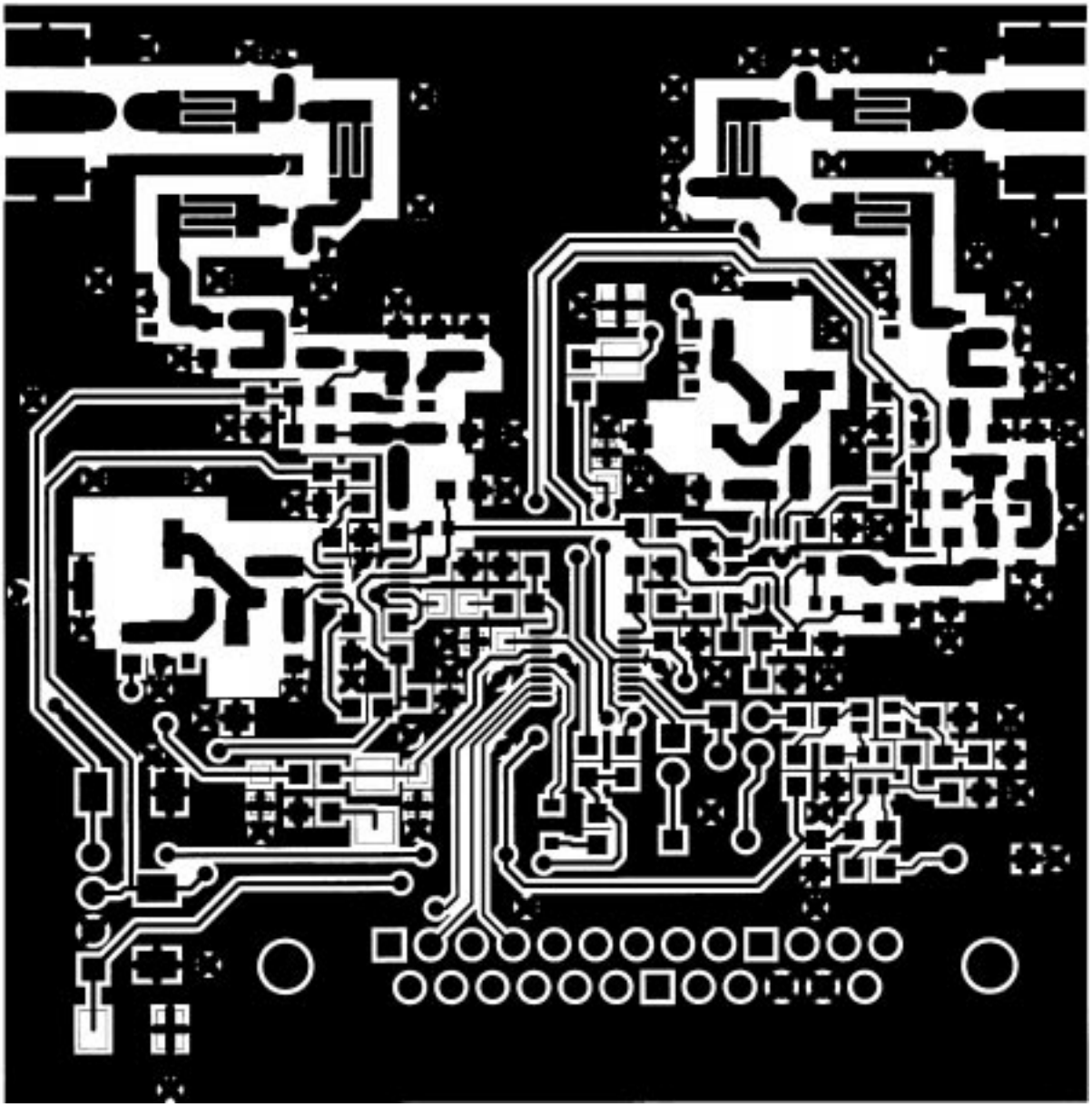


Fig 7C

ICS 31202 Evaluation Board Bottom Layer

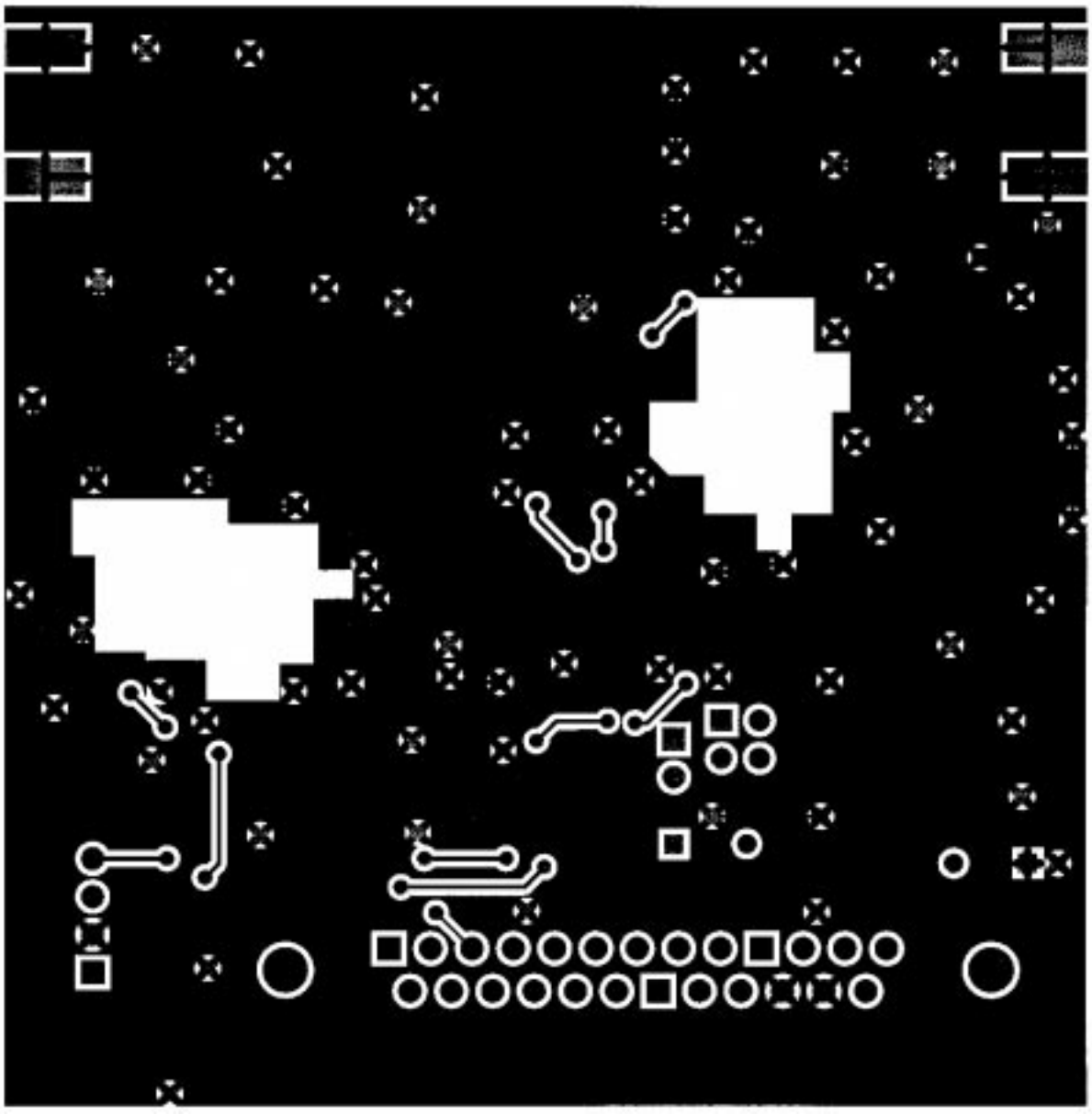


Fig 7D

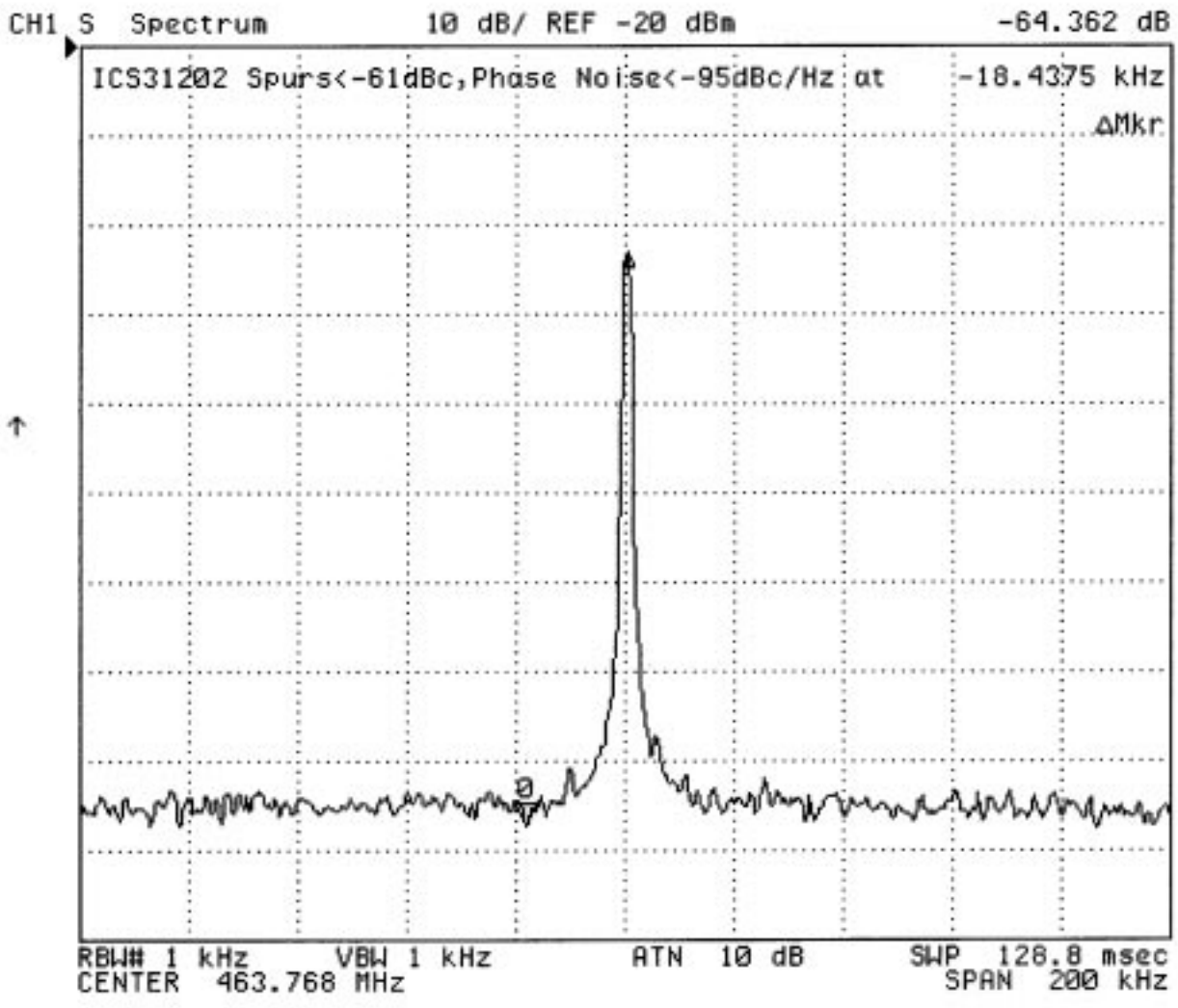
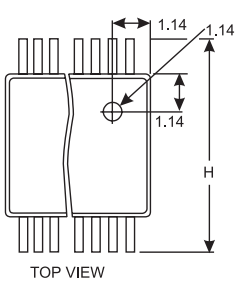
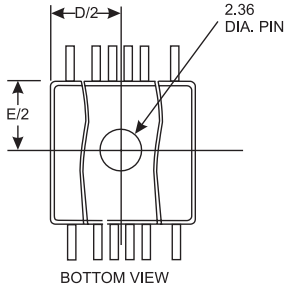
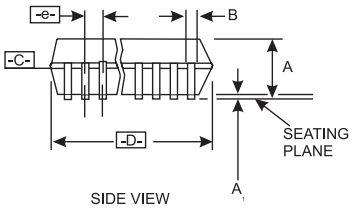


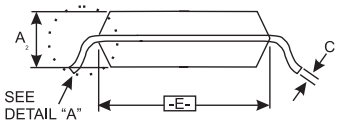
Fig 8

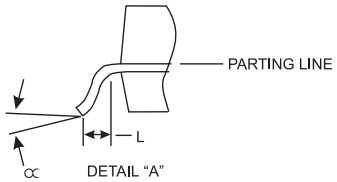
Channel 1 Output Spectrum











16 Pin TSSOP Package

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.068	0.073	0.078
B	0.010	0.012	0.015
C	0.005	0.006	0.008
D	0.239	0.244	0.249
E	0.205	0.209	0.212
e		0.026 BSC	
H	0.150	0.173	
L	0.022	0.030	0.037
∝	0°	4°	8°

Dimensions are in inches

Ordering Information

ICS31202