

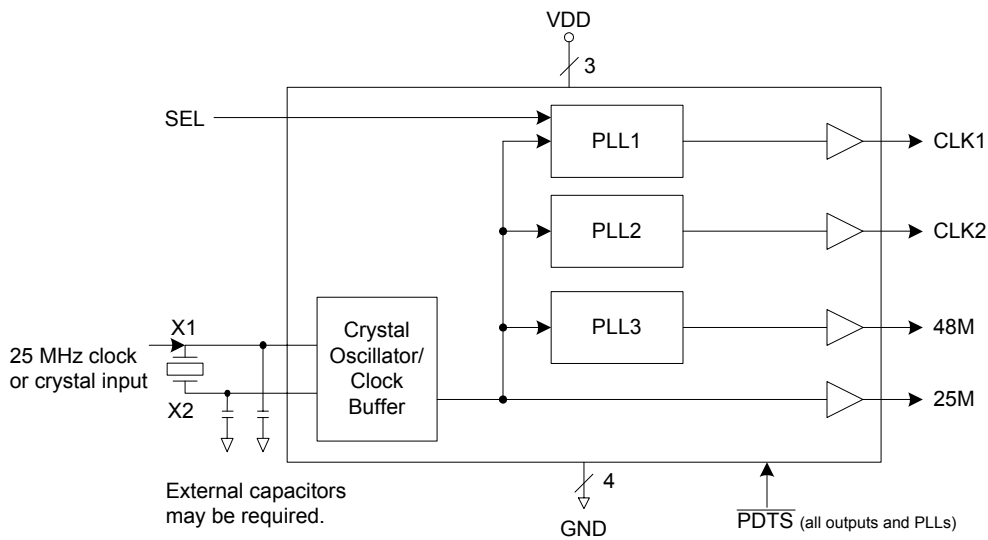
### Description

The ICS448-16 generates four high-quality, high-frequency clock outputs. It is designed to replace multiple crystals and crystal oscillators in networking applications. Using ICS' patented Phase-Locked Loop (PLL) techniques, the device runs from a 25 MHz crystal or clock input.

### Features

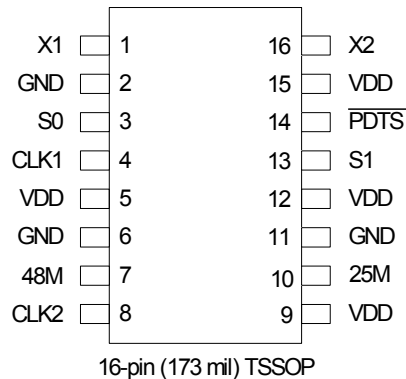
- Packaged in 16-pin TSSOP
- Replaces multiple crystals and oscillators
- Input crystal or clock frequency of 25 MHz
- Zero ppm frequency synthesis error
- Fixed output frequencies of 25 MHz and 48 MHz
- Selectable output frequencies of 24 MHz, 48 MHz, 50 MHz and 66.6666 MHz
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

### Block Diagram





## Pin Assignment



## Output Select Table (MHz)

| S1 | S0 | CLK1    | CLK2 |
|----|----|---------|------|
| 0  | 0  | 50      | 48   |
| 0  | 1  | 66.6666 | 48   |
| 1  | 0  | 50      | 24   |
| 1  | 1  | 66.6666 | 24   |

## Pin Descriptions

| Pin Number | Pin Name                 | Pin Type | Pin Description   |
|------------|--------------------------|----------|---|
| 1          | X1                       | XI       | Crystal input. Connect this pin to a crystal or external clock source.                                    |
| 2          | GND                      | Power    | Connect to ground.  |
| 3          | S0                       | Input    | Select pin 0. Internal pull-up resistor.  |
| 4          | CLK1                     | Output   | Selectable output clock. See table above. Weak internal pull-down when tri-state.                         |
| 5          | VDD                      | Power    | Connect to voltage supply.  |
| 6          | GND                      | Power    | Connect to ground.  |
| 7          | 48M                      | Output   | 48 MHz output clock. Weak internal pull-down when tri-state.  |
| 8          | CLK2                     | Output   | Selectable output clock. See table above. Weak internal pull-down when tri-state.                         |
| 9          | VDD                      | Power    | Connect to voltage supply.  |
| 10         | 25M                      | Output   | 25 MHz output clock. Weak internal pull-down when tri-state.  |
| 11         | GND                      | Power    | Connect to ground.  |
| 12         | VDD                      | Power    | Connect to voltage supply.  |
| 13         | S1                       | Input    | Select pin 1. Internal pull-up resistor.  |
| 14         | $\overline{\text{PDTS}}$ | Input    | Power down tri-state. Powers down entire chip and tri-states outputs when low. Internal pull-up resistor. |
| 15         | VDD                      | Power    | Connect to voltage supply.  |
| 16         | X2                       | XO       | Crystal output. Connect this pin to a crystal. Float for clock input.                                     |



## External Components

### Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS448-16 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01 $\mu$ F must be connected between each VDD and the PCB ground plane.

### Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance), place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$ .

### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal  $(C_L - 6 \text{ pF}) \times 2$ . In this equation,  $C_L$  = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF  $[(16-6) \times 2] = 20$ .

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The 0.01 $\mu$ F decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.
- 2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- 3) To minimize EMI, the 33 $\Omega$  series termination resistor (if needed) should be placed close to the clock output.
- 4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS448-16. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS448-16. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating              |
|-------------------------------|---------------------|
| Supply Voltage, VDD           | 7 V                 |
| All Inputs and Outputs        | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70°C          |
| Storage Temperature           | -65 to +150°C       |
| Junction Temperature          | 125°C               |
| Soldering Temperature         | 240°C               |

## Recommended Operation Conditions

| Parameter   | Min.   | Typ. | Max.   | Units |
|---|--------|------|--------|-------|
| Ambient Operating Temperature                     | 0      |      | +70    | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.135 | +3.3 | +3.465 | V     |

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V  $\pm$ 5%, Ambient Temperature 0 to +70°C

| Parameter                   | Symbol           | Conditions  | Min.    | Typ.     | Max.  | Units      |
|-----------------------------|------------------|---|---------|----------|-------|------------|
| Operating Voltage           | VDD              |   | 3.135   | 3.3      | 3.465 | V          |
| Supply Current              | IDD              | No load, $\overline{\text{PDT}}\overline{\text{S}}=1$   |         | 30       |       | mA         |
| Power Down Current          | IDDPD            | No load, $\overline{\text{PDT}}\overline{\text{S}}=0$   |         | 50       |       | $\mu$ A    |
| Input High Voltage          | V <sub>IH</sub>  |   | 2       |          |       | V          |
| Input Low Voltage           | V <sub>IL</sub>  |   |         |          | 0.8   | V          |
| Output High Voltage         | V <sub>OH</sub>  | I <sub>OH</sub> = -4 mA                                 | VDD-0.4 |          |       | V          |
| Output High Voltage         | V <sub>OH</sub>  | I <sub>OH</sub> = -12 mA                                | 2.4     |          |       | V          |
| Output Low Voltage          | V <sub>OL</sub>  | I <sub>OL</sub> = 12 mA                                 |         |          | 0.4   | V          |
| Short Circuit Current       | I <sub>OS</sub>  | Clock outputs   |         | $\pm$ 70 |       | mA         |
| Input Capacitance, Inputs   | C <sub>IN</sub>  |   |         | 5        |       | pF         |
| Nominal Output Impedance    | Z <sub>OUT</sub> |   |         | 20       |       | $\Omega$   |
| Internal Pull-down Resistor | R <sub>PD</sub>  | Clock outputs   |         | 500      |       | k $\Omega$ |
| Internal Pull-up Resistor   | R <sub>PU</sub>  | S1, S0, $\overline{\text{PDT}}\overline{\text{S}}$ pins |         | 360      |       | k $\Omega$ |



## AC Electrical Characteristics

Unless stated otherwise,  $V_{DD} = 3.3\text{ V} \pm 5\%$ , Ambient Temperature 0 to  $+70^{\circ}\text{C}$

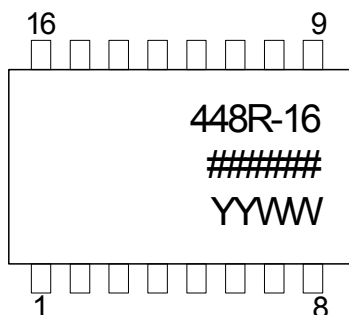
| Parameter                    | Symbol   | Conditions  | Min. | Typ.      | Max. | Units         |
|------------------------------|----------|---|------|-----------|------|---------------|
| Input Frequency              | $f_{IN}$ |   |      | 25        |      | MHz           |
| Output Rise Time             | $t_{OR}$ | 20% to 80%, Note 1  |      | 1         |      | ns            |
| Output Fall Time             | $t_{OF}$ | 80% to 20%, Note 1  |      | 1         |      | ns            |
| Output Clock Duty Cycle      |          | at $V_{DD}/2$ , Note 1                                      | 45   | 50        | 55   | %             |
| Absolute Clock Period Jitter |          | Note 1  |      | $\pm 150$ |      | ps            |
| Frequency Synthesis Error    |          | All clock outputs   |      | 0         |      | ppm           |
| Startup Time                 |          |   |      | 1         | 2    | ms            |
| Output Enable Time           | $t_{OE}$ | $\overline{\text{PDTs}}$ high to output locked to $\pm 1\%$ |      | 20        |      | $\mu\text{s}$ |
| Output Disable Time          | $t_{OD}$ | $\overline{\text{PDTs}}$ low to tri-state                   |      | 2         |      | ns            |

Note 1: Measured with a 15 pF load.

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units                |
|--|---------------|----------------|------|------|------|----------------------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 78   |      | $^{\circ}\text{C/W}$ |
|  | $\theta_{JA}$ | 1 m/s air flow |      | 70   |      | $^{\circ}\text{C/W}$ |
|  | $\theta_{JA}$ | 3 m/s air flow |      | 68   |      | $^{\circ}\text{C/W}$ |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 37   |      | $^{\circ}\text{C/W}$ |

## Marking Diagram



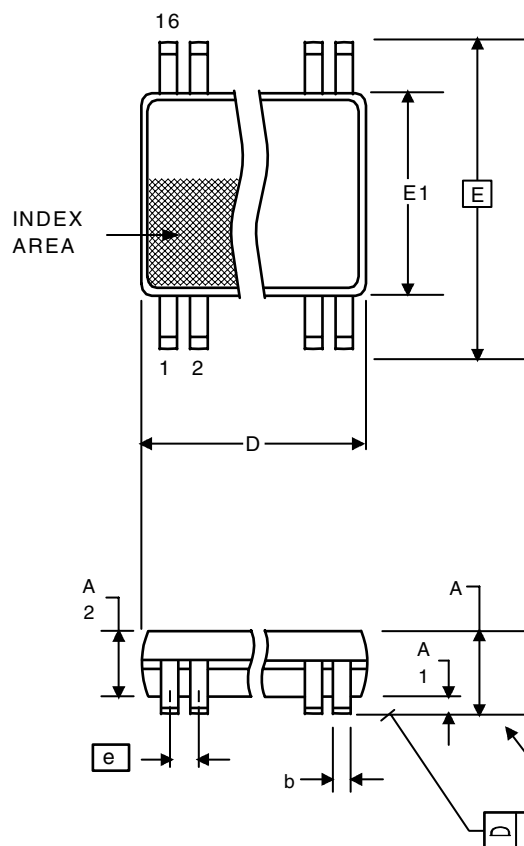
Notes:

- ##### is the lot code.
- YYWW is the last two digits of the year, and the week number that the part was assembled.



## Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol   | Millimeters |      | Inches       |       |
|----------|-------------|------|--------------|-------|
|          | Min         | Max  | Min          | Max   |
| A        | --          | 1.20 | --           | 0.047 |
| A1       | 0.05        | 0.15 | 0.002        | 0.006 |
| A2       | 0.80        | 1.05 | 0.032        | 0.041 |
| b        | 0.19        | 0.30 | 0.007        | 0.012 |
| C        | 0.09        | 0.20 | 0.0035       | 0.008 |
| D        | 4.90        | 5.1  | 0.193        | 0.201 |
| E        | 6.40 BASIC  |      | 0.252 BASIC  |       |
| E1       | 4.30        | 4.50 | 0.169        | 0.177 |
| e        | 0.65 Basic  |      | 0.0256 Basic |       |
| L        | 0.45        | 0.75 | 0.018        | 0.030 |
| $\alpha$ | 0°          | 8°   | 0°           | 8°    |
| aaa      | --          | 0.10 | --           | 0.004 |

## Ordering Information

| Part / Order Number | Marking    | Shipping Packaging | Package      | Temperature |
|---------------------|------------|--------------------|--------------|-------------|
| ICS448G-16          | See page 5 | Tubes              | 16-pin TSSOP | 0 to +70° C |
| ICS448G-16T         |            | Tape and Reel      | 16-pin TSSOP | 0 to +70° C |

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## Revision History

| Rev. | Originator | Date     | Description of Change  |
|------|------------|----------|--|
| C    | P.Griffith | 09/23/04 | Added "weak internal pull-down when tri-state" to pins 4 and 8; removed "Ambient Operating Temperature" from Max Ratings; removed "Operating Voltage" from DC chars; updated Supply/PowerDown current and internal pul-down resistor values in DC chars; updated Output rise/fall and enable/disable times and Startup time from AC chars. |
| D    | R. Wei     | 10/19/04 | Changed package designator on Part Number Ordering info from "R" to "G".   |
| E    | P.Griffith | 03/16/05 | Released to Final and from custom to standard, general purpose device.   |
|      |            |          |  |
|      |            |          |  |