




Description

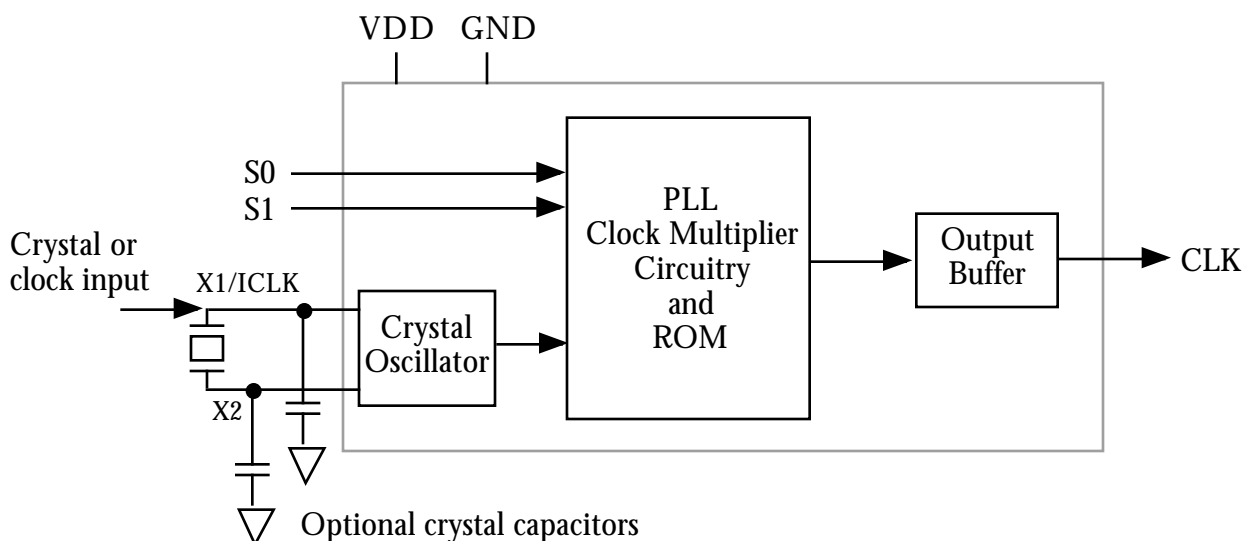
The ICS503 is a member of the LOCO™ family, the most cost effective way to generate a high quality, high frequency clock output from a low frequency crystal or clock input. The name LOCO stands for LOW Cost Oscillator, as it is designed to replace crystals and crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

Stored in the chip's ROM is the ability to generate 9 different multiplication factors, allowing one chip to be used in two or three different applications (see page 2).

Features

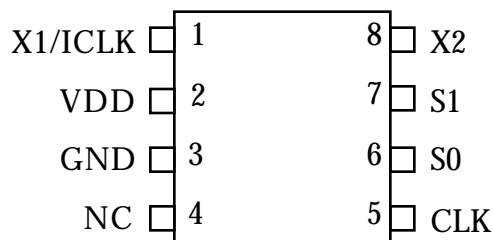
- Packaged as 8 pin SOIC or die 
- ICS' lowest cost PLL clock family
- Generates 16.9344 MHz for stereo codecs from the 14.31818 MHz motherboard clock
- Can be cost effective in replacing a single surface-mount crystal
- Can be driven by other 5xx series
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Low jitter - 50 ps one sigma
- Duty cycle of 45/55 up to 160 MHz
- Operating voltages of 3.0 to 5.5V
- Full CMOS level outputs with 25mA drive capability at TTL levels
- Advanced, low power CMOS process

Block Diagram





Pin Assignment



Clock Decoding Table (MHz)

S1	S0	Multiplier	Typical Input (MHz)	CLK (MHz)	Input Range (MHz) at 5V	Input Range (MHz) at 3.3V
0	0	10	10	100	2 Input 16	2 Input 10
0	M	16	10	160	2 Input 10	2 Input 6
0	1	1.1111	27	30.00	20 Input 50	20 Input 40
M	0	2.4444	14.31818	35.00	10 Input 50	10 Input 40
M	M	2.4164	14.31818	34.60	10 Input 50	10 Input 40
M	1	2.4	14.31818	34.36	10 Input 50	10 Input 40
1	0	5.5873	14.31818	80.00	14 Input 28	14 Input 18
1	M	1.1827	14.31818	16.934	14 Input 30	14 Input 30
1	1	4.1905	14.31818	60.00	5 Input 38	5 Input 24

0 = connect directly to ground, 1 = connect directly to VDD, M = leave unconnected (floating).

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection or clock input.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	NC	-	Nothing is connected to this pin.
5	CLK	O	Clock output per Table above. Output frequency equals input frequency times multiplier.
6	S0	TI	Select 0 for output clock. Connect to GND or VDD or float.
7	S1	TI	Select 1 for output clock. Connect to GND or VDD or float.
8	X2	O	Crystal connection. Leave unconnected for clock input.

Key: I = Input, TI = Tri-Level Input, O = output, P = power supply connection

**Electrical Specifications**

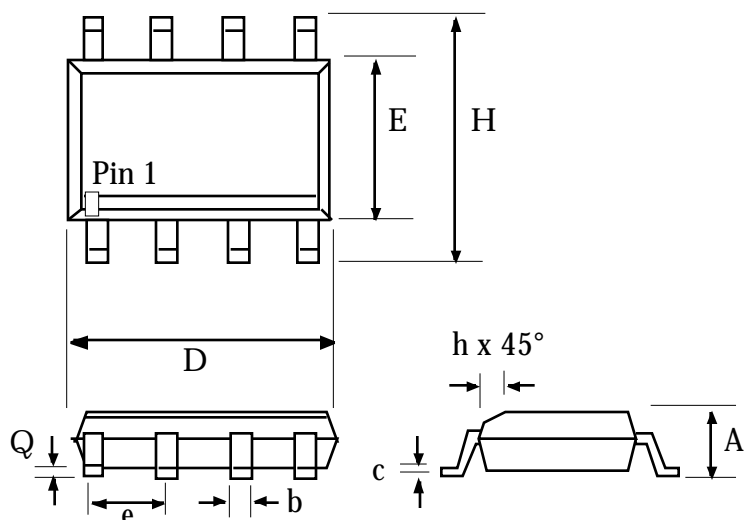
Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	S1, S0	VDD-0.5			V
Input Low Voltage, VIL	S1, S0			0.5	V
Output High Voltage, VOH, CMOS high	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 14 MHz crystal	No Load, 80MHz		16		mA
Short Circuit Current	CLK output		±70		mA
Input Capacitance, S1, S0	Pins 6, 7		4		pF
AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Input Frequency, crystal input	See table on page 2	5		27	MHz
Input Frequency, clock input	See table on page 2	2		50	MHz
Output Frequency	VDD = 4.5 to 5.5V	14		160	MHz
Output Frequency	VDD = 3.0 to 3.6V	14		100	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter	Deviation from mean		±120		ps
One Sigma Clock Period Jitter			50		ps



External Components / Crystal Selection

The ICS503 requires a 0.01 μ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS503 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 6 pF, so a parallel resonant, fundamental mode crystal should be used. If exact tuning of the frequency is required, crystal capacitors should be connected from each of the pins X1 and X2 to ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be equal to $(C_L - 6) * 2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions



8 pin SOIC

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS503M	ICS503M	8 pin SOIC	0-70°C
ICS503MT	ICS503M	8 pin SOIC on tape and reel	0-70°C

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