

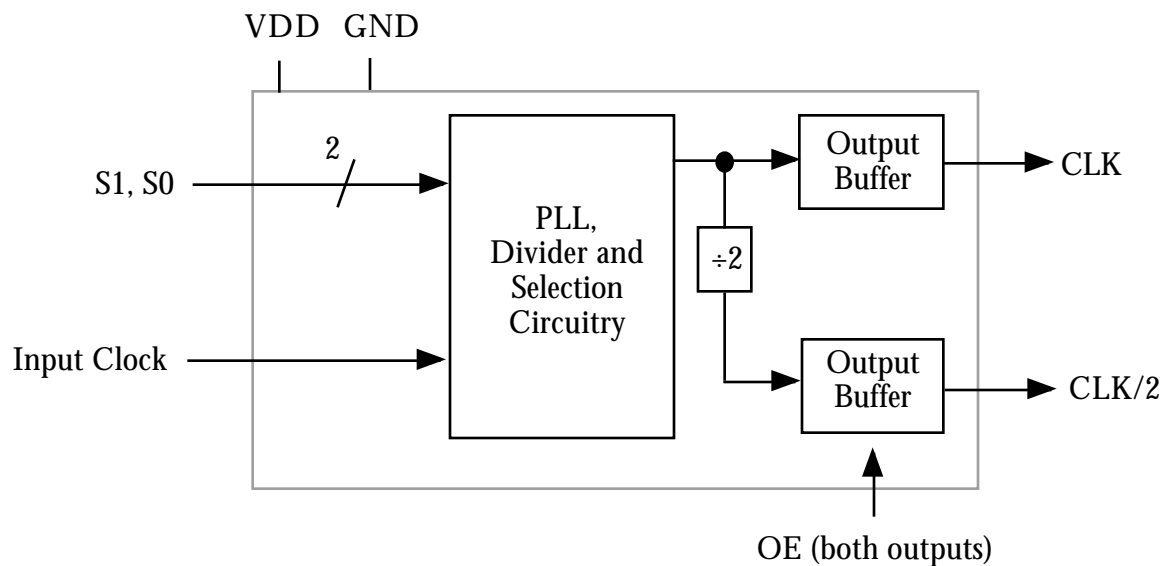


## Description


The ICS541 is a cost effective way to produce a high quality clock output divided from a clock input. The chip accepts a clock input up to 135 MHz at 3.3 V, and by using proprietary Phase Locked Loop (PLL) techniques, produces a divide by 1, 2, 4, or 8 of the input clock. There are two outputs on the chip, one being a low-skew divide by two of the other. So, for instance, if an 80 MHz input clock is used, the ICS541 can produce low skew 80 MHz and 40 MHz clocks, or 40 MHz and 20 MHz clocks, or 20 MHz and 10MHz clocks. The chip has an all-chip power down mode that stops the outputs low, and an OE pin that tri-states the outputs.

The ICS541 is a member of the ICS ClockBlocks™ family of clock building blocks. See the ICS542 and ICS543 for other clock dividers, and the ICS300, 501, 502, and 503 for clock multipliers.

## Block Diagram

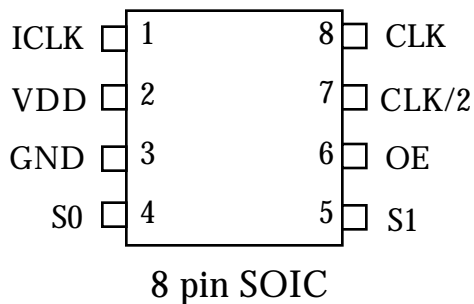


## Features

- Packaged in 8 pin SOIC 
- Low cost clock divider
- Low skew (500ps) outputs. One is  $\div 2$  of other.
- Easy to use with other generators and buffers
- Input clock frequency up to 135 MHz at 3.3 V
- Input clock frequency up to 156 MHz at 5.0 V
- Tolerant of poor input clock duty cycle, jitter.
- Output clock duty cycle of 45/55
- Power Down turns off chip
- Output Enable
- Full CMOS clock swings with 25mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltages of 3.0 to 5.5 V



### Pin Assignment



### Clock Decoding Table

| S1 | S0 | CLK            | CLK/2   |
|----|----|----------------|---------|
| #5 | #4 | pin #8         | pin #7  |
| 0  | 0  | Power Down All |         |
| 0  | 1  | Input/4        | Input/8 |
| 1  | 0  | Input          | Input/2 |
| 1  | 1  | Input/2        | Input/4 |

0 = connect directly to ground.  
1 = connect directly to VDD.

### Pin Descriptions

| Number | Name  | Type | Description   |
|--------|-------|------|---|
| 1      | ICLK  | CI   | Clock input.  |
| 2      | VDD   | P    | Connect to +3.3V or +5V.  |
| 3      | GND   | P    | Connect to ground.  |
| 4      | S0    | I    | Select 0 for output clock. Connect to GND or VDD, per decoding table above. |
| 5      | S1    | I    | Select 1 for output clock. Connect to GND or VDD, per decoding table above. |
| 6      | OE    | I    | Output Enable. Tri-states both output clocks when low.                      |
| 7      | CLK/2 | O    | Clock output per Table above. Low skew divide by two of pin 8 clock.        |
| 8      | CLK   | O    | Clock output per Table above.   |

Key: CI = clock input, I = input, O = output, P = power supply connection

### External Components

The ICS541 requires a 0.01  $\mu$ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS541 to minimize lead inductance. No external power supply filtering is required for this device. A 33  $\Omega$  terminating resistor can be used next to each output pin. If a 3.3 V input clock is applied to the ICLK pin, with the ICS541 at 5 V, the clock must be AC coupled.

**Electrical Specifications**

| Parameter   | Conditions            | Minimum   | Typical  | Maximum   | Units |
|---|-----------------------|-----------|----------|-----------|-------|
| <b>ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)</b> |                       |           |          |           |       |
| Supply Voltage, VDD   | Referenced to GND     |           |          | 7         | V     |
| Inputs  | Referenced to GND     | -0.5      |          | VDD+0.5   | V     |
| Clock Output  | Referenced to GND     | -0.5      |          | VDD+0.5   | V     |
| Ambient Operating Temperature   |                       | 0         |          | 70        | C     |
| Soldering Temperature   | Max of 10 seconds     |           |          | 260       | C     |
| Storage temperature   |                       | -65       |          | 150       | C     |
| <b>DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)</b>                             |                       |           |          |           |       |
| Operating Voltage, VDD  |                       | 3         |          | 5.5       | V     |
| Input High Voltage, VIH, ICLK only, Note 1  | ICLK (Pin 1)          | (VDD/2)+1 |          |           | V     |
| Input Low Voltage, VIL, ICLK only, Note 1   | ICLK (Pin 1)          |           |          | (VDD/2)-1 | V     |
| Input High Voltage, VIH   | S0, S1, OE            | 2         |          |           | V     |
| Input Low Voltage, VIL  | S0, S1, OE            |           |          | 0.8       | V     |
| Output High Voltage, VOH  | IOH=-25mA             | 2.4       |          |           | V     |
| Output Low Voltage, VOL   | IOL=25mA              |           |          | 0.4       | V     |
| Output High Voltage, VOH, CMOS level  | IOH=-4mA              | VDD-0.4   |          |           | V     |
| IDD Operating Supply Current, 80 in, 40+20 out  | No Load, 5.0V         |           | 15       |           | mA    |
| IDD Operating Supply Current, 40 in, 40+20 out  | No Load, 3.3V         |           | 8        |           | mA    |
| Short Circuit Current   | Each Output           |           | ±70      |           | mA    |
| Input Capacitance, S1, S0, OE   | Pins 4, 5, 6          |           | 4        |           | pF    |
| <b>AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)</b>                             |                       |           |          |           |       |
| Input Frequency, clock input  | at VDD = 5V           | 4         |          | 156       | MHz   |
| Input Frequency, clock input  | at VDD = 3.3V         | 4         |          | 135       | MHz   |
| Skew of output clocks   | rising edges at VDD/2 |           |          | 500       | ps    |
| Output Clock Rise Time  | 0.8 to 2.0V           |           | 1        |           | ns    |
| Output Clock Fall Time  | 2.0 to 0.8V           |           | 1        |           | ns    |
| Output Clock Duty Cycle   | at VDD/2              | 45        | 49 to 51 | 55        | %     |

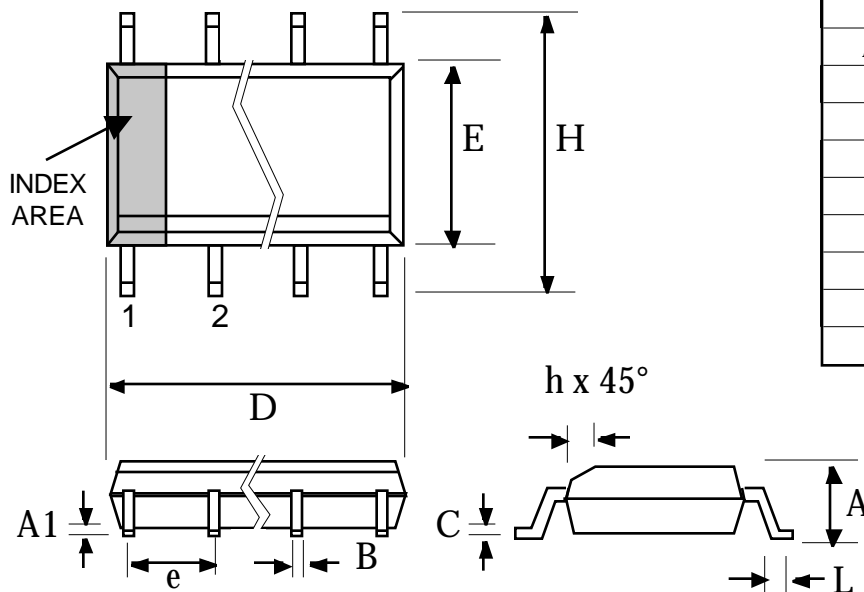
Note 1: CMOS level input; nominal trip point is VDD/2.



**Package Outline and Package Dimensions**

(For current dimensional specifications, see JEDEC Publication No. 95.)

**8 pin SOIC**



| Symbol | Inches   |        | Millimeters |      |
|--------|----------|--------|-------------|------|
|        | Min      | Max    | Min         | Max  |
| A      | 0.0532   | 0.0688 | 1.35        | 1.75 |
| A1     | 0.0040   | 0.0098 | 0.10        | 0.24 |
| B      | 0.0130   | 0.0200 | 0.33        | 0.51 |
| C      | 0.0075   | 0.0098 | 0.19        | 0.24 |
| D      | 0.1890   | 0.1968 | 4.80        | 5.00 |
| E      | 0.1497   | 0.1574 | 3.80        | 4.00 |
| e      | .050 BSC |        | 1.27 BSC    |      |
| H      | 0.2284   | 0.2440 | 5.80        | 6.20 |
| h      | 0.0099   | 0.0195 | 0.25        | 0.50 |
| L      | 0.0160   | 0.0500 | 0.41        | 1.27 |

**Ordering Information**

| Part/Order Number | Marking | Package                     | Temperature |
|-------------------|---------|-----------------------------|-------------|
| ICS541M           | ICS541M | 8 pin SOIC                  | 0 to 70 C   |
| ICS541MT          | ICS541M | 8 pin SOIC on tape and reel | 0 to 70 C   |

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems (ICS) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.

ClockBlocks is a trademark of ICS