



## Description

The ICS5OSK482 is a low cost integrated clock synthesizer solution designed for replacing crystals and crystal oscillators.

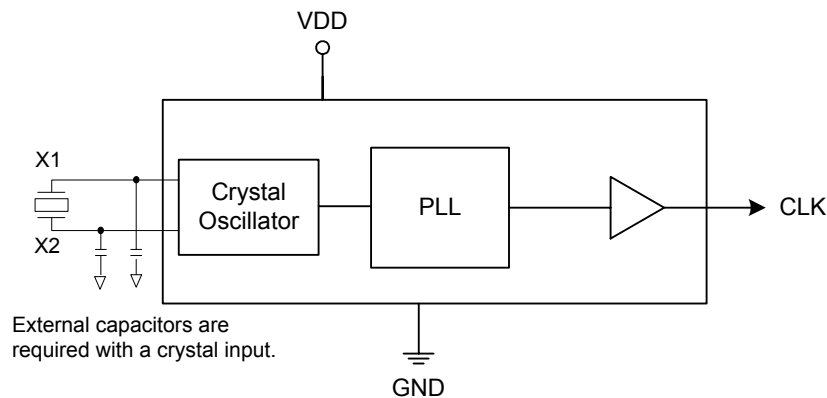
The ICS5OSK482 generates a very accurate 48.00 MHz clock output.

## Features

- 25 MHz crystal input
- The 48.00 MHz CLK output is USB2.0 reference clock compliant
- Output duty cycle 45/55% (worst case)
- Advanced, low-power CMOS process
- Industrial temperature range (-40 to +85°C)
- Packaged in 5-pin TSOT
- 3.3 V supply voltage
- Pb (lead) free package available
- Short term C-C Jitter of 100 ps

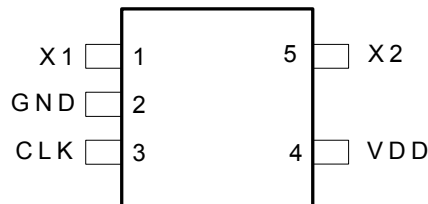
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## Block Diagram





## Pin Assignment



## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	25 MHz crystal input. Connect to a parallel resonant fundamental crystal.
2	GND	Power	Connect to ground.
3	CLK	Output	PLL output clock. Internal pull-down resistor.
4	VDD	Power	Connect to 3.3 V.
5	X2	Output	25 MHz crystal output.

## External Components

### External Crystal

The ICS5OSK482 requires a 14.31818 MHz crystal. In order to minimize ppm errors, the PCB should include pads for crystal capacitors from pins X1 to ground and X2 to ground to optimize the initial accuracy. The capacitor value can be determined by tuning the PCB so that the error on the reference output is equal to the initial crystal error.

### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal  $(C_L - 6 \text{ pF}) \times 2$ . In this equation,  $C_L$  = crystal load capacitance in pF. Example: For a crystal with a 8 pF load capacitance, each crystal capacitor would be 4 pF  $[(8 - 6) \times 2 = 4]$ .



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS50SK482. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+3.465	V

## DC Electrical Characteristics

Unless stated otherwise, VDD=3.3 V  $\pm$ 5% , Ambient temperature 0 to +70°C, CL=15pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage	V <sub>IH</sub>	OE	2.0			V
Input Low Voltage	V <sub>IL</sub>	OE			0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA			0.4	V
IDD Operating Supply Current		No load		TBD		mA
Short Circuit Current		CLK output		$\pm$ 70		mA
On-Chip Pull-up Resistor		OE		270		k $\Omega$
Input Capacitance				4		pF
Nominal Output Impedance				20		$\Omega$



## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C, CL=15pF

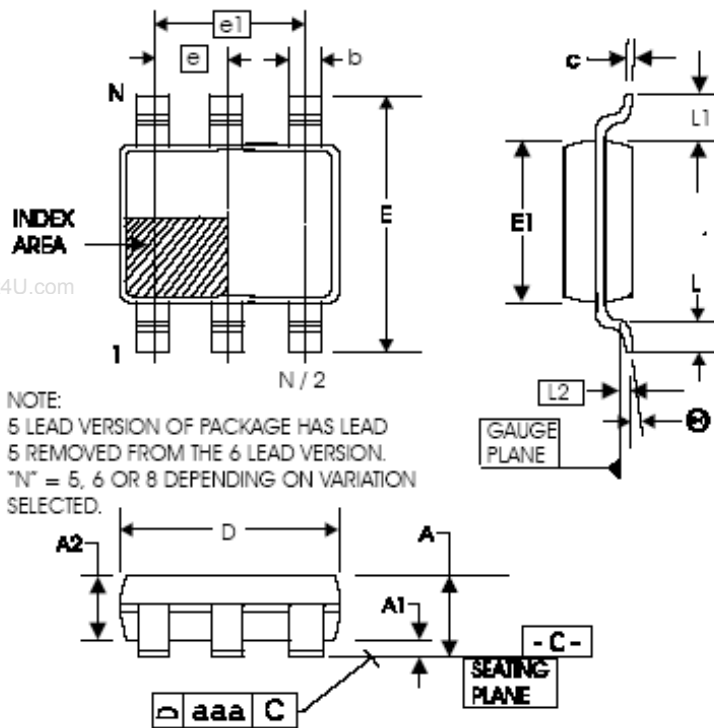
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F <sub>IN</sub>			25		MHz
Output Frequency, VDD = 3.3 V ±5%	F <sub>OUT</sub>	-40°C to +85°C		48		MHz
Output Clock Rise Time	t <sub>OR</sub>	0.8 to 2.0 V, Note 1		1		ns
Output Clock Fall Time	t <sub>OF</sub>	2.0 to 8.0 V, Note 1		1		ns
Output Clock Duty Cycle	t <sub>OD</sub>	1.5 V	45	49-51	55	%
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t <sub>ja</sub>	Deviation from mean, Note 1		TBD		ps

Note 1: Measured with 15 pF load.



## Package Outline and Package Dimensions (5-pin TSOT)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters	
	Min	Max
A	—	1.00
A1	0.01	0.10
A2	0.84	0.90
b	0.30	0.45
c	0.12	0.20
D	2.90 BASIC	
E	2.80 BASIC	
E1	1.60 BASIC	
e	0.95 BASIC	
e1	1.90 BASIC	
L	0.30	0.50
L1	0.60 REF	
L2	0.25 BASIC	
$\theta$	0°	8°
aaa	—	0.10

## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS50SK482TILF	TBD	Tubes	5-pin TSOT	-40 to +85° C
ICS50SK482TILFT	TBD	Tape and Reel	5-pin TSOT	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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