ICS650-07B
Broadcom Clock Source

Description

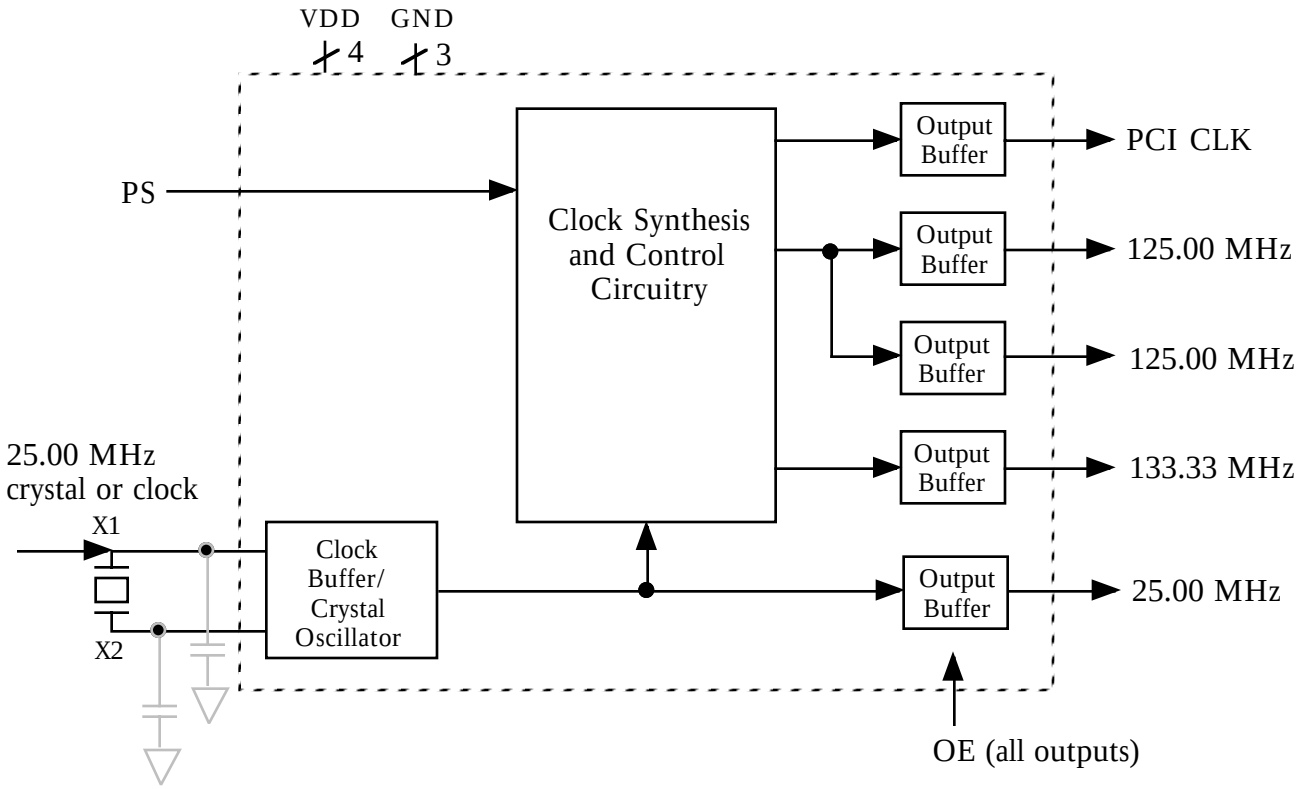
The ICS650-07B is a low cost, low jitter, high performance clock synthesizer customized for Broadcom. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 25.00 MHz clock or fundamental mode crystal input to produce multiple output clocks of 25.0 MHz, two 125.0 MHz, 133.33 MHz, and a selectable 33.3/66.6 MHz clock. All output clocks are frequency locked together. The ICS650-07B outputs all have 0 ppm synthesis error.

Do not use the 125 MHz outputs to drive Gigabit Ethernet SERDES. Instead, the 25 MHz clock can be driven into our ICS601 in the X5 mode. The ICS601 has low enough jitter and phase noise for all popular SERDES.

Features

- Packaged in 20 pin narrow (150 mil) SSOP (QSOP)
- 25.00 MHz fundamental crystal or clock input
- Four fixed output clocks of 25 MHz, 133.33 MHz, and two copies of 125 MHz
- One selectable output clock of 33.3 or 66.6 MHz
- Zero ppm synthesis error in all clocks
- PCI clock switching occurs within 1 µs
- Ideal for Broadcom's BCM5600 chipset
- Full CMOS output swing
- Advanced, low power, sub-micron CMOS process
- 3.0 V to 5.5 V operating voltage

Block Diagram



Optional crystal capacitors are shown and may be required for tuning of initial accuracy (determined once per board).

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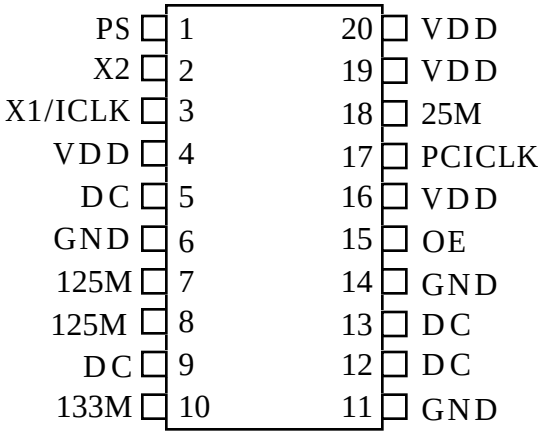
Pin Assignment



20 pin (150 mil) SSOP

PCI CLK Output Select Table

PS	PCICLK
Pin 1	Pin 17
0	33.33 MHz
1	66.66 MHz

0 = connect directly to GND
1 = connect directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	PS	I	PCI Clock frequency select input. Determines PCI CLK output per table above.
2	X2	XO	Crystal connection. Connect to 25 MHz crystal or leave unconnected for a clock input.
3	X1/ICLK	XI	Crystal connection. Connect to 25 MHz fundamental crystal or clock input.
4	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDDs.
5	DC	-	Don't Connect. Do not connect anything to this pin.
6	GND	P	Connect to ground.
7	125M	O	125.0 MHz clock output. Cannot be used for Gigabit Ethernet SERDES.
8	125M	O	125.0 MHz clock output. Cannot be used for Gigabit Ethernet SERDES.
9	DC	-	Don't Connect. Do not connect anything to this pin.
10	133M	O	133.33 MHz clock output.
11	GND	P	Connect to ground.
12	DC	-	Don't Connect. Do not connect anything to this pin.
13	DC	-	Don't Connect. Do not connect anything to this pin.
14	GND	P	Connect to ground.
15	OE	I	Output Enable. Tri-states all outputs when low. Internal pull-up.
16	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDDs.
17	PCICLK	O	PCI Clock output per table above.
18	25M	O	25.0 MHz buffered reference clock output.
19	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDDs.
20	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDDs.

Key: XI, XO = crystal connections; I = Input; O = Output; P = power supply connection

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, X1 pin only		VDD/2 + 1	VDD/2		V
Input Low Voltage, VIL, X1 pin only			VDD/2	VDD/2 - 1	V
Input High Voltage, VIH, PS pin only		VDD-0.5			V
Input Low Voltage, VIL, PS pin only				0.5	V
Output High Voltage, VOH	IOH=-12 mA	2.4			V
Output Low Voltage, VOL	IOL=12 mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4 mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		35		mA
Short Circuit Current	Each output		±50		mA
Internal pull-up resistor	PS, OE		200		kΩ
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Frequency			25.000		MHz
Output Clock Rise Time	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
Frequency error	All clocks			0	ppm
Absolute Jitter, short term	Variation from mean		±200		ps

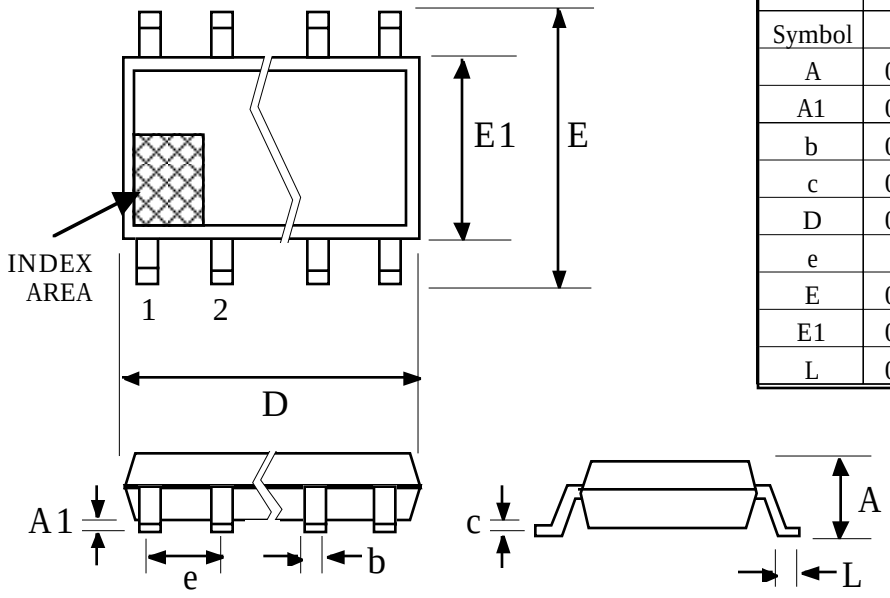
Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

The ICS650-07B requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between each VDD and GND, as close to the ICS650-07B as possible. A series termination resistor of 33 Ω may be used for each clock output. The 25.00 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = (C_L-6) x 2. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



20 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.337	0.344	8.56	8.74
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS650R-07	ICS650R-07	tubes	20 pin SSOP	0-70°C
ICS650R-07T	ICS650R-07	tape and reel	20 pin SSOP	0-70°C