

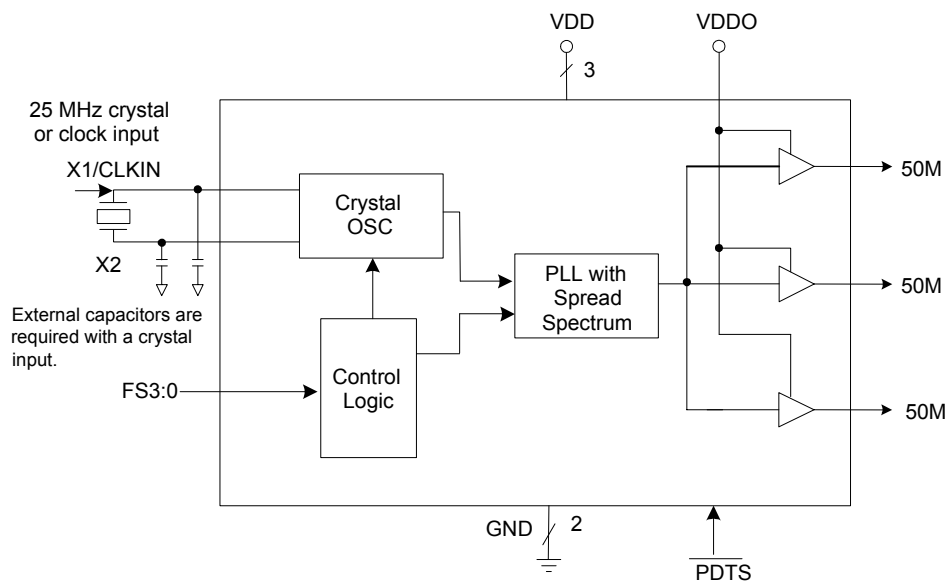
Description

The ICS650-44 is a spread spectrum clock synthesizer intended for video projector and digital TV applications. It generates three copies of an EMI optimized 50 MHz clock signal (EMI peak reduction of 7 to 14 dB on 3rd through 19th harmonics) through the use of Spread Spectrum techniques from a 25 MHz crystal or clock input. The modulation rate is 50 kHz.

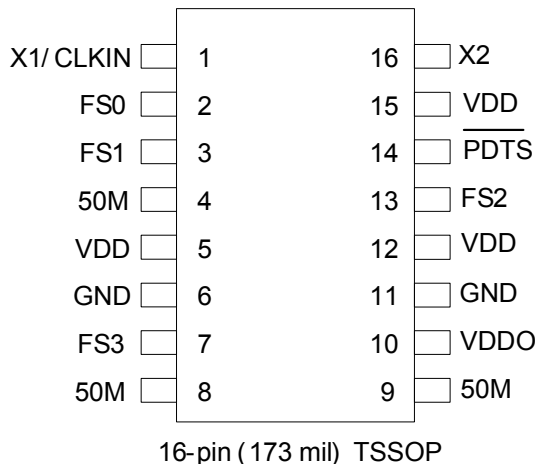
Features

- Packaged in 16-pin TSSOP (173 mil)
- Supply voltages: VDD = 3.3 V, VDDO = 2.5 V
- Peak-to-peak jitter: ± 125 ps typ
- Output duty cycle 45/55% (worst case)
- 25 MHz crystal or reference clock input
- Zero (0) ppm frequency error on all output clocks
- Advanced, low-power CMOS process
- Industrial temperature range (-40 to +85°C)
- Pb (lead) free package

Block Diagram



Pin Assignment



Spread Spectrum and Output Configuration Table

FS3	FS2	FS1	FS0	Spread Type	SS Out
0	0	0	0	Center	±0.25
0	0	0	1	Center	±0.50
0	0	1	0	Center	±0.75
0	0	1	1	Center	±1.00
0	1	0	0	Center	±1.25
0	1	0	1	Center	±1.50
0	1	1	0	Center	±1.75
0	1	1	1	Center	±2.00
1	0	0	0	Down	-0.5
1	0	0	1	Down	-0.75
1	0	1	0	Down	-1.0
1	0	1	1	Down	-1.25
1	1	0	0	Down	-1.5
1	1	0	1	Down	-1.75
1	1	1	0	Down	-2.0
1	1	1	1	Off	Off

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal input. Connect this pin to a 25 MHz crystal or external input clock.
2	FS0	Input	Select pin 0. Internal pull-up resistor. See table on page 2.
3	FS1	Input	Select pin 1. Internal pull-up resistor. See table on page 2.
4	50M	Output	Spread Spectrum output. Weak internal pull-down when tri-stated.
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to ground.
7	FS3	Input	Select pin 3. Internal pull-up resistor. See table on page 2.
8	50M	Output	Spread Spectrum output. Weak internal pull-down when tri-stated.
9	50M	Output	Spread Spectrum output. Weak internal pull-down when tri-stated.
10	VDDO	Power	Connect to +2.5 V.
11	GND	Power	Connect to ground.
12	VDD	Power	Connect to +3.3 V.
13	FS2	Input	Select pin 2. Internal pull-up resistor. See table on page 2.
14	PDTS	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up.
15	VDD	Power	Connect to +3.3 V.
16	X2	Output	Crystal Output. Connect this pin to a 25 MHz crystal. Do not connect if clock input is used.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS650-44 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01 μ F must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

Crystal Load Capacitors

The device crystal connections should include pads for

small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 6 \text{ pF})^2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF $[(16-6) \times 2] = 20$.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01 μ F decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33 Ω series termination resistor should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS650-44. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-44. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature (max. of 10 seconds)	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	–	+85	°C
Power Supply Voltage (VDD, with respect to GND)	+3.135	+3.3	+3.465	V
Power Supply Voltage (VDDO)	+2.375	+2.5	+2.625	V
Power Supply Ramp Time, Figure 4			4	ms

DC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDO} = 2.5\text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD	no load		27		mA
		$\overline{PDTS} = 0$, no load		40		uA
	IDDO	no load		4		mA
		$\overline{PDTS} = 0$, no load		1		uA
Input High Voltage	V_{IH}	FS3:0, \overline{PDTS}	2			V
Input Low Voltage	V_{IL}	FS3:0, \overline{PDTS}			0.8	V
Input High Voltage	V_{IH}	X1/CLKIN	$0.7 \times V_{DD}$			V
Input Low Voltage	V_{IL}	X1/CLKIN			$0.3 \times V_{DD}$	V
Output High Voltage	V_{OH}	$I_{OH} = -4\text{ mA}$	1.8			V
Output Low Voltage	V_{OL}	$I_{OL} = 4\text{ mA}$			0.6	V
Short Circuit Current	I_{OS}			± 50		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}	FS3:0, \overline{PDTS}		360		k Ω
Input Leakage Current	I_I	FS3:0, \overline{PDTS} , $V_{IN} = V_{DD}$		1		uA
Internal Pull-down Resistor	R_{PD}	CLK outputs		900		k Ω
Input Capacitance	C_{IN}	Inputs		4		pF

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDO} = 2.5\text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^\circ\text{ C}$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Crystal or clock input		25		MHz
Spread Spectrum Modulation Frequency				50		kHz
Duty Cycle	t_2/t_1	At $V_{DD}/2$, Note 1 and Figures 1 and 2	45	50	55	%
Output Fall Time	t_3	80% to 20%, Note 1 and Figures 1 & 3		1.5		ns
Output Rise Time	t_4	20% to 80%, Note 1 and Figures 1 & 3		1.5		ns
One Sigma Clock Period Jitter		Note 1		30		ps
Absolute Jitter, Peak-to-Peak	t_{ja}	Deviation from mean, Note 1 & Figures 1 and 6		± 125		ps
Output Enable Time	t_{EN}	$\overline{PDT\overline{S}}$ high to PLL locked to within 1% of final value, Figure 5		2.5	5	ms
Output Disable Time	t_{DIS}	$\overline{PDT\overline{S}}$ low to tri-state, Figure 5		20		ns
Output-to-Output Skew				± 180		ps
Power-up Time	t_P	PLL lock-time from power-up to 1% of final value, Figure 4		6	10	ms

Note 1: Measured with 5 pF load.

Timing Diagrams

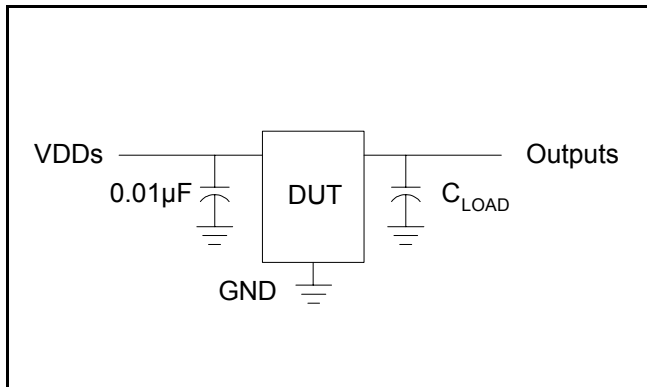


Figure 1: Test and Measurement Setup

Figure 5: $\overline{\text{PDTs}}$ to Stable Clock Output Timing

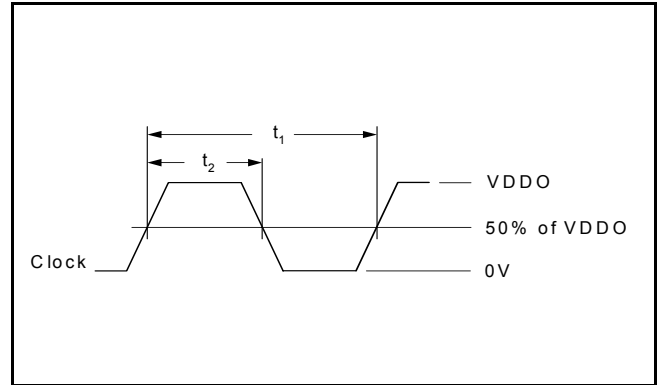


Figure 2: Duty Cycle Definitions

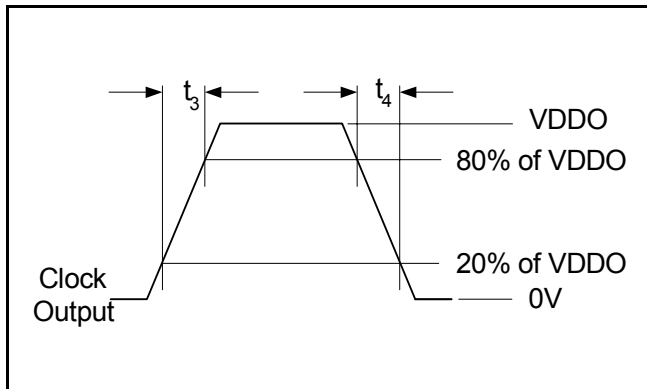


Figure 3: Rise and Fall Time Definitions

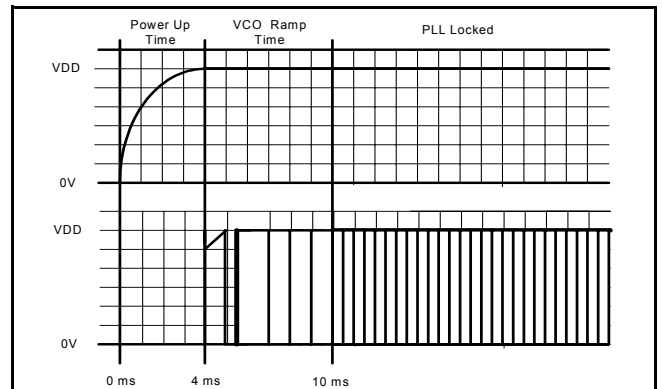


Figure 4: Power Up and PLL Lock Timing

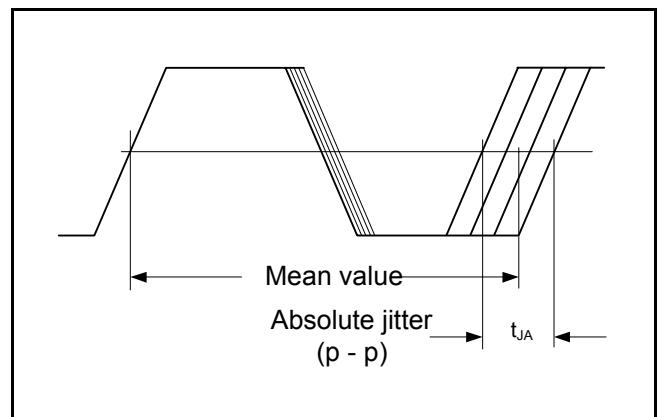
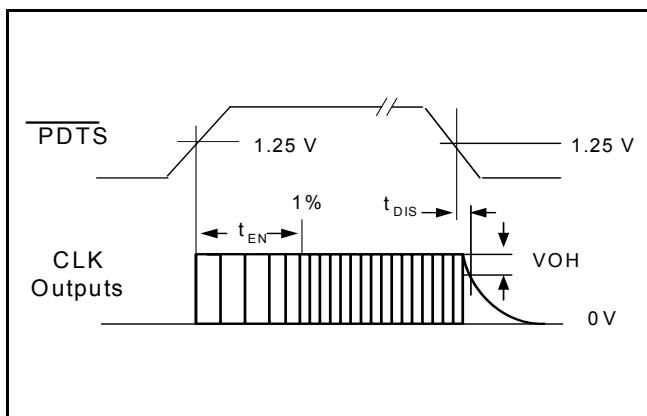
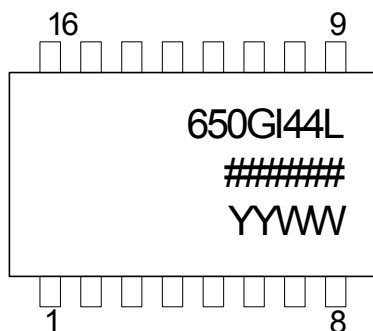


Figure 6: Short Term Jitter Definition

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		70		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		68		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			37		$^{\circ}\text{C/W}$

Marking Diagram (Pb free)

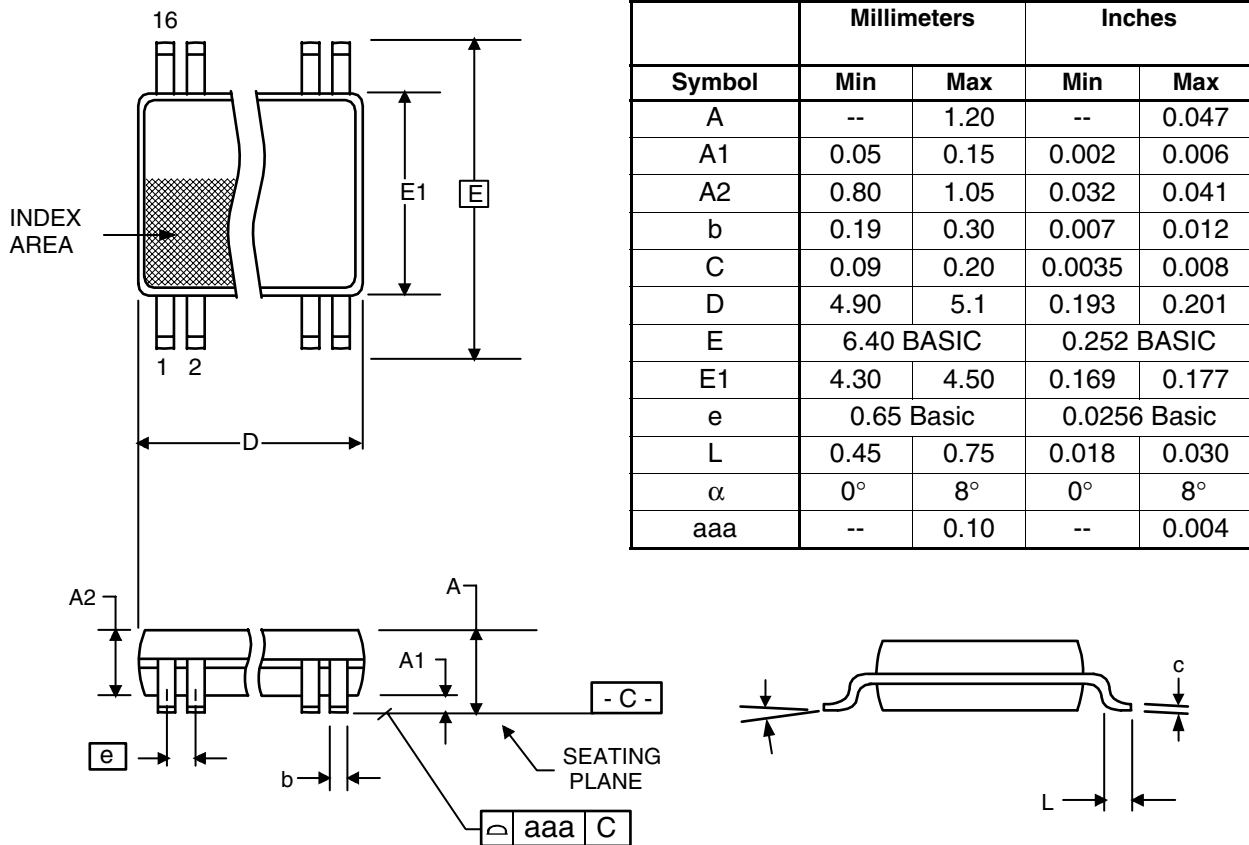


Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. "I" designates industrial temperature range.
4. "L" designates Pb (lead) free package.
5. Bottom marking: (origin)
Origin = country of origin of not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650GI-44LF	see page 7	Tubes	16-pin TSSOP	-40 to +85° C
650GI-44LFT		Tape and Reel	16-pin TSSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

Rev.	Originator	Date	Description of Change
-	P. Griffith	05/13/05	New proposal.
A	P. Griffith	05/24/05	Move from Advance (proposal) to Preliminary. Added ICS part number and LF.
B	P. Griffith	06/14/05	Added "Output-to-Output skew" psec of ± 180 ps.
C	P. Griffith	08/03/05	Removed references to SS_EN.
D		10/27/09	Added EOL note for non-green parts
E		05/13/10	Removed EOL note and non-green parts

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.