



# ICS671-15

## ZERO DELAY, LOW SKEW BUFFER

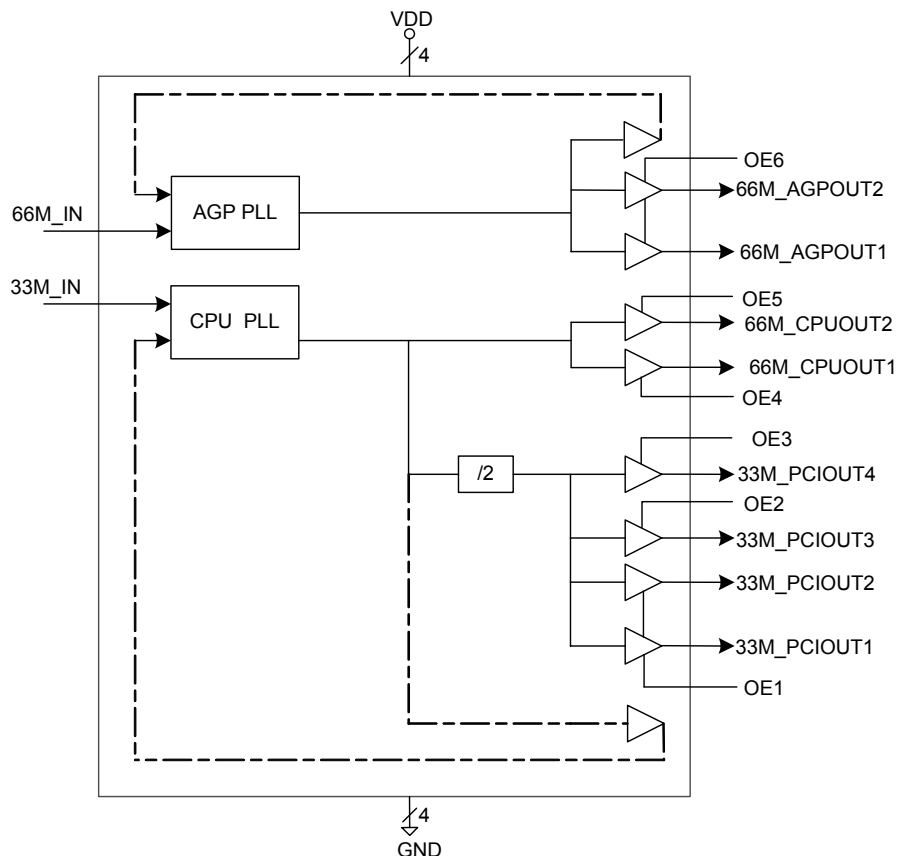
### Description

The ICS671-15 is a low-jitter, low-skew, high-performance zero delay buffer (ZDB) for high-speed applications. The device is designed using ICS' proprietary low-jitter PLL (Phase-Locked Loop) techniques. The ICS671-15 includes a ZDB bank of four outputs running at 33 MHz, and two outputs at 66 MHz from the CPU PLL. This device also provides two 66 MHz zero delay clocks derived from the AGP PLL. In the zero delay mode, the rising edge of the input clock is aligned with the rising edges of the feedback clock. The ICS671-15 provides feedback clocks internally for the CPU PLL and the AGP PLL, and with the lowest jitter.

### Features

- Packaged in 24-pin TSSOP
- Input-output delay ( $\pm 300$  ps)
- Two ZDB 66 MHz outputs from a 66 MHz input AGP clock
- Two ZDB 66 MHz outputs, plus four 33 MHz outputs from a 33 MHz input CPU clock
- Output-to-output skew is less than 250 ps
- Full CMOS outputs with 18 mA output drive capability at TTL levels (at 3.3 V)
- Spread Smart™ technology works with spread spectrum clock generators
- Advanced, low-power, sub-micron CMOS process
- Operating voltage of 3.3 V
- Separate hardware output enable pins: OE1, OE2, OE3, OE4, OE5 and OE6

### Block Diagram





## Pin Assignment

33M_IN	<input type="checkbox"/>	1	24	<input type="checkbox"/>	66M_IN
VDD	<input type="checkbox"/>	2	23	<input type="checkbox"/>	OE6
OE5	<input type="checkbox"/>	3	22	<input type="checkbox"/>	VDD
GND	<input type="checkbox"/>	4	21	<input type="checkbox"/>	66M_AGPOUT2
66M_CPUOUT1	<input type="checkbox"/>	5	20	<input type="checkbox"/>	66M_AGPOUT1
66M_CPUOUT2	<input type="checkbox"/>	6	19	<input type="checkbox"/>	GND
VDD	<input type="checkbox"/>	7	18	<input type="checkbox"/>	GND
VDD	<input type="checkbox"/>	8	17	<input type="checkbox"/>	OE4
OE3	<input type="checkbox"/>	9	16	<input type="checkbox"/>	OE1
33M_PCIOUT4	<input type="checkbox"/>	10	15	<input type="checkbox"/>	GND
33M_PCIOUT3	<input type="checkbox"/>	11	14	<input type="checkbox"/>	33M_PCIOUT1
OE2	<input type="checkbox"/>	12	13	<input type="checkbox"/>	33M_PCIOUT2

24-pin (173 mil) TSSOP

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## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	33M_IN	Input	Connect this pin to a 33 MHz input clock.
2	VDD	Power	Connect to +3.3 V.
3	OE5	Input	Output Enable control pin for outputs 66M_CPUOUT2. This pin is active high and tri-states the outputs when low.
4	GND	Power	Connect to ground.
5	66M_CPUOUT1	Output	66 MHz output clock.
6	66M_CPUOUT2	Output	66 MHz output clock.
7	VDD	Power	Connect to +3.3 V.
8	VDD	Power	Connect to +3.3 V.
9	OE3	Input	Output Enable control pin for output 33M_PCIOUT4. This pin is active high and tri-states the outputs when low.
10	33M_PCIOUT4	Output	33 MHz output clock.
11	33M_PCIOUT3	Output	33 MHz output clock.
12	OE2	Input	Output Enable control pin for output 33M_PCIOUT3. This pin is active high and tri-states the outputs when low.
13	33M_PCIOUT2	Output	33 MHz output clock.



Pin Number	Pin Name	Pin Type	Pin Description
14	33M_PCIOUT1	Output	33 MHz output clock.
15	GND	Power	Connect to ground.
16	OE1	Input	Output Enable control pin for output 33M_PCIOUT1 and 33M_PCIOUT2. This pin is active high and tri-states the outputs when low.
17	OE4	Input	Output Enable control pin for outputs 66M_CPUOUT1. This pin is active high and tri-states the outputs when low.
18	GND	Power	Connect to ground.
19	GND	Power	Connect to ground.
20	66M_AGPOUT1	Output	66 MHz output clock.
21	66M_AGPOUT2	Output	66 MHz output clock.
22	VDD	Power	Connect to +3.3 V.
23	OE6	Input	Output Enable control pin for outputs 66M_AGPOUT1 and 66M_AGPOUT2. This pin is active high and tri-states the outputs when low.
24	66M_IN	Input	Connect this pin to a 66 MHz input clock.

## External Components

The ICS671-15 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1  $\mu$ F should be connected between VDD and GND, as close to the part as possible. A 33  $\Omega$  series terminating resistor should be used on each clock output to reduce reflections.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS671-15. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C



## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.135	3.3	+3.465	V

## DC Electrical Characteristics

VDD=3.3 V ±5%, Ambient temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Input High Voltage	V <sub>IH</sub>	66M, 33M, OE1:OE6	2.0			V
Input Low Voltage	V <sub>IL</sub>	66M, 33M OE1:OE6			0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA			0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	VDD-0.4			V
Operating Supply Current 66M, 33M Input	I <sub>DD</sub>	No Load. both inputs active		32		mA
Short Circuit Current	I <sub>OS</sub>	Each output		±50		mA
Input Capacitance	C <sub>IN</sub>			5		pF

## AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, CL=15 pF (Total)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F <sub>IN</sub>		33		66	MHz
Output Frequency	F <sub>OUT</sub>		33		66	MHz
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0 V			1.5	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		at VDD/2	45	50	55	%
Device-to-Device Skew		Rising edges at VDD/2 for similar outputs, Note 1		500	700	ps
Output-to-Output Skew	t <sub>S</sub>	Rising edges at VDD/2 66M AGP outputs, Note 1		250	500	ps



Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output-to-Output Skew	$t_S$	Rising edges at VDD/2 66M CPU outputs, Note 1		250	500	ps
Output-to-Output Skew	$t_S$	Rising edges at VDD/2 33M PCI outputs, Note 1		300	500	ps
Skew from output of 66M CPU to 33M PCI, equally loaded	$t_S$	Rising edges at VDD/2 33M PCI outputs		300	500	ps
Short-term Jitter	$t_{JA}$	peak-to-peak		300		ps
Input-to-Output Delay	$t_D$	measured at VDD/2	-500		+500	ps
PLL Lock Time	$t_{LOCK}$	Stable power supply, valid clocks on 66M and 33M			1	ms
Output Enable Time (for OE1 to E6)		OE going from low to high with stable output			1.0	ns
Output Disable Time (for OE1 to E6)		OE going high to low tri-state output			1.0	ns

Note 1: All outputs are equally loaded.

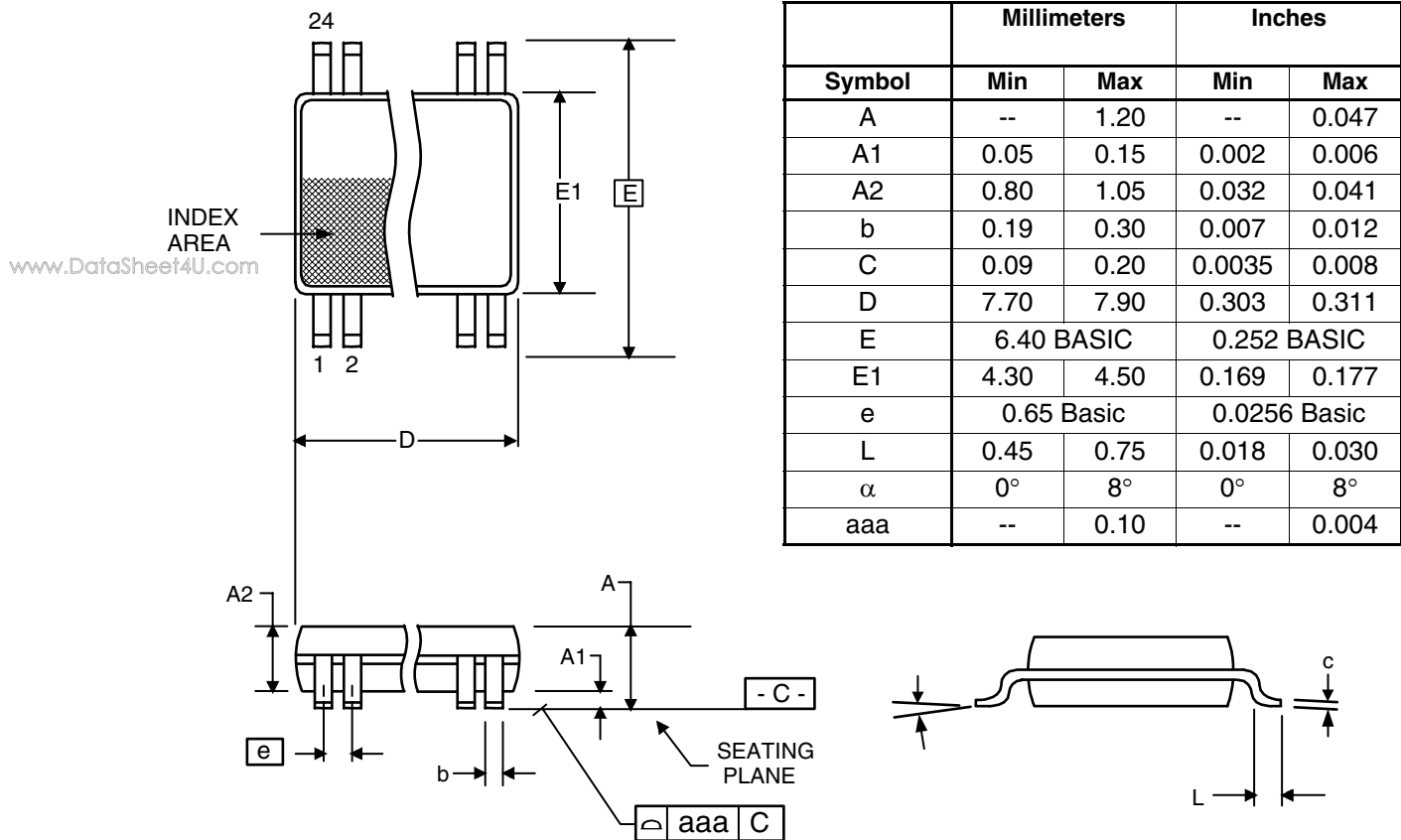
## Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		77		°C/W
	$\theta_{JA}$	1 m/s air flow		68		°C/W
	$\theta_{JA}$	2 m/s air flow		66		°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$			25		°C/W



### Package Outline and Package Dimensions (24-pin TSSOP, 4.4mm Body)

Package dimensions are kept current with JEDEC Publication No. 95



### Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS671G-15	ICS671G-15	Tubes	24-pin TSSOP	0 to 70° C
ICS671G-15T	ICS671G-15	Tape and Reel	24-pin TSSOP	0 to 70° C

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