

Description

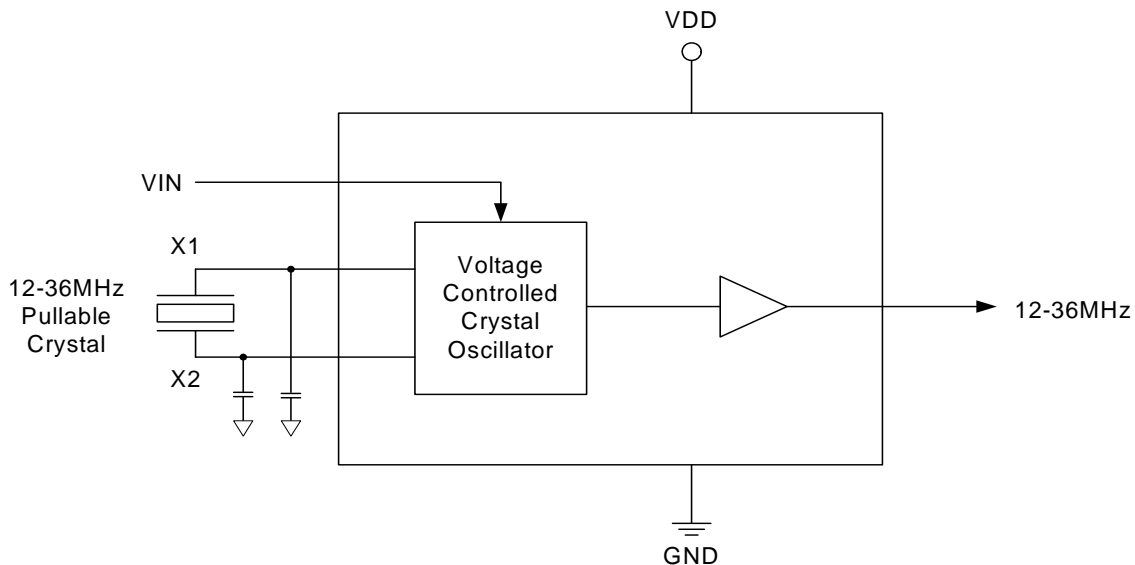
Used in conjunction with an external pullable quartz crystal, this monolithic integrated circuit replaces more costly hybrid (canned) VCXO devices. The ICS726A is designed primarily for data and clock recovery applications such as ADSL modems, set-top box receivers, and telecom systems.

The frequency of the on-chip VCXO is adjusted by an external control voltage to the VIN pin. Since VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3.3 V.

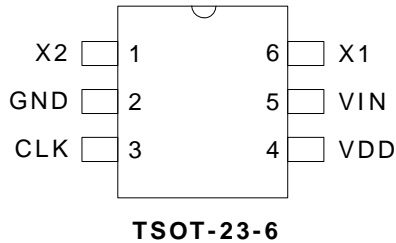
Features

- Uses an inexpensive 12 to 36 MHz external crystal
- Output frequency range of 12 to 36 MHz
- On-chip VCXO with guaranteed pull range of ± 115 ppm minimum
- VCXO tuning voltage 0 to 3.3 V
- Packaged in 6-pin TSOT
- Pb (lead) free package

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Input	Crystal connection. Connect to the external pullable crystal.
2	GND	Power	Connect to ground.
3	CLK	Output	VCXO CMOS level clock output at the frequency of the crystal.
4	VDD	Power	Connect to +3.3 V (0.01µF decoupling capacitor recommended).
5	VIN	Input	Voltage input to VCXO — 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
6	X1	Input	Crystal connection. Connect to the external pullable crystal.

External Component Selection

The ICS726A requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 4) and GND (pin 2), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 3) and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Quartz Crystal

The ICS726A VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and

reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS726A incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS726A is designed to have zero frequency error when the total of on-chip + stray capacitance is 8.9 pF.

Required Crystal Parameters:

Nominal Frequency	as required MHz
Initial Accuracy at 25° C	-20 min/+20 max ppm
Temperature Stability	-30 min/+30 max ppm
Aging, 1st year	-5 min/+5 max ppm
Aging, 10 years	-20 min/+20 max ppm
Operating Temp. Range, °C	0 min/+25 typ/+70 max or
Operating Temp. Range, °C	-40 min/+25 typ/+85 max
Load Capacitance	8.6 pF
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	270 Max
Equivalent Series Resistance	35 Ω Max

The third overtone mode of the crystal and all spurs must be >100 ppm distant from the 3x fundamental resonance measured with a physical load of 8.6pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS726A. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. See application note MAN05.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the value of the crystal capacitors:

1. Connect VDD of the ICS726A to 3.3 V. Connect pin 5 of the ICS726A to the second power supply. Adjust the voltage on pin 5 to 0V. Measure and record the frequency of the CLK output. (f_{0V})
2. Adjust the voltage on pin 5 to 3.3 V. Measure and record the frequency of the same output. (f_{high})

To calculate the centering error:

Centering error

$$= 10^6 \cdot \frac{(f_{high} - f_{target}) + (f_{0V} - f_{target})}{2 \times f_{target}} - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ = actual initial accuracy (in ppm) of the crystal being measured.

If the centering error is less than ± 25 ppm, no adjustment is needed. If the centering error is more than 25 ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact IDT for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground.

The value for each of these caps (in pF) is given by:

$$= 2 \times (\text{centering error}) / (\text{trim sensitivity})$$

Trim sensitivity is a parameter which can be supplied by your crystal vendor or calculated using the following formula:

$$\text{trim sensitivity} = \frac{10^6 \times C_1}{2 \times (C_0 + C_L)^2}$$

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS726A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD = 3.3 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	Output = 12 MHz, no load		5		mA
Short Circuit Current	I _{OS}			±50		mA
VIN, VCXO Control Voltage	V _{IA}		0		3.3	V

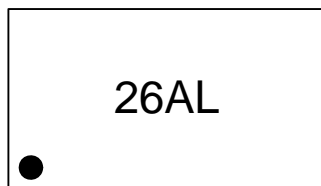
AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_O		12		36	MHz
Crystal Pullability, Note 2	F_P	$0V \leq V_{IN} \leq 3.3 V$, Note 1	±115			ppm
VCXO Gain		$V_{IN} = V_{DD}/2 \pm 1 V$, Note 1		140		ppm/V
Output Rise Time	t_{OR}	0.8 to 2.0 V, $C_L=15 pF$		0.8	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, $C_L=15 pF$		0.8	1.5	ns
Output Clock Duty Cycle	t_D	Measured at 1.4 V, $C_L=15 pF$	40	50	60	%
Maximum Output Jitter, short term	t_j	$C_L=15 pF$		100		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

Marking Diagram

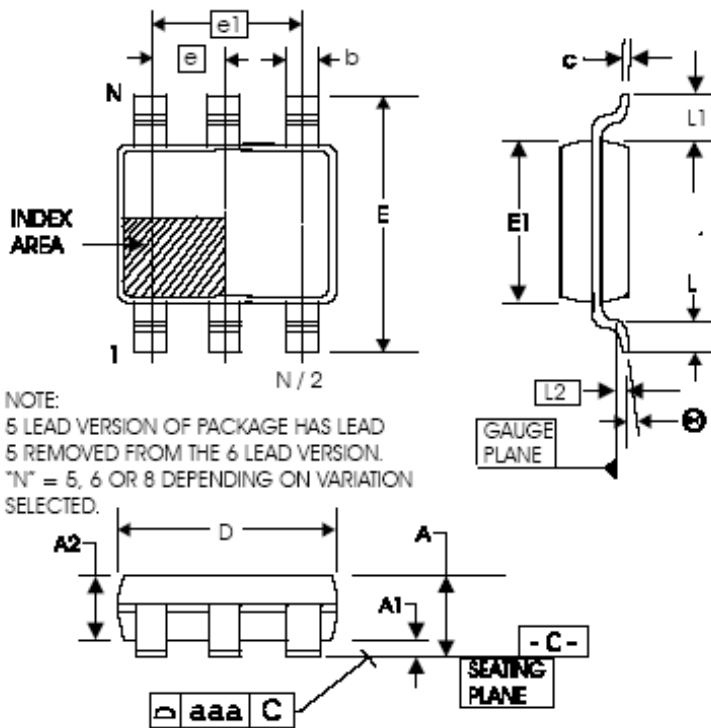


Notes:

1. '26AL' denotes part number.
2. "L" denotes Pb (lead) free package.
3. Bottom marking: '####' denotes last 4 digits of lot number

Package Outline and Package Dimensions (6-pin TSOT)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters	
	Min	Max
A	—	1.00
A1	0.01	0.10
A2	0.84	0.90
b	0.30	0.45
c	0.12	0.20
D	2.90 BASIC	
E	2.80 BASIC	
E1	1.60 BASIC	
e	0.95 BASIC	
e1	1.90 BASIC	
L	0.30	0.50
L1	0.60 REF.	
L2	0.25 BASIC	
θ	0°	8°
aaa	—	0.10

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
726ATLFT	26AL	Tape and Reel	6-pin TSOT	0 to +70° C

"A" denotes revision designator (will not correlate with datasheet revision)

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

ICS726A
12 TO 36 MHZ 6TSOT VCXO

VCXO

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.