Integrated
Circuit
Systems, Inc.

ICS8312I

LOW SKEW, 1-TO-12 LVCMOS / LVTTL FANOUT BUFFER

GENERAL DESCRIPTION

HiPerClockS™

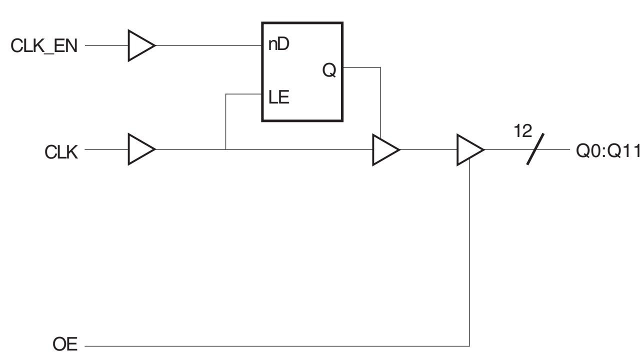
The ICS8312I is a low skew, 1-to-12 LVCMOS / LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8312I single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS8312I is characterized at full 3.3V, 2.5V, and 1.8V, or mixed 3.3V core/2.5V, 3.3V core/1.8V and 2.5V core/1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS8312I ideal for high performance, single ended applications that also require a limited output voltage.

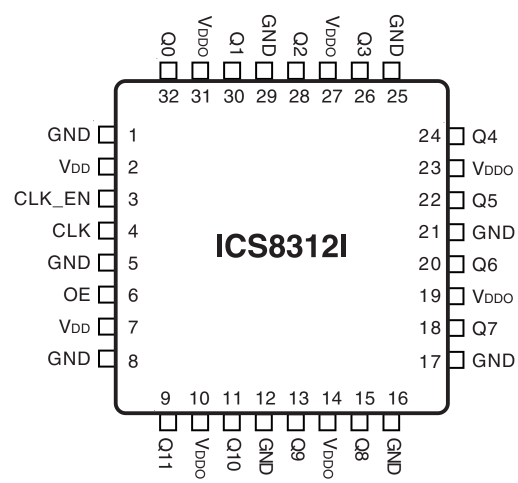
FEATURES

- 12 LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- Maximum output frequency: 250MHz
- Output skew: 160ps (maximum)
- Operating supply modes: Core/Output
  3.3V/3.3V
  2.5V/2.5V
  1.8V/1.8V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Pacakge
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Power supply ground.
2, 7	V_{DD}	Power		Core supply pins.
3	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
6	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q11. LVCMOS / LVTTL interface levels.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Q0 thru Q11 outputs. LVCMOS / LVTTL interface levels.
10, 14, 19, 23, 27, 31	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V			19	pF
		V_{DDO} = 2.625V			18	pF
		V_{DDO} = 2V			16	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		7		Ω
		V_{DDO} = 2.5V ± 5%		7		Ω
		V_{DDO} = 1.8V ± 0.2V		10		Ω

TABLE 3A. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Output
OE	**CLK_EN**	**Q0:Q11**
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs
OE	**CLK_EN**	**CLK**	**Q0:Q11**
1	1	0	LOW
1	1	1	HIGH

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4F. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	µA
I_{DDO}	Output Supply Current				10	µA

TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
			V_{DD} = 1.8V ± 0.2V	0.65*V_{DD}		V_{DD} + 0.3	V
		CLK_EN, OE	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
			V_{DD} = 1.8V ± 0.2V	0.65*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK	V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
			V_{DD} = 1.8V ± 0.2V	-0.3		0.35*V_{DD}	V
		CLK_EN, OE	V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
			V_{DD} = 1.8V ± 0.2V	-0.3		0.35*V_{DD}	V
I_{IH}	Input High Current	CLK	V_{DD} = 3.3V ± 5%			150	µA
			V_{DD} = 2.5V ± 5%			150	µA
			V_{DD} = 1.8V ± 0.2V			150	µA
		CLK_EN, OE	V_{DD} = 3.3V ± 5%			5	µA
			V_{DD} = 2.5V ± 5%			5	µA
			V_{DD} = 1.8V ± 0.2V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.3V ± 5%	-5			µA
			V_{DD} = 2.5V ± 5%	-5			µA
			V_{DD} = 1.8V ± 0.2V	-5			µA
		CLK_EN, OE	V_{DD} = 3.3V ± 5%	-150			µA
			V_{DD} = 2.5V ± 5%	-150			µA
			V_{DD} = 1.8V ± 0.2V	-150			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -1mA	2			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; I_{OH} = -100uA	V_{DD} - 0.2			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 1mA			0.4	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 0.2V; I_{OL} = 100uA			0.2	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 250MHz	1.2	2.0	2.7	ns
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				850	ps
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	175		800	ps
odc	Output Duty Cycle	f ≤ 150MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
See Table 5C listed below for Notes 1 through 5.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 250MHz	1.25	2.4	3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 5				155	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.1	ns
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 150MHz	45		55	%

All parameters measured at fMAX unless noted otherwise.
See Table 5C listed below for Notes 1 through

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 200MHz	1.6	3.3	4.9	ns
*t*sk(o)	Output Skew; NOTE 2, 5				160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				2.4	ns
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	175		875	ps
odc	Output Duty Cycle	f ≤ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5D. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 250MHz	1.5	2.1	2.8	ns
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1	ns
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 150MHz	45		55	%

All parameters measured at fMAX unless noted otherwise.
See Table 5F listed below for Notes 1 through 5.

TABLE 5E. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 200MHz	1.5	2.5	3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.4	ns
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 100MHz	45		55	%

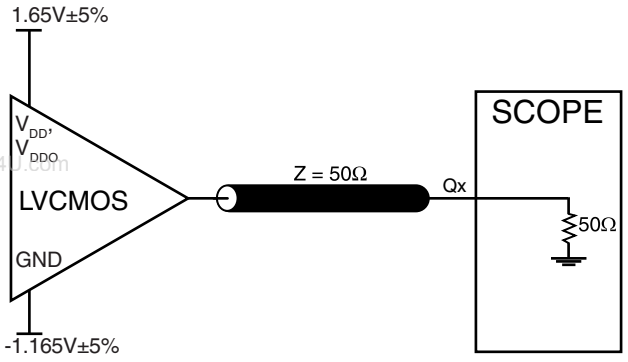
All parameters measured at fMAX unless noted otherwise.
See Table 5F listed below for Notes 1 through

TABLE 5F. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

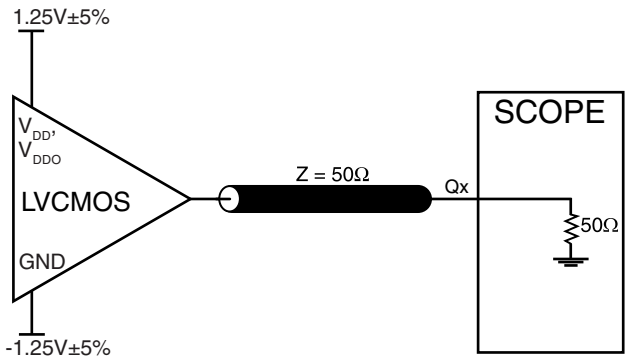
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 200MHz	1.4	2.7	3.9	ns
*t*sk(o)	Output Skew; NOTE 2, 5				160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.6	ns
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

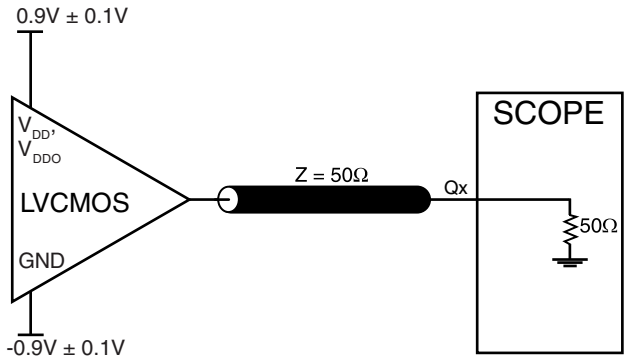
PARAMETER MEASUREMENT INFORMATION



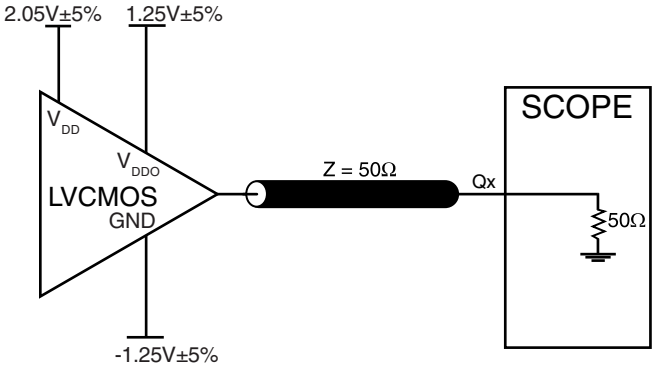
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



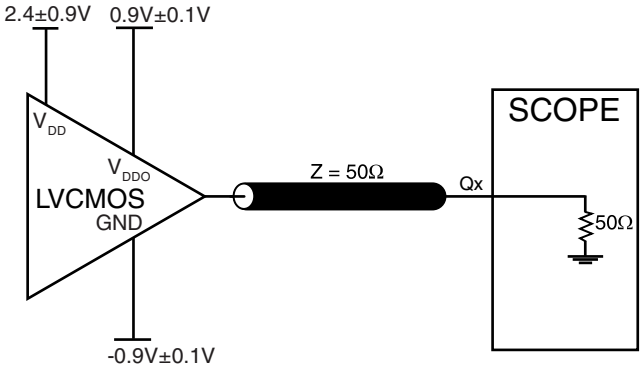
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



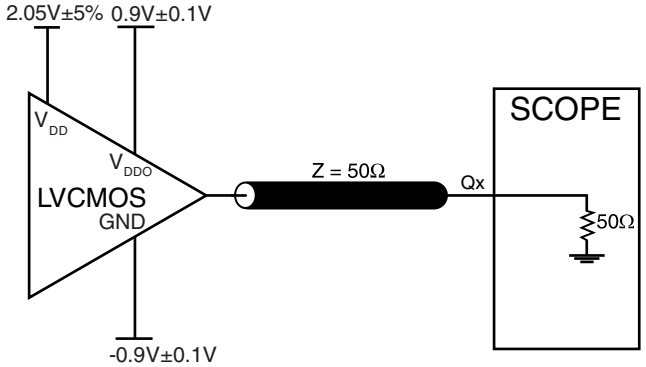
1.8V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



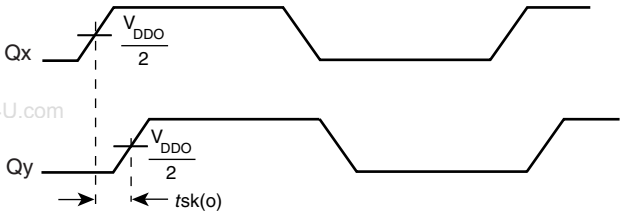
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



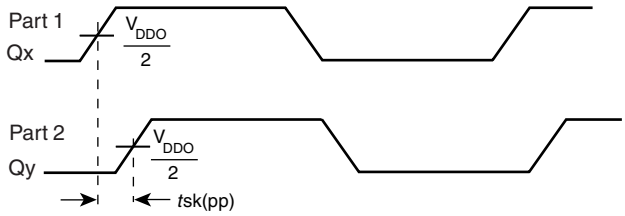
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



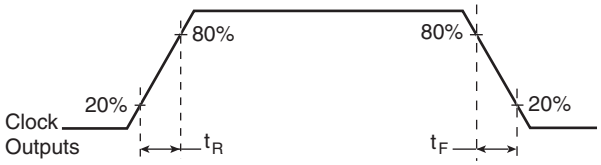
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



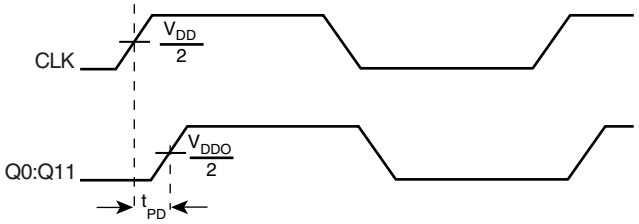
OUTPUT SKEW



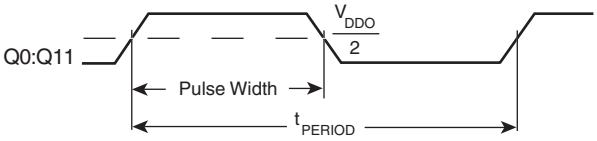
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8312I is: 339

PACKAGE OUTLINE - Y SUFFIX

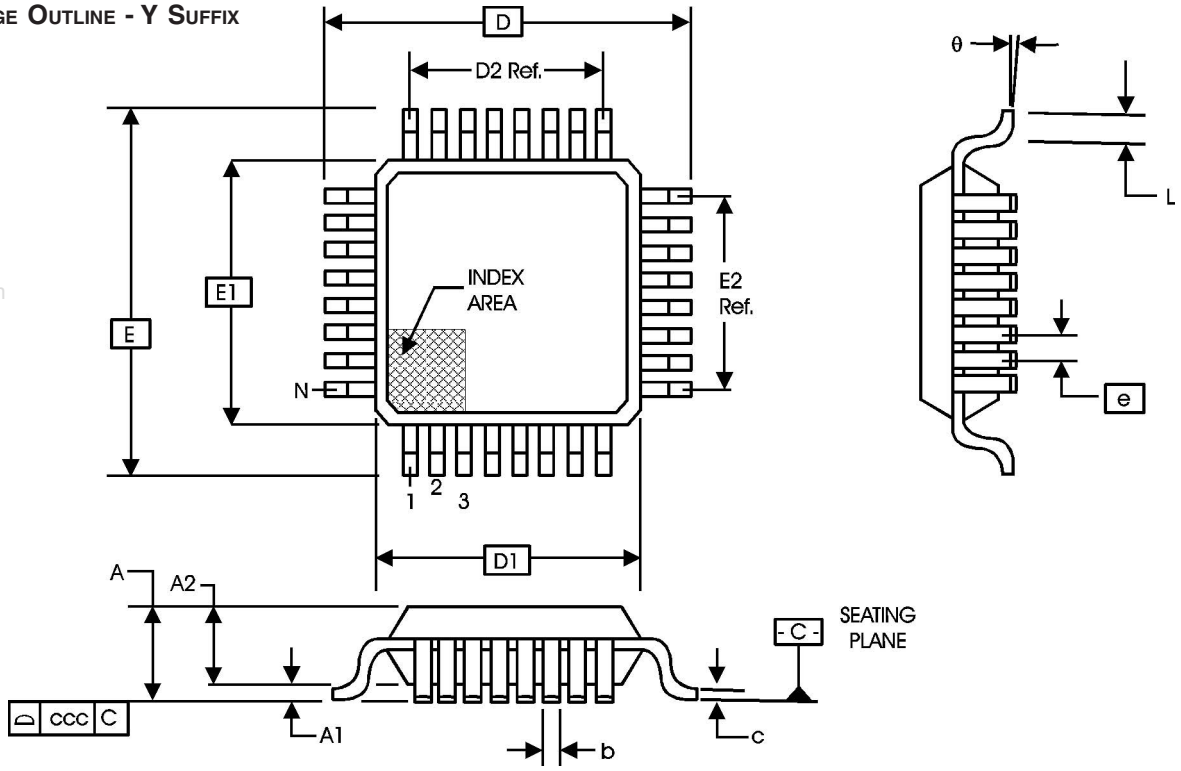


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8312AYI	ICS8312AYI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS8312AYIT	ICS8312AYI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C