PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS8316
LOW SKEW, 1-TO-16, LVCMOS / LVTTL FANOUT BUFFER W/1.2V LVCMOS OUTPUTS

GENERAL DESCRIPTION

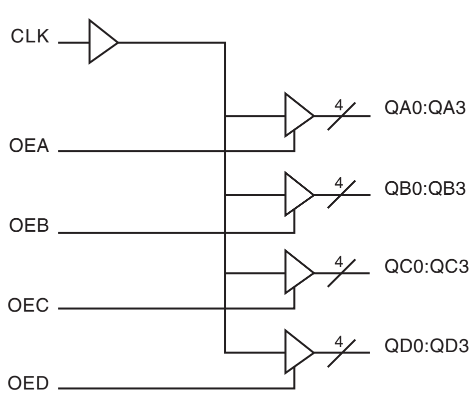
The ICS8316 is a low skew, 1-to-16 LVCMOS/ LVTTL Fanout Buffer with 1.2V LVCMOS Outputs and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8316 single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines.

Guaranteed output and part-to-part skew characteristics along with the 1.2V output makes the ICS8316 ideal for high performance, single ended applications that also require a limited output voltage.

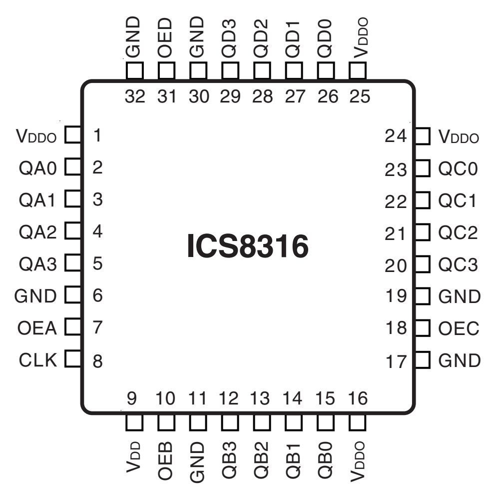
FEATURES

- Sixteen 1.2V LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- Maximum output frequency: 150MHz
- Output skew: TBD
- Propagation delay: 3.5ns (typical)
- 3.3V core/1.2V output operating supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead VFQFN
5mm x 5mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 16, 24, 25	V_{DDO}	Power		Output supply pins.
2, 3, 4, 5	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. LVCMOS / LVTTL interface levels.
6, 11, 17, 19, 30, 32	GND	Power		Power supply ground.
7	OEA	Input	Pullup	Bank A output enable pin. Controls enabling and disabling of QA0:QA3 outputs. LVCMOS / LVTTL interface levels.
8	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
9	V_{DD}	Power		Core supply pin.
10	OEB	Input	Pullup	Bank B output enable pin. Controls enabling and disabling of QB0:QB3 outputs. LVCMOS / LVTTL interface levels.
12, 13, 14, 15	QB3, QB2, QB1, QB0	Output		Bank B clock outputs. LVCMOS / LVTTL interface levels.
18	OEC	Input	Pullup	Bank C output enable pin. Controls enabling and disabling of QC0:QC3 outputs. LVCMOS / LVTTL interface levels.
20, 21, 22, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. LVCMOS / LVTTL interface levels.
26, 27, 28, 29	QD0, QD1, QD2, QD3	Output		Bank D clock outputs. LVCMOS / LVTTL interface levels.
31	OED	Input	Pullup	Bank D output enable pin. Controls enabling and disabling of QD0:QD3 outputs. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 1.26V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 1.2 ± 5%		15		Ω

TABLE 3A. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs	Outputs
OE[A:D]	**Qx0:Qx3**
0	Hi-Z
1	Active

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs
OE[A:D]	**CLK**	**Qx0:Qx3**
1	0	LOW
1	1	HIGH

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	34.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V, V_{DDO} = 1.2V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4B. LVCMOS DC CHARACTERISTICS, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
		OEA:OED	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OEA:OED	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		V_{DDO} = 1.2V ± 5%; NOTE 1	V_{DD}*0.7			V
V_{OL}	Output Low Voltage		V_{DDO} = 1.2V ± 5%; NOTE 1			V_{DD}*0.3	V

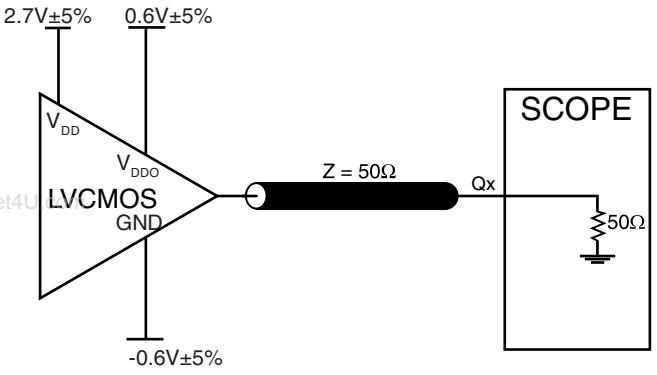
NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagram.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.2V±5%, T_A = 0°C TO 70°C

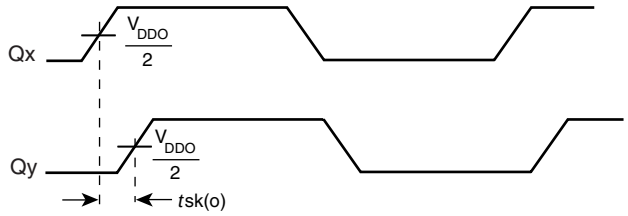
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				150	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1			3.5		ns
*t*sk(o)	Output Skew; NOTE 2, 5			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			TBD		ps
t_R/t_F	Output Rise Time; NOTE 4	20% to 80%		650		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

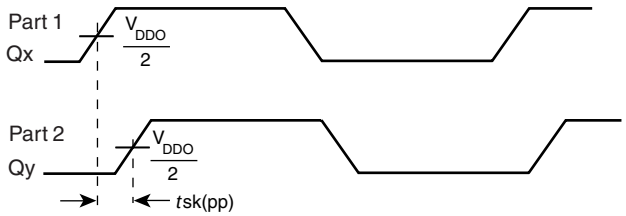
PARAMETER MEASUREMENT INFORMATION



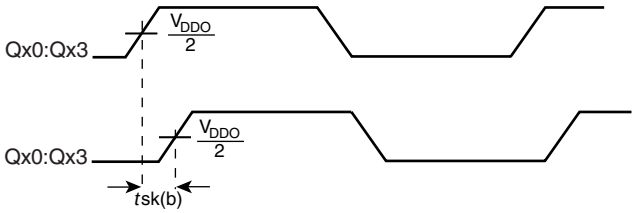
3.3V CORE/1.2V OUTPUT LOAD AC TEST CIRCUIT



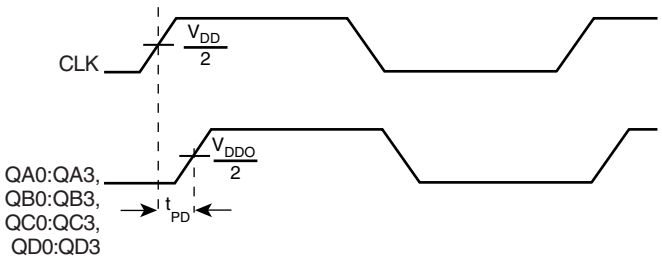
OUTPUT SKEW



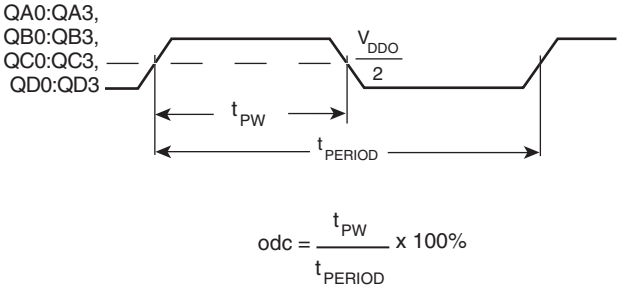
PART-TO-PART SKEW



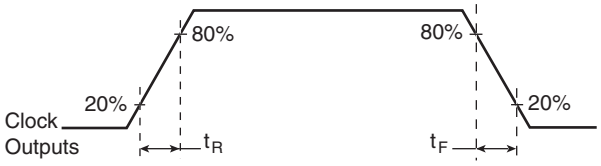
BANK SKEW (where x denotes outputs in the same bank)



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PLUSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

TRANSISTOR COUNT

The transistor count for ICS8316 is: 416

PACKAGE OUTLINE AND DIMENSIONS - K SUFFIX FOR 32 LEAD VFQFN

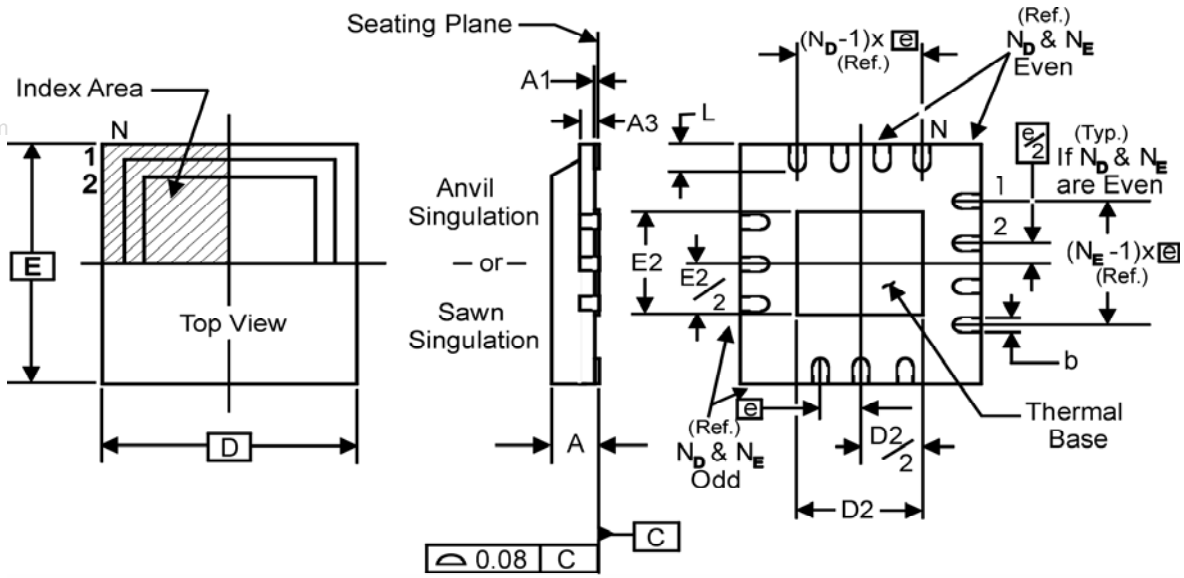


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8316AK	ICS8316AK	32 Lead VFQFN	tray	0°C to 70°C
ICS8316AKT	ICS8316AK	32 Lead VFQFN	2500 tape & reel	0°C to 70°C
ICS8316AKLF	TBD	32 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS8316AKLFT	TBD	32 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.