



GENERAL DESCRIPTION



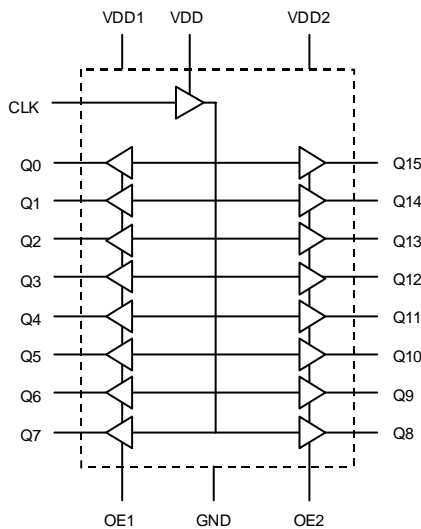
The ICS8343 is a low skew, 1-to-16 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8343 is at 3.3V, 2.5V and mixed 3.3V input and 2.5V supply modes over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the ICS8343 ideal for those clock distribution applications demanding well defined performance and repeatability.

www.DataSheet

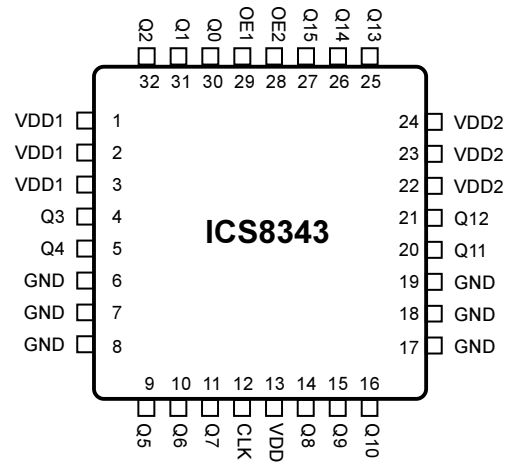
FEATURES

- 16 LVCMOS outputs
- Output frequency up to 200MHz
- 250ps output skew
- 700ps part to part
- CMOS compatible clock input at 5V, LVTTTL and LVCMOS compatible at 3.3V and 2.5V
- LVTTTL output enable inputs
- Dual output enable inputs facilitates 1-to-16 or 1-to-8 input to output modes
- 3.3V, 2.5V or mixed 3.3V, 2.5V from 0°C to 70°C ambient operating temperature
- 32 lead low-profile QFP(LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch

BLOCK DIAGRAM



PIN ASSIGNMENT



**32-Lead LQFP
(Top View)**



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 3	VDD1	Power		Output Q0 thru Q7 power supply. Connect to 5V, 3.3V or 2.5V.
4, 5	Q3, Q4	Output		Clock outputs. 14Ω typical output impedance.
6, 7, 8	GND	Power		Connect to ground.
9, 10, 11	Q5, Q6, Q7	Output		Clock outputs. 14Ω typical output impedance.
12	CLK	Input		Clock input.
13	VDD	Power		Input power supply. Connect to 5V, 3.3V or 2.5V
14, 15, 16	Q8, Q9, Q10	Output		Clock outputs. 14Ω typical output impedance.
17, 18, 19	GND	Power		Connect to ground.
20, 21	Q11, Q12	Output		Clock outputs. 14Ω typical output impedance.
22, 23, 24	VDD2	Power		Output Q8 thru Q15 power supply. Connect to 5V, 3.3V or 2.5V.
25, 26, 27	Q13, Q14, Q15	Output		Clock outputs. 14Ω typical output impedance.
28	OE2	Input	Pullup	Output enable. When low forces outputs Q8 thru Q15 to HiZ state.
29	OE1	Input	Pullup	Output enable. When low forces outputs Q0 thru Q7 to HiZ state.
30, 31, 32	Q0, Q1, Q2	Output		Clock outputs. 14Ω typical output impedance.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance					pF
CPD	Power Dissipation Capacitance (per output)	VDD1, VDD2 = 5.25V		15		pF
		VDD1, VDD2 = 3.47V		11		pF
		VDD1, VDD2 = 2.63V		9.5		pF

TABLE 3. FUNCTION TABLE

Inputs		Outputs	
OE1	OE2	Q0 thru Q7	Q8 thru Q15
0	0	Hi Z	Hi Z
1	0	Active	Hi Z
0	1	Hi Z	Active
1	1	Active	Active



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

www.DataSheet4U.com

TABLE 4A. DC ELECTRICAL CHARACTERISTICS, VDD = VDD1 = VDD2 = 3.3V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD, VDD1, VDD2	Operating Supply Voltage		3.135	3.3	3.465	V
VIH	Input High Voltage	CLK	VDD = 3.465V	2	VDD + 0.3	V
		OEx	VDD = 3.465V	2	VDD + 0.3	V
VIL	Input Low Voltage	CLK	VDD = 3.135V	-0.3	0.8	V
		OEx	VDD = 3.135V	-0.3	0.8	V
IIH	Input High Current	CLK	VIN = VDD		1	µA
		OEx	VIN = VDD		1	µA
IIL	Input Low Current	CLK	VIN = 0V	-15		µA
		OEx	VIN = 0V	-15		µA
IDD	Input Operating Supply Current				100	µA
VOH	Output High Voltage	VDD = 3.135V, IOH = -25mA	2.4			V
VOL	Output Low Voltage	VDD = 3.135V, IOL = 25mA			0.8	V
IOZH	High Impedance Leakage Current	OEx = 0V, VOUT = VDD			1	µA
IOZL	High Impedance Leakage Current	OEx = 0V, VOUT = 0V	-1			µA

TABLE 5A. AC ELECTRICAL CHARACTERISTICS, VDD = VDD1 = VDD2 = 3.3V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				200	MHz
tpLH	Propagation Delay, Low-to-High	0 < f ≤ 200MHz	1.1	2.1	3.1	ns
tpHL	Propagation Delay, High-to-Low	0 < f ≤ 200MHz	1.2	2.0	2.7	ns
tsk(o)	Output Skew; NOTE 3	Measured on rising edge @VDDx/2			250	ps
tsk(p)	Process Skew; NOTE 4	Measured on rising edge @VDDx/2			450	ps
tsk(pp)	Part-to-Part Skew; NOTE 5	Measured on rising edge @VDDx/2			700	ps
tR	Output Rise Time			0.5	0.8	ns
tF	Output Fall Time			0.9	1.7	ns
tPW	Output Pulse Width		tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to VDDx/2.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at the same output on different devices operating at the same supply voltages and with equal load conditions.

NOTE 5: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



TABLE 4B. DC ELECTRICAL CHARACTERISTICS, VDD = 3.3V±5%, VDD1 = VDD2 = 2.5V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Input Operating Supply Voltage		3.135	3.3	3.465	V
VDD1, VDD2	Output Operating Supply Voltage		2.375	2.5	2.625	
VIH	Input High Voltage	CLK	VDD = 3.465	2	VDD + 0.3	V
		OEx	VDD = 3.465	2	VDD + 0.3	V
VIL	Input Low Voltage	CLK	VDD = 3.135	-0.3	0.8	V
		OEx	VDD = 3.135	-0.3	0.8	V
IIH	Input High Current	CLK	VIN = VDD		1	μA
		OEx	VIN = VDD		1	μA
IIL	Input Low Current	CLK	VIN = 0V	-15		μA
		OEx	VIN = 0V	-15		μA
IDD	Input Operating Supply Current				100	μA
VOH	Output High Voltage	VDD = 2.375V, IOH = -25mA	1.5			V
VOL	Output Low Voltage	VDD = 2.375V, IOL = 25mA			0.8	V
IOZH	High Impedance Leakage Current	OEx = 0V, VOUT = VDD			1	μA
IOZL	High Impedance Leakage Current	OEx = 0V, VOUT = 0V	-1			μA

TABLE 5B. AC ELECTRICAL CHARACTERISTICS, VDD = 3.3V±5%, VDD1 = VDD2 = 2.5V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				200	MHz
tpLH	Propagation Delay, Low-to-High	0 < f ≤ 200MHz	1.0	2.3	3.2	ns
tpHL	Propagation Delay, High-to-Low	0 < f ≤ 200MHz	1.4	2.3	3.2	ns
tsk(o)	Output Skew; NOTE 3	Measured on rising edge @VDDx/2			250	ps
tsk(p)	Process Skew; NOTE 4	Measured on rising edge @VDDx/2			450	ps
tsk(pp)	Part-to-Part Skew; NOTE 5	Measured on rising edge @VDDx/2			700	ps
tR	Output Rise Time			0.5	0.8	ns
tF	Output Fall Time			0.9	1.7	ns
tPW	Output Pulse Width		tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to VDDx/2.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at the same output on different devices operating at the same supply voltages and with equal load conditions.

NOTE 5: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



TABLE 4C. DC ELECTRICAL CHARACTERISTICS, VDD = VDD1 = VDD2 = 2.5V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD, VDD1, VDD2	Operating Supply Voltage		2.375	2.5	2.625	V
VIH	Input High Voltage	CLK	VDD = 2.625	2	VDD + 0.3	V
		OEx	VDD = 2.625	2	VDD + 0.3	V
VIL	Input Low Voltage	CLK	VDD = 2.375	-0.3	0.7	V
		OEx	VDD = 2.375	-0.3	0.8	V
IIH	Input High Current	CLK	VIN = VDD		1	μA
		OEx	VIN = VDD		1	μA
IIL	Input Low Current	CLK	VIN = 0V	-10		μA
		OEx	VIN = 0V	-10		μA
IDD	Input Operating Supply Current				100	μA
VOH	Output High Voltage	VDD = 2.375V, IOH = -25mA	1.5			V
VOL	Output Low Voltage	VDD = 2.375V, IOL = 25mA			0.8	V
IOZH	High Impedance Leakage Current	OEx = 0V, VOUT = VDD			1	μA
IOZL	High Impedance Leakage Current	OEx = 0V, VOUT = 0V	-1			μA

TABLE 5C. AC ELECTRICAL CHARACTERISTICS, VDD = VDD1 = VDD2 = 2.5V±5%, TA = 0° TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				133	MHz
tpLH	Propagation Delay, Low-to-High	0 < f ≤ 200MHz	1.0	2.5	3.7	ns
tpHL	Propagation Delay, High-to-Low	0 < f ≤ 200MHz	1.4	2.6	3.5	ns
tsk(o)	Output Skew; NOTE 3	Measured on rising edge @VDDx/2			250	ps
tsk(p)	Process Skew; NOTE 4	Measured on rising edge @VDDx/2			500	ps
tsk(pp)	Part-to-Part Skew; NOTE 5	Measured on rising edge @VDDx/2			750	ps
tR	Output Rise Time			0.5	0.8	ns
tF	Output Fall Time			0.9	1.7	ns
tPW	Output Pulse Width		tCYCLE/2 - 0.75	tCYCLE/2	tCYCLE/2 + 0.75	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to VDDx/2.

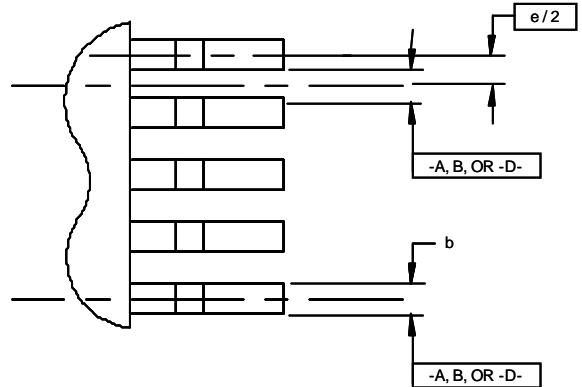
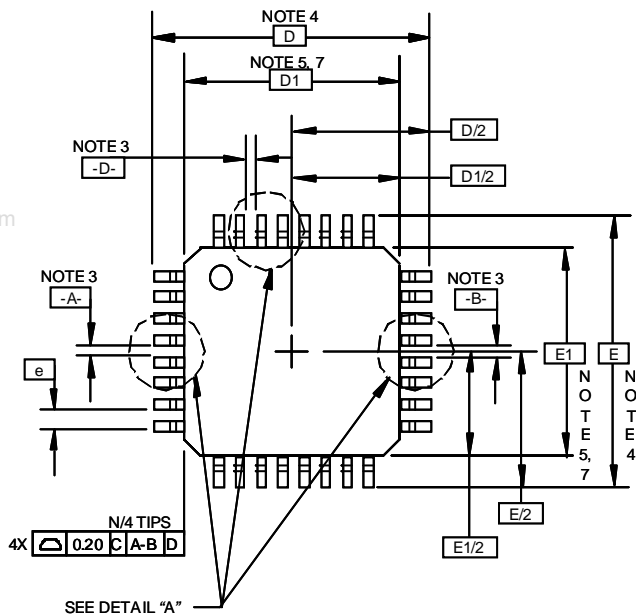
NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at the same output on different devices operating at the same supply voltages and with equal load conditions.

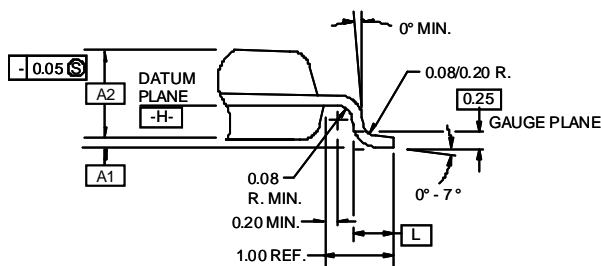
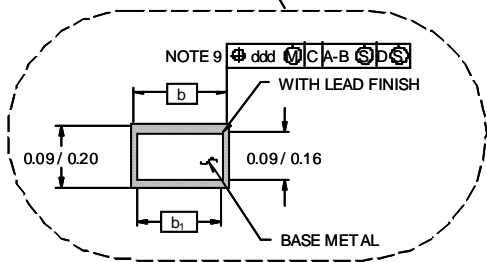
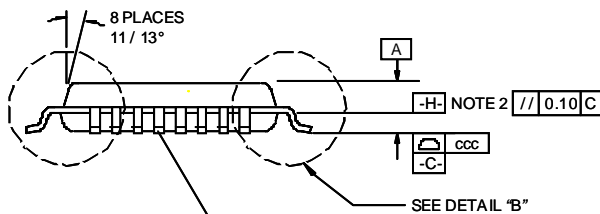
NOTE 5: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



PACKAGE OUTLINE & DIMENSIONS



- NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
 2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
 3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
 4. TO BE DETERMINED AT SEATING PLACE -C- .
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 6. "N" IS THE TOTAL NUMBER OF TERMINALS.
 7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
 8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
 9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
 10. CONTROLLING DIMENSION: MILLIMETER.
 11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION BBA.
 12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBA			
	MIN	NOM	MAX	
A			1.60	
A1	0.05		0.15	12
A2	1.35	1.4	1.45	
D		9.00 BSC.		4
D1		7.00 BSC.		7, 8
E		9.00 BSC.		4
E1		7.00 BSC.		7, 8
L	0.45	0.60	0.75	
N		32		
e		0.80 BSC.		
b	0.30	0.37	0.45	
b1	0.30	0.35	0.40	9
ccc			0.10	
ddd			0.20	



**Integrated
Circuit
Systems, Inc.**

ICS8343

LOW SKEW 1-TO-16 FANOUT BUFFER

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8343Y	ICS8343Y	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8343YT	ICS8343Y	32 Lead LQFP on Tape and Reel	2000	0°C to 70°C

www.DataSheet4U.com

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.