LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

ICS8344I-01

General Description

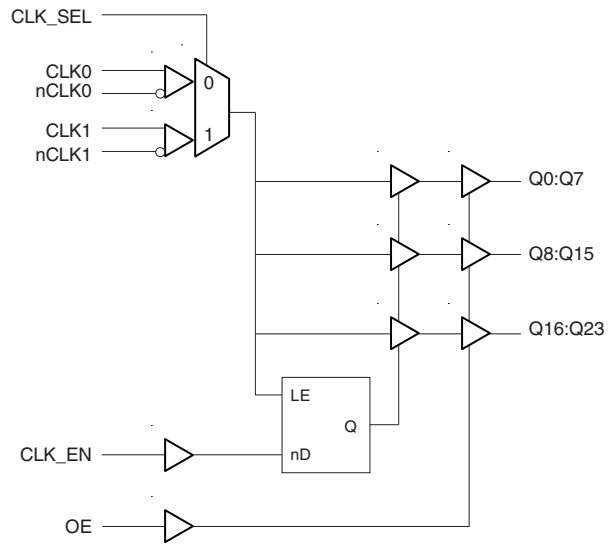
The ICS8344I-01 is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8344I-01 has two selectable clock inputs. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS8344I-01 is designed to translate any differential signal level to LVCMOS/LVTTL levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock inputs which also facilitate board level testing. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The outputs are driven low when disabled. The ICS8344I-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

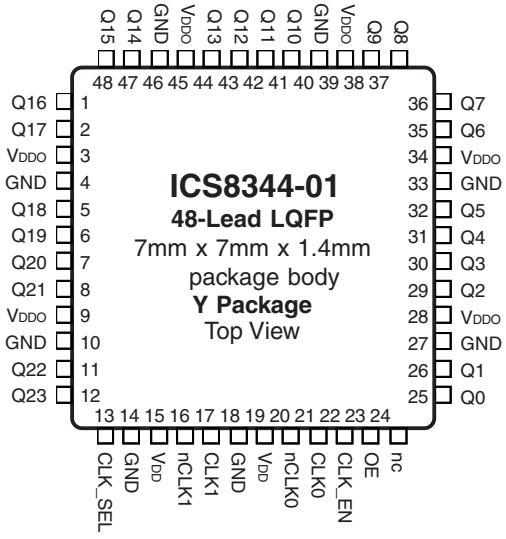
Features

- Twenty-four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Two selectable differential CLKx, nCLKx inputs
- CLK0, nCLK0 and CLK1, nCLK1 pairs can accept the following input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 200MHz
- Translates any single ended input signal to LVCMOS/LVTTL with resistor bias on nCLK input
- Synchronous clock enable
- Output skew: 250ps (maximum)
- Part-to-part skew: 1ns (maximum)
- Bank skew: 125ps (maximum)
- Propagation delay: 5.25ns (maximum)
- Output supply modes:
  Core/Output
  3.3V/3.3V
  2.5V/2.5V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q16 thru Q23 outputs. 7Ω typical output impedance.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins.
4, 10, 14,18, 27, 33, 40, 46	GND	Power		Power supply ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK inputs, When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levelss.
15, 19	V_{DD}	Power		Core supply pins.
16	nCLK1	Input	Pullup	Inverting differential LVPECL clock input.
17	CLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
20	nCLK0	Input	Pullup	Inverting differential LVPECL clock input.
21	CLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
22	CLK_EN	Input	Pullup	Synchronizing control for enabling and disabling clock outputs. LVCMOS interface levels.
23	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q23. LVCMOS / LVTTL interface levels.
24	nc	Unused		No connect.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Q0 thru Q7 outputs. 7Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Q8 thru Q15 outputs. 7Ω typical output impedance.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)					pF
R_{PULLUP}	Input Pullup Resistor			51		KW
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Banks 1, 2, 3		
Inputs		Outputs
OE	CLK_EN	Q0-Q23
0	X	Hi-Z
1	0	Disabled in logic LOW state. NOTE 1
1	1	Enabled. NOTE 1

NOTE 1: The clock enable and disable function is synchronous to the falling edge of the selected reference clock.

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	CLK1, nCLK1
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE	CLK0, CLK1	nCLK0, nCLK1	Q0 thru Q23		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 8, Figure 1, which discusses *Wiring the Differential Input to Accept Single-Ended Levels.*

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$ or 2.5V ± 5%, or $V_{DD} = 3.3V ± 5\%$, $V_{DDO} = 2.5V ± 5\%$; T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				70	mA
I_{DDO}	Output Supply Current				25	mA

Table 4B. LVCMOS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$ or 2.5V ± 5%, or $V_{DD} = 3.3V ± 5\%$, $V_{DDO} = 2.5V ± 5\%$; T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, CLK_EN, OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
		CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	V_{DD} = 3.465 or 2.625V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465 or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.135V, I_{OH} = -36mA	2.6			V
			V_{DDO} = 2.375V, I_{OH} = -27mA	1.8			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.135V, I_{OL} = 36mA			0.5	V
			V_{DDO} = 2.375V, I_{OL} = 27mA			0.5	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$ OR 2.5V ± 5%, OR $V_{DD} = 3.3V ± 5\%$, $V_{DDO} = 2.5V ± 5\%$; T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage: NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

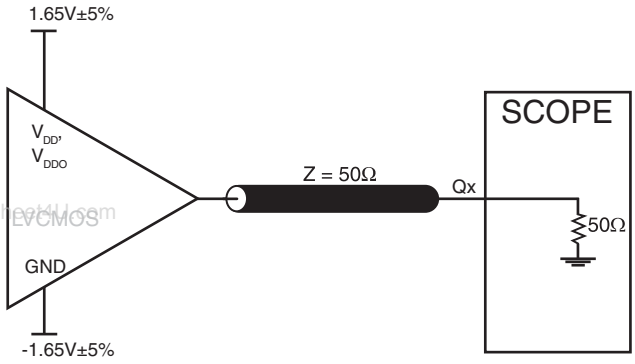
NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$ OR 2.5V ± 5%, OR $V_{DD} = 3.3V ± 5\%$, $V_{DDO} = 2.5V ± 5\%$; T_A = -40°C TO 85°C

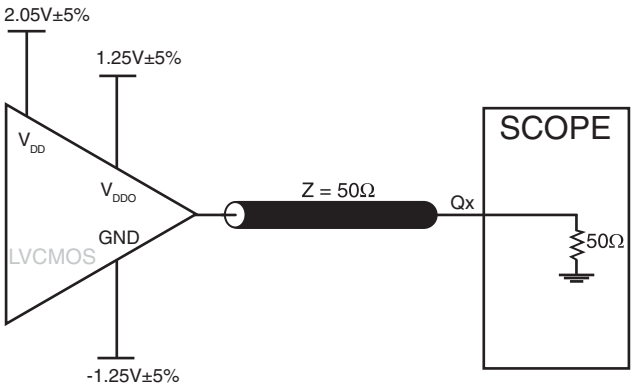
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					200	MHz
t_{PD}	Propagation Delay, NOTE 1		f ≤ 200MHz	2.5		5.25	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Q0:Q7	Measured on the rising edge of $V_{DDO}/2$			125	ps
		Q8:Q15				200	ps
		Q16:Q23				175	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the rising edge of $V_{DDO}/2$			250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6		Measured on the rising edge of $V_{DDO}/2$			1	ns
t_R	Output Rise Time; NOTE 5		30% to 70%	200		800	ps
t_F	Output Fall Time; NOTE 5		30% to 70%	200		800	ps
odc	Output Duty Cycle		f ≤ 200MHz	40%		60%	%
t_{EN}	Output Enable Time; NOTE 5		f = 10MHz			5	ns
t_{DIS}	Output Disable TIme; NOTE 5		f = 10MHz			4	ns

All parameters measured at 200MHz and V_{PP}typ unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

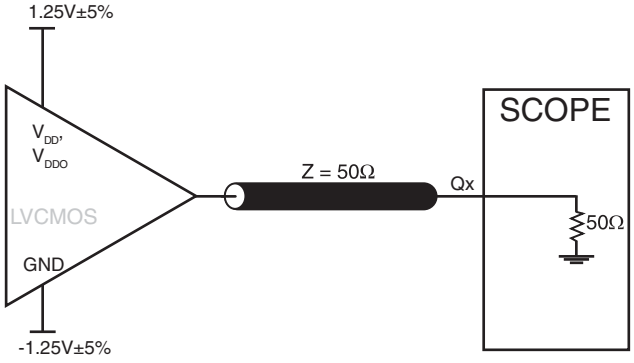
PARAMETER MEASUREMENT INFORMATION



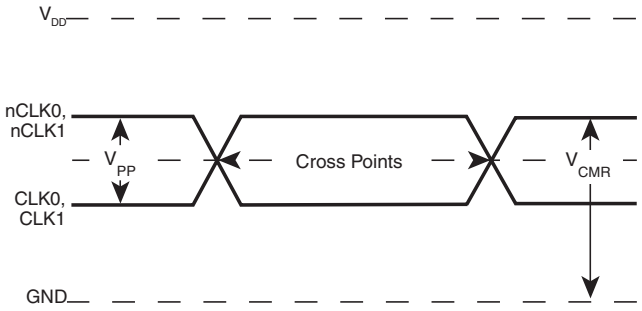
3.3V OUTPUT LOAD AC TEST CIRCUIT



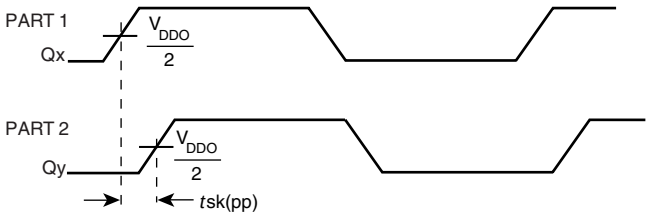
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



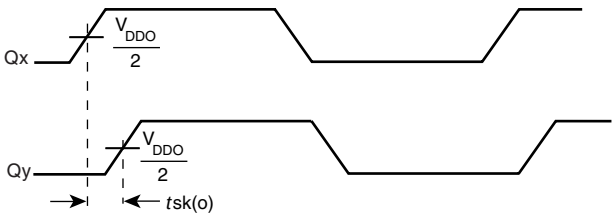
2.5V OUTPUT LOAD AC TEST CIRCUIT



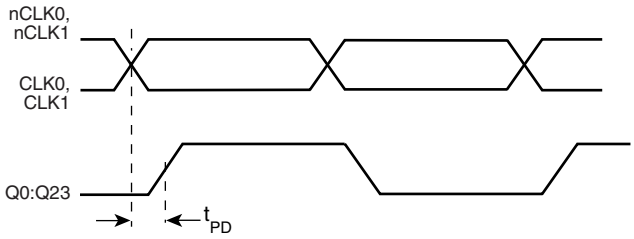
DIFFERENTIAL INPUT LEVEL



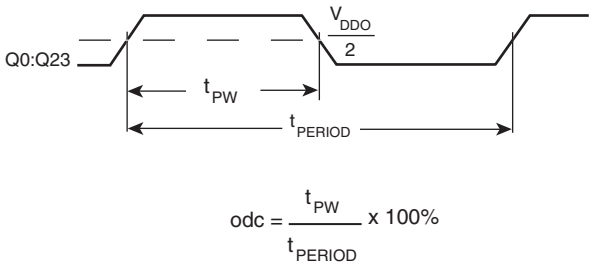
PART-TO-PART SKEW



OUTPUT SKEW

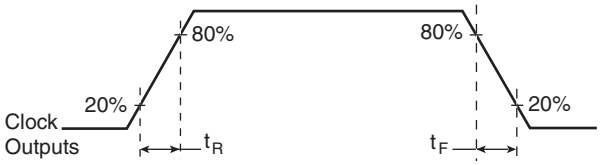


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

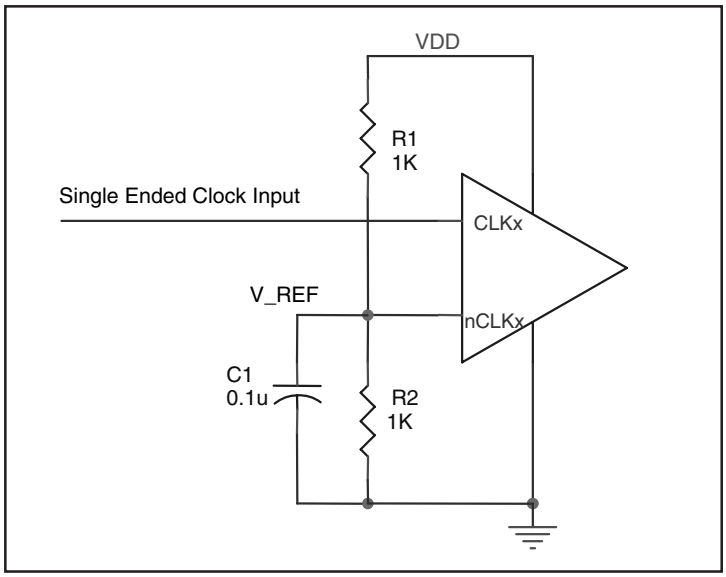


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

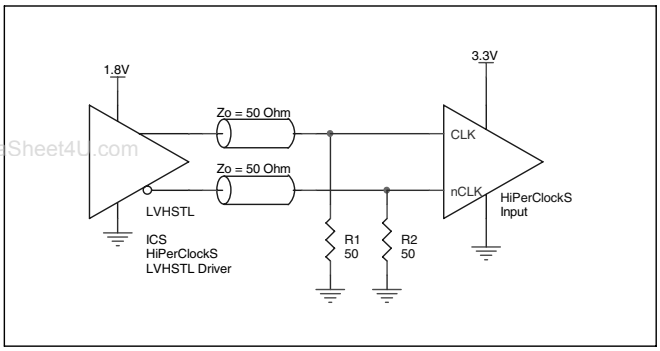


Figure 2A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

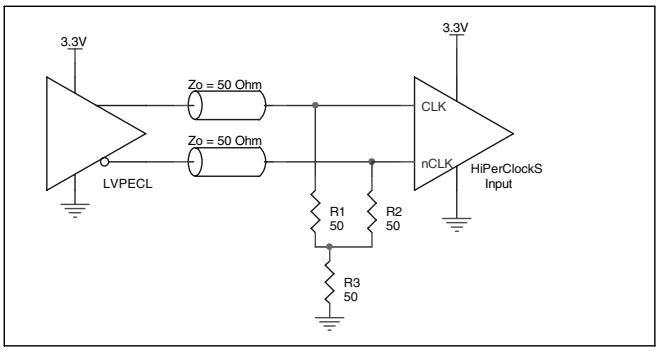


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

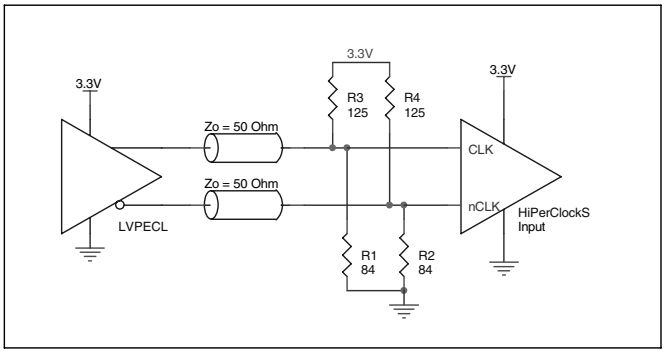


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

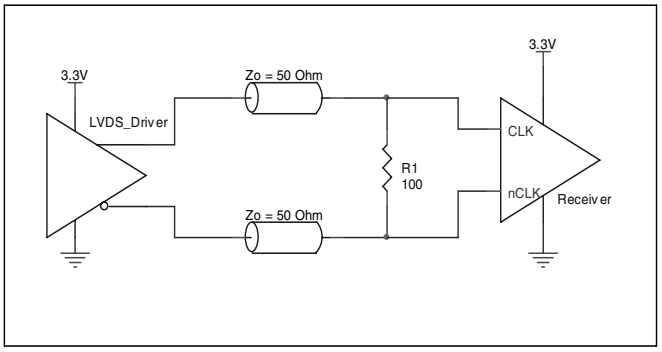


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

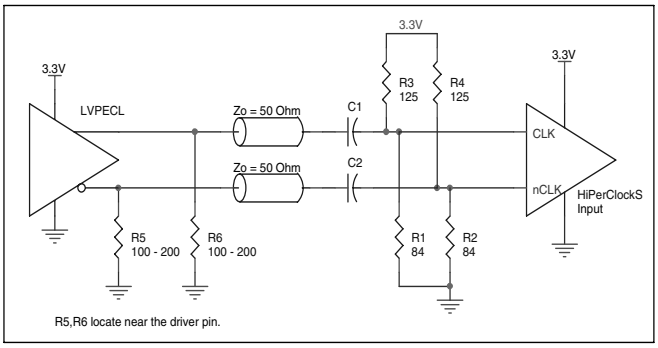


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8344I-01 is: 1503

Package Outline - Y Suffix for 48 Lead LQFP

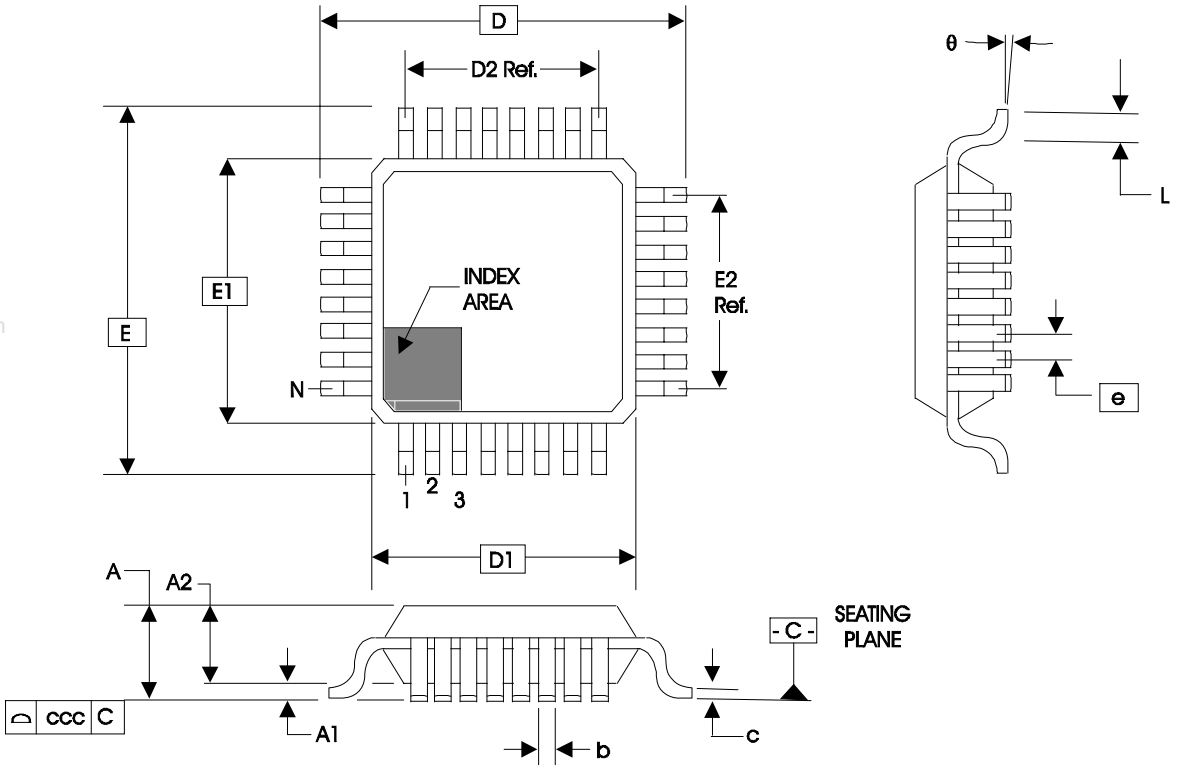


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8344AYI-01	ICS8344AYI-01	48 Lead LQFP	tray	-40°C to 85°C
ICS8344AYI-01T	ICS8344AYI-01	48 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS8344AYI-01LF	ICS8344AYI0IL	48 lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS8344AYI-01LFT	ICS8344AYI0IL	48 lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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