Integrated Circuit Systems, Inc.

ICS8344I

LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

The ICS8344I is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8344I has two selectable clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. The ICS8344I is designed to translate any differential signal levels to LVCMOS levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. ICS8344I is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

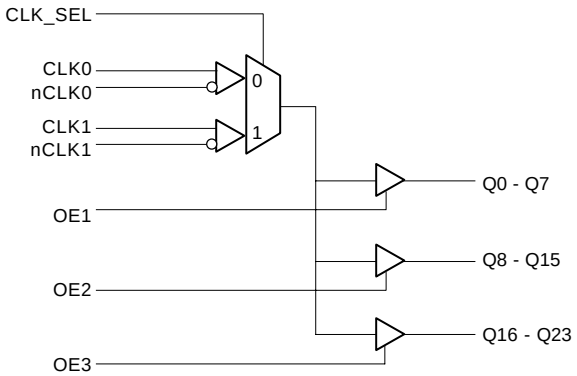
Guaranteed output and part-to-part skew characteristics make the ICS8344I ideal for those clock distribution applications demanding well defined performance and repeatability.

www.DataSheet4U.com

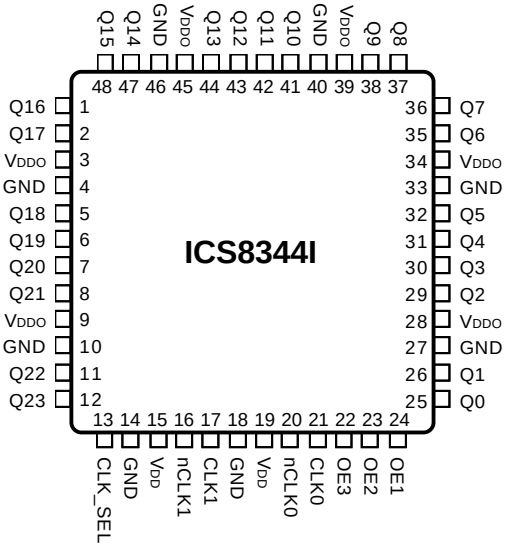
FEATURES

- 24 LVCMOS outputs, 7Ω typical output impedance
- 2 selectable differential clock input pairs for redundant clock applications
- CLKx, nCLKx pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 100MHz
- Translates any single-ended input signal to LVCMOS with resistor bias on nCLK input
- Multiple output enable pins for disabling unused outputs in reduced fanout applications
- Output skew: 275ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Bank skew: 150ps (maximum)
- 3.3V, 2.5V or mixed 3.3V, 2.5V operating supply modes
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

www.DataSheet4U.com

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q16 thru Q23 outputs. 7Ω typical output impedance.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins. Connect 3.3V or 2.5V.
4, 10, 14,18, 27, 33, 40, 46	GND	Power		Power supply ground. Connect to ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0. LVTTL / LVCMOS interface levels.
15, 19	V_{DD}	Power		Positive supply pins. Connect 3.3V or 2.5V.
16	nCLK1	Input	Pullup	Inverting differential clock input.
17	CLK1	Input	Pulldown	Non-inverting differential clock input..
20	nCLK0	Input	Pullup	Inverting differential clock input.
21	CLK0	Input	Pulldown	Non-inverting differential clock input..
22	OE3	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q16 thru Q23.
23	OE2	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q8 thru Q15.
24	OE1	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q7.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Q0 thru Q7 outputs. 7Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Q8 thru Q15 outputs. 7Ω typical output impedance.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK0, nCLK0, CLK1, nCLK1				4	pF
		CLK_SEL, OE1, OE2, OE3				4	pF
C_{PD}	Power Dissipation Capacitance (per output)					20	pF
R_{PULLUP}	Input Pullup Resistor				51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		KΩ
R_{OUT}	Output Impedance				7		Ω

www.DataSheet4U.com

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	Output	Input	Output	Input	Output
OE1	Q0-Q7	OE2	Q8-Q15	OE3	Q16-Q23
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Enabled	1	Enabled	1	Enabled

www.DataSheet4U.com

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	CLK1, nCLK1
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUTS FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE1, OE2, OE3	CLK	nCLK	Q0 thru Q23		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 13, Figure 8, which discusses wiring the differential input to accept single ended levels.

www.DataSheet4U.com

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

www.DataSheet4U.com

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Quiescent Power Supply Current				95	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO}$ = 3.135V, I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO}$ = 3.135V, I_{OL} = 36mA			0.6	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

www.DataSheet4U.com

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.6		4.3	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.4		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			5	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			4	ns

All parameters measured at 100MHz unless noted otherwise.
NOTE 1: Measured from the diffferential input crossing point to $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

www.DataSheet4U.com

www.DataSheet4U.com

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

www.DataSheet4U.com

TABLE 4E. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465, V_{IN} = 0	-5			µA
V_{OH}	Output High Voltage		V_{DD} = 3.135V, V_{DDO} = 2.375V I_{OH} = -27mA	2			V
V_{OL}	Output Low Voltage		V_{DD} = 3.135V, V_{DDO} = 2.365V I_{OL} = 27mA			0.63	V

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

www.DataSheet4U.com

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.6		4.5	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.6		4.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

All parameters measured at 100MHz unless noted otherwise.
NOTE 1: Measured from the diffferential input crossing point to V_{DDO}/2.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

www.DataSheet4U.com

www.DataSheet4U.com

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

www.DataSheet4U.com

TABLE 4H. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		2.9	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 2.625$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = VDDO = 2.375V$ $I_{OH} = -27mA$	2			V
V_{OL}	Output Low Voltage		$V_{DD} = VDDO = 2.375V$ $I_{OL} = 27mA$			0.6	V

TABLE 4I. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

www.DataSheet4U.com

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.7		4.3	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.7		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

All parameters measured at 100MHz unless noted otherwise.
NOTE 1: Measured from the diffferential input crossing point to $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

www.DataSheet4U.com

www.DataSheet4U.com

PARAMETER MEASUREMENT INFORMATION

www.DataSheet4U.com

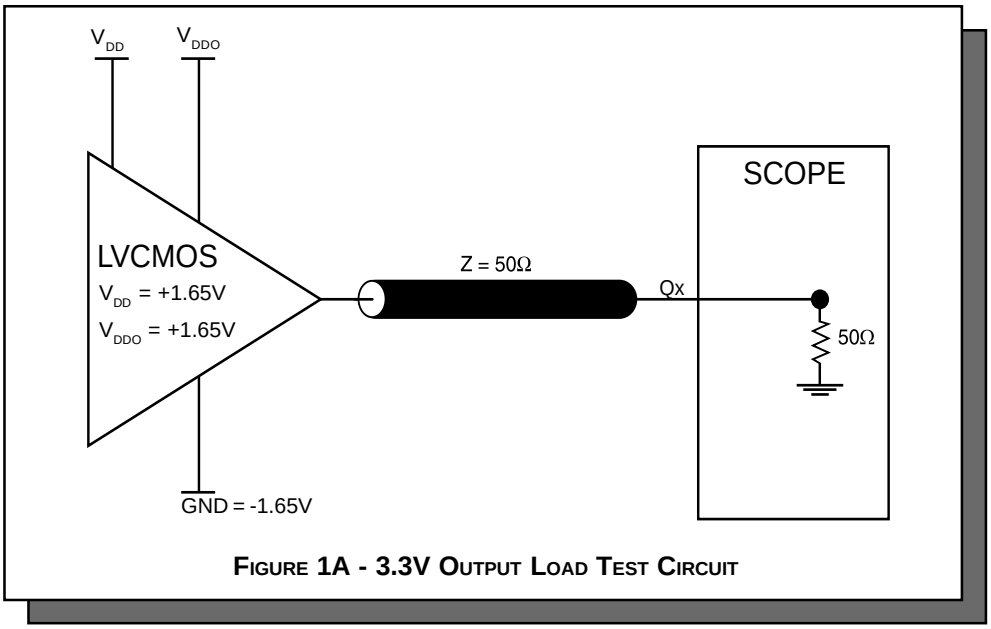


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

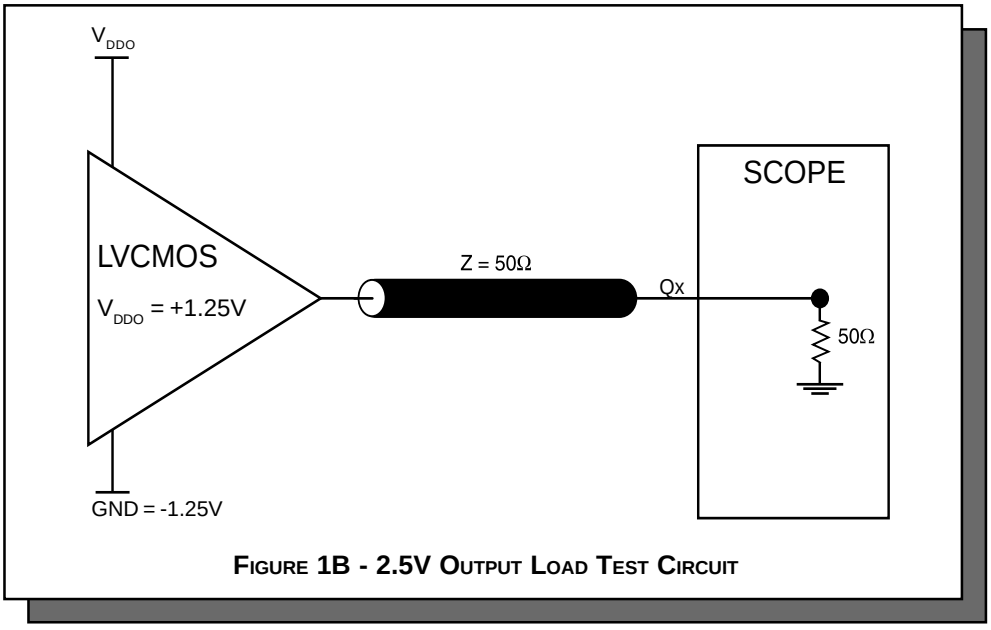


FIGURE 1B - 2.5V OUTPUT LOAD TEST CIRCUIT

www.DataSheet4U.com

www.DataSheet4U.com

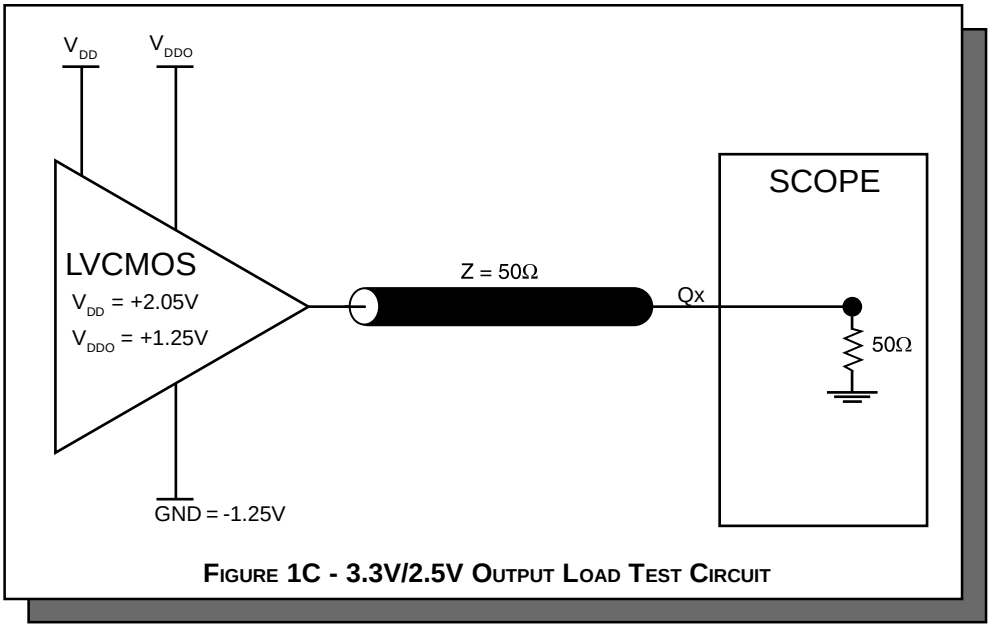


FIGURE 1C - 3.3V/2.5V OUTPUT LOAD TEST CIRCUIT

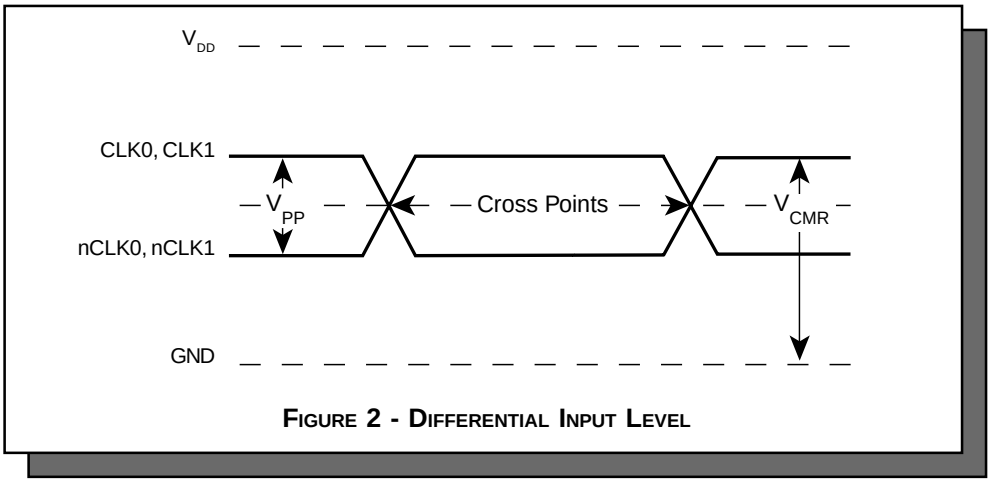


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

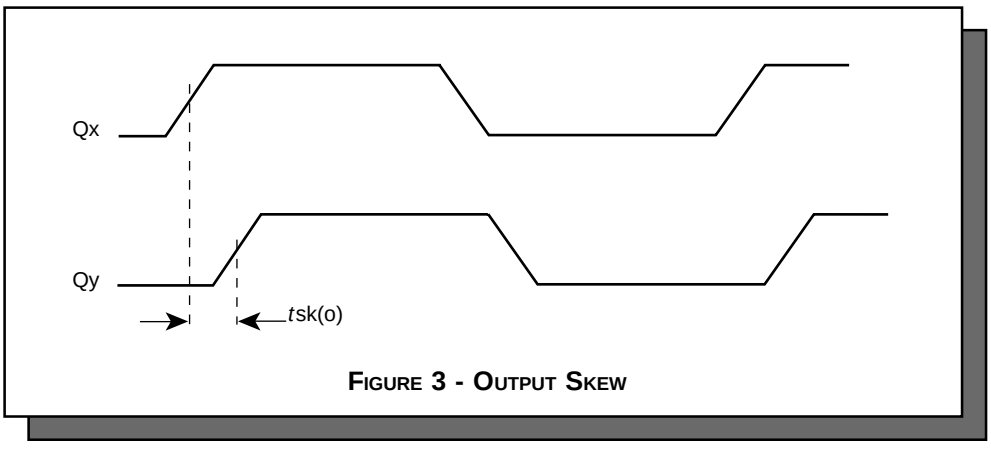


FIGURE 3 - OUTPUT SKEW

www.DataSheet4U.com

www.DataSheet4U.com

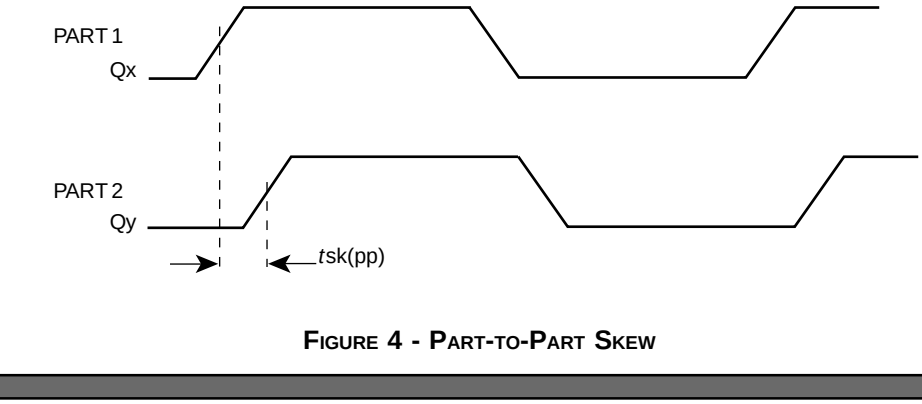


FIGURE 4 - PART-TO-PART SKEW

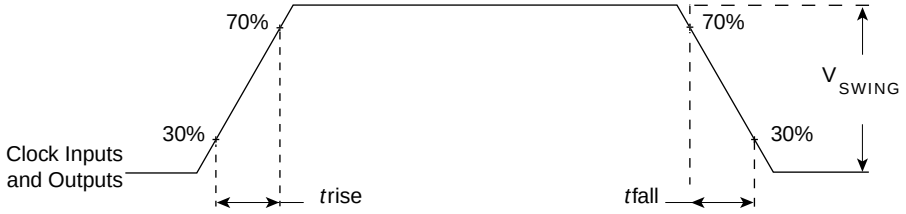


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

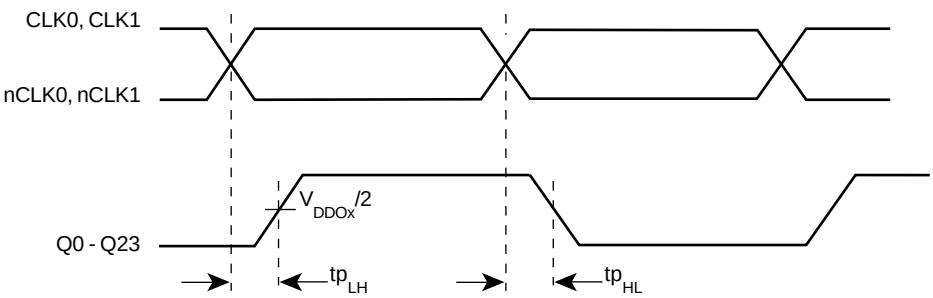


FIGURE 6 - PROPAGATION DELAY

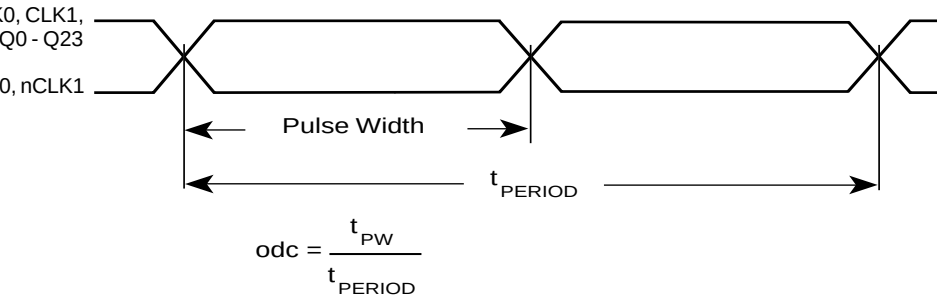


FIGURE 7 - odc & t_{PERIOD}

www.DataSheet4U.com

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

www.DataSheet4U.com

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

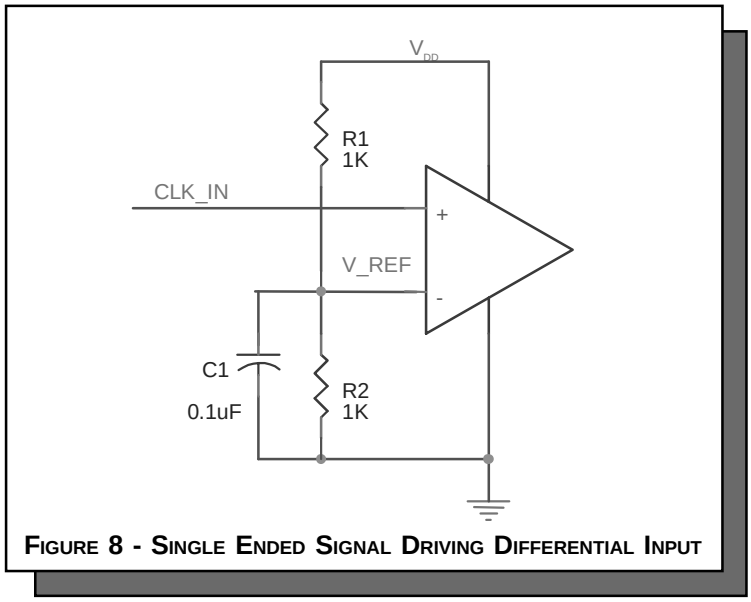


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

www.DataSheet4U.com

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

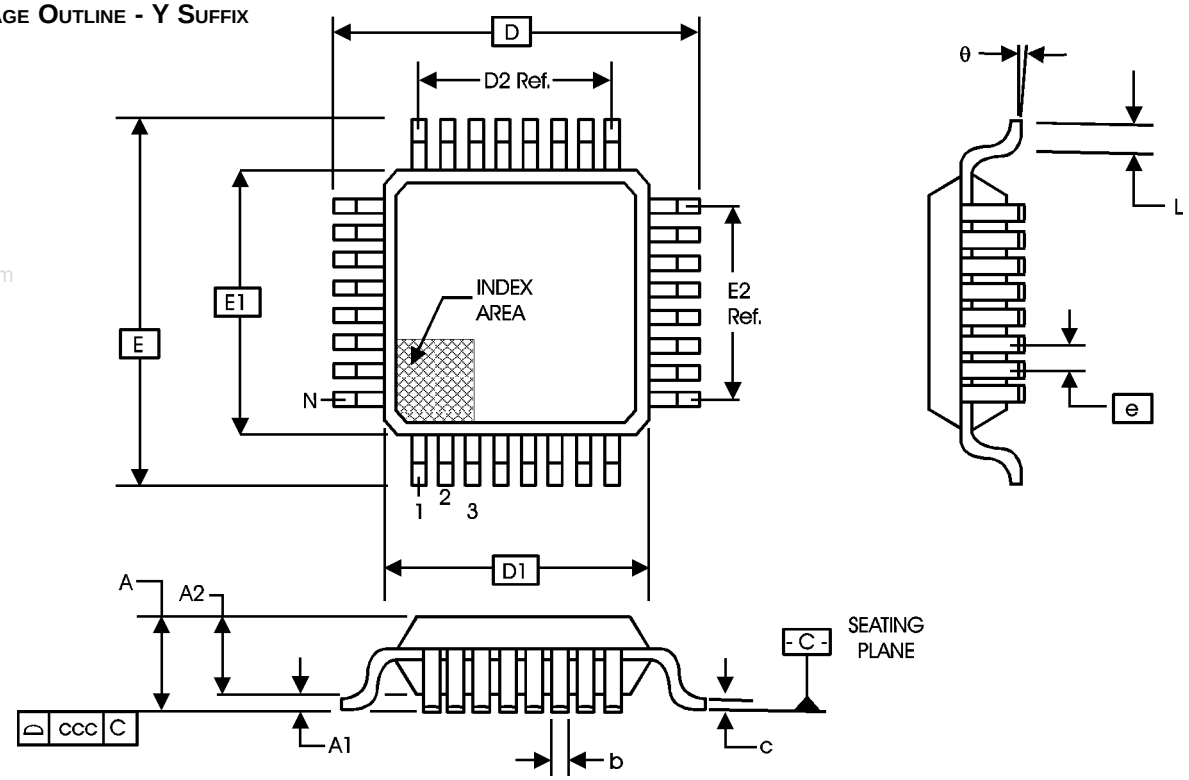
www.DataSheet4U.com

TRANSISTOR COUNT

The transistor count for ICS8344I is: 1,449

www.DataSheet4U.com

PACKAGE OUTLINE - Y SUFFIX



www.DataSheet4U.com

TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50	
e		0.5 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

www.DataSheet4U.com

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8344BYI	ICS8344BYI	48 Lead LQFP	250 per tray	-40°C to 85°C
ICS8344BYI-T	ICS8344BYI	48 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

www.DataSheet4U.com

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.

www.DataSheet4U.com