PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83905

LOW SKEW, 1:6 CRYSTAL INTERFACE-TO-LVCMOS / LVTTL FANOUT BUFFER

GENERAL DESCRIPTION

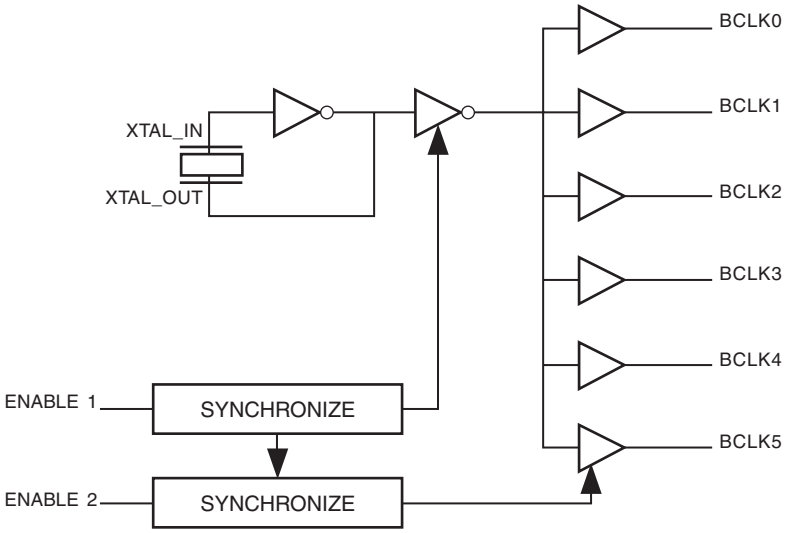
The ICS83905 is a low skew, 1-to-6 LVCMOS / LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83905 single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 6 to 12 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83905 is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply mode. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS83905 ideal for high performance, single ended applications that also require a limited output voltage.

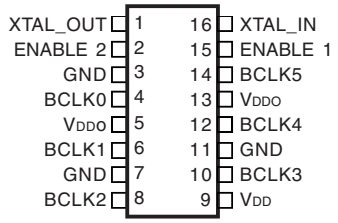
FEATURES

- 6 LVCMOS / LVTTL outputs
- Crystal oscillator interface
- Output frequency range: 10MHz to 50MHz
- Crystal input frequency range: 10MHz to 50MHz
- Output skew: 10ps (typical)
- 5V tolerant enable inputs
- Synchronous output enables
- Operating supply modes: Full 3.3V, 2.5V and 1.8V, mixed 3.3Vcore/2.5V or1.8V operating supply, and mixed 2.5V core/1.8V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant
- Pin compatible to MPC905
- Industrial version available upon request

BLOCK DIAGRAM

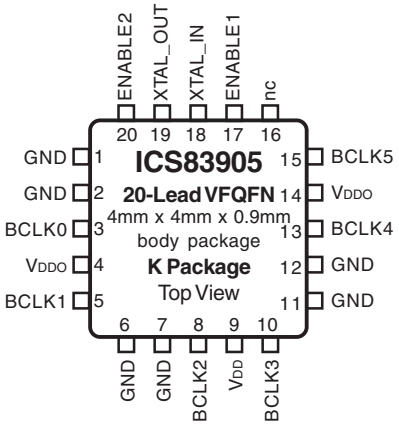


PIN ASSIGNMENT



ICS83905
16-Lead SOIC
3.9mm x 9.9mm x 1.38mm body package
M Pacakge
Top View

ICS83905
16-Lead TSSOP
4.4mm x 3.0mm x 0.92mm body package
G Pacakge
Top View



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Name	Type		Description
XTAL_OUT	Output		Crystal oscillator interface. XTAL_OUT is the output.
XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input.
ENABLE 1, ENABLE2	Input		Output enable. LVCMOS / LVTTL interface levels.
BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, BCLK5	Output		Clock outputs. LVCMOS / LVTTL interface levels.
GND	Power		Power supply ground.
V_{DD}	Power		Core supply pin.
V_{DDO}	Power		Output supply pin.
n/c	Unused		No connect.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V			19	pF
		V_{DDO} = 2.625V			18	pF
		V_{DDO} = 2V			16	pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%	5	7	12	Ω
		V_{DDO} = 2.5V ± 5%		7		Ω
		V_{DDO} = 1.8V ± 0.2V		10		Ω

TABLE 3. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Outputs	
ENABLE 1	ENABLE 2	BCLK0:BCLK4	BCLK5
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	
16 Lead SOIC package	78.8°C/W (0 mps)
16 Lead TSSOP package	89°C/W (0 lfpm)
20 Lead VFQFN package	38.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4F. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			TBD		µA
I_{DDO}	Output Supply Current			TBD		µA

TABLE 4G. LVCMOS/LVTTL DC CHARACTERISTICS, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	ENABLE1, ENABLE2	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
			V_{DD} = 1.8V ± 0.2V	0.65*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	ENABLE1, ENABLE2	V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
			V_{DD} = 1.8V ± 0.2V	-0.3		0.35*V_{DD}	V
V_{OH}	Output High Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -1mA	2			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 1mA			0.4	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
t_{PW}	Output Pulse Width	HIGH (above 2V); NOTE 1	T = Periods		0.5T		
		LOW (below 0.8V), NOTE 2			0.5T		
		HIGH (above 2V); NOTE 1			0.5T		
		LOW (below 0.8V), NOTE 2			0.5T		
t_{PER}	Output Period		T = desired Period		TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		500		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Assuming input duty cycle specs from Recommended Operating Conditons table are met.
NOTE 2: Assuming external crystal or 50% duty cycle external reference is used.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
odc	Output Duty Cycle				50		%
t_{PER}	Output Period				TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		500		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

See notes from Table 5A.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
odc	Output Duty Cycle				50		%
t_{PER}	Output Period				TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		550		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

See notes from Table 5A.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
odc	Output Duty Cycle				50		%
t_{PER}	Output Period				TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		500		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

See notes from Table 5A.

TABLE 5E. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
t_{PW}	Output Pulse Width				50		%
t_{PER}	Output Period				TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		550		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

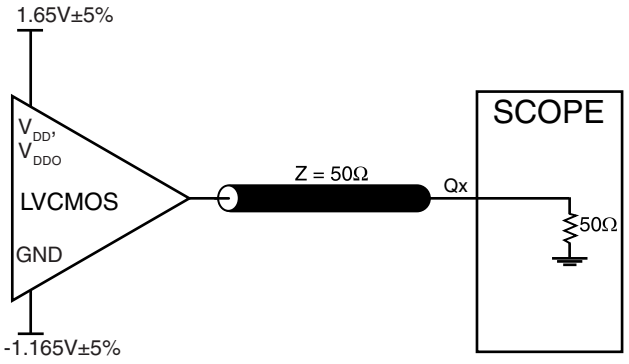
See notes from Table 5A.

TABLE 5F. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, T_A = 0°C TO 70°C

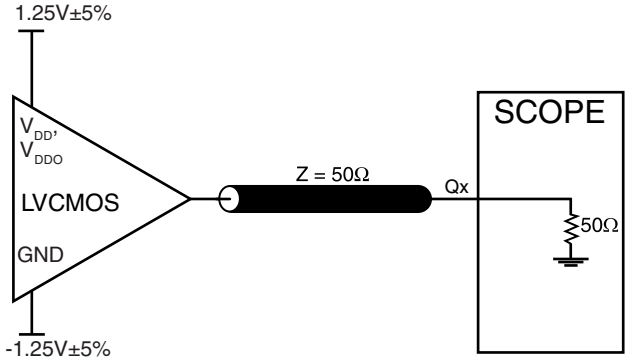
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source		DC		100	MHz
odc	Output Duty Cycle				50		%
t_{PER}	Output Period				TBD		
*t*sk(o)	Output Skew; NOTE 3, 5				10		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		550		ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1			TBD		ms
		ENABLE 2			TBD		ms
A_{OSC}	XTAL_IN to XTAL_OUT Oscillator Gain				TBD		db
Phase	Loop Phase Shift Modulo 360°+				TBD		°

See notes from Table 5A.

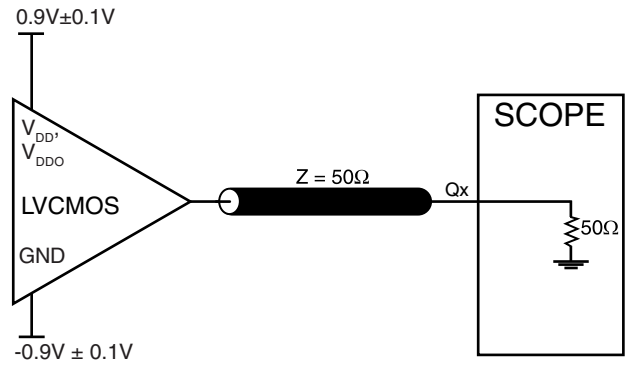
PARAMETER MEASUREMENT INFORMATION



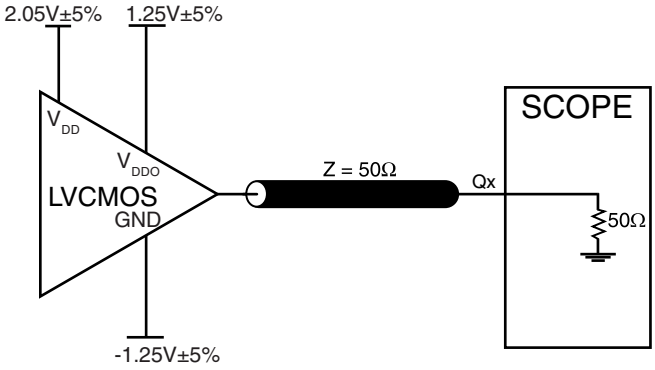
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



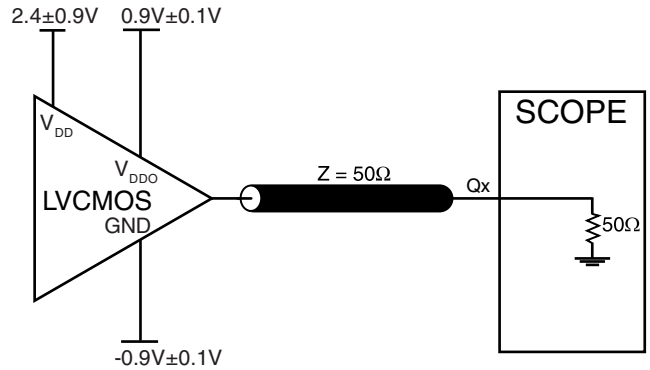
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



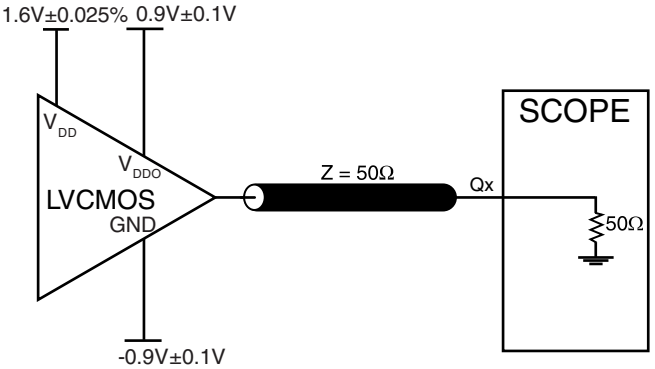
1.8V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



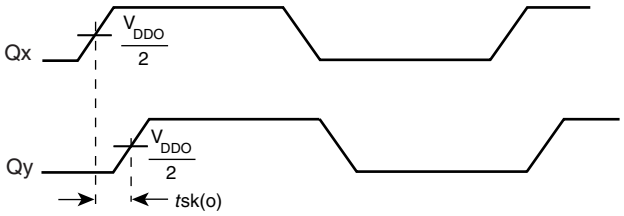
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



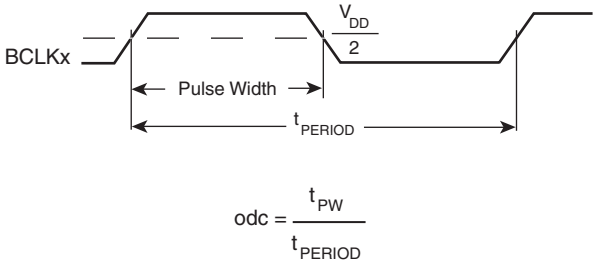
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



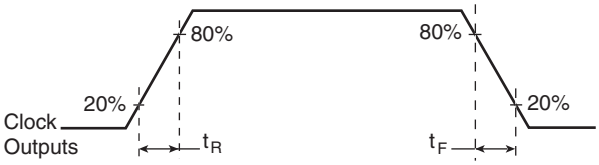
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE, FUNDAMENTAL

Figure 1A shows an example of ICS83905 crystal interface with parallel resonance crystal using fundamental frequency. The C1, C2 and R1 values are suggested for the best frequency accuracy ppm. The optimum C1 and C2 values can be adjusted to improve the frequency accuracy for stray capacitance of different board layout.

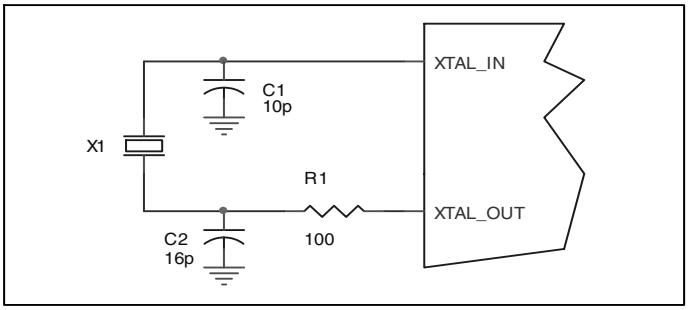


FIGURE 1A. CRYSTAL OSCILLATOR INTERFACE, (FUNDAMENTAL)

CRYSTAL INPUT INTERFACE, 3RD OVERTONE

Figure 1B shows an example of ICS83905 crystal interface with parallel resonance crystal using 3rd overtone frequency. The C1, C2 values are suggested for the best frequency accuracy ppm. The optimum C1 and C2 values can be adjusted to improve the frequency accuracy for stray capacitance of different board layout. The C3 and L1 can be calculated from the given equation.

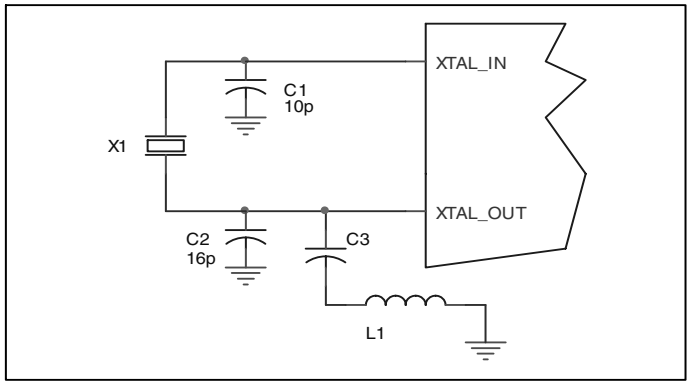


FIGURE 1B. CRYSTAL OSCILLATOR INTERFACE (3RD OVERTONE)

$$F\_fund = \frac{1}{2\pi\sqrt{L1 * C3}}$$

RELIABILITY INFORMATION

TABLE 6A. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD SOIC

θ_{JA} by Velocity (Meters per Second)	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	78.8°C/W	71.1°C/W	66.2°C/W

TABLE 6B. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 6C. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD VFQFN

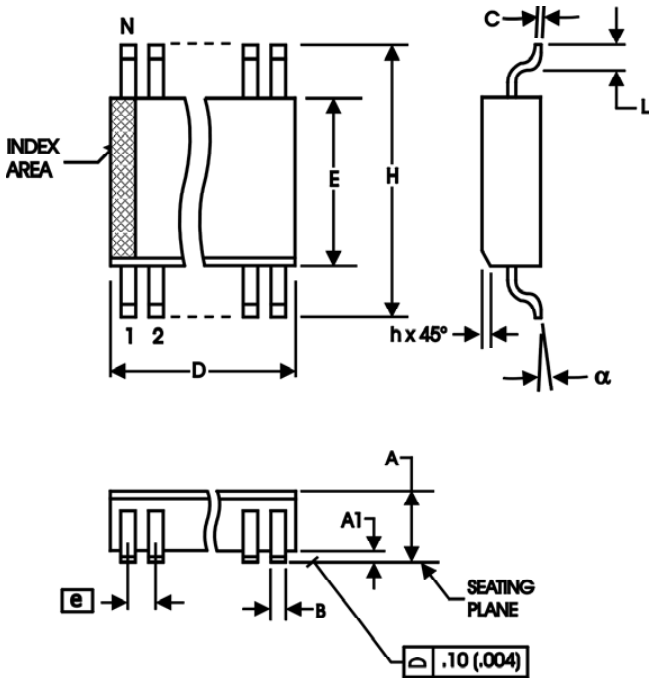
θ_{JA} by Velocity (Meters per Second)	0	1	2.5
Single-Layer PCB, JEDEC Standard Test Boards	141.7°C/W	126°C/W	116.9°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	38.5°C/W	35°C/W	33.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83905 is: 339

PACKAGE OUTLINE - M SUFFIX FOR 16 LEAD SOIC



PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

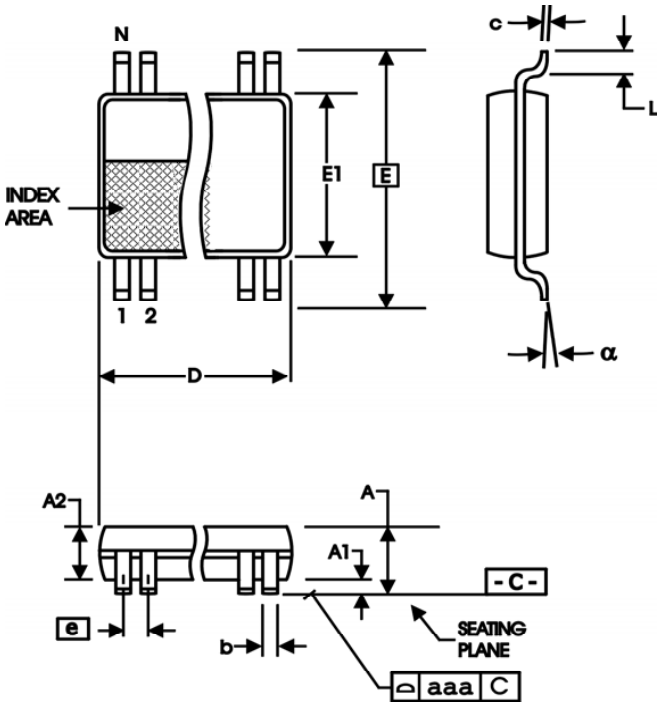


TABLE 7A. PACKAGE DIMENSIONS FOR 16 LEAD SOIC

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	16	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7B. PACKAGE DIMENSIONS FOR TSSOP

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

PACKAGE OUTLINE - K SUFFIX FOR 20 LEAD VFQFN

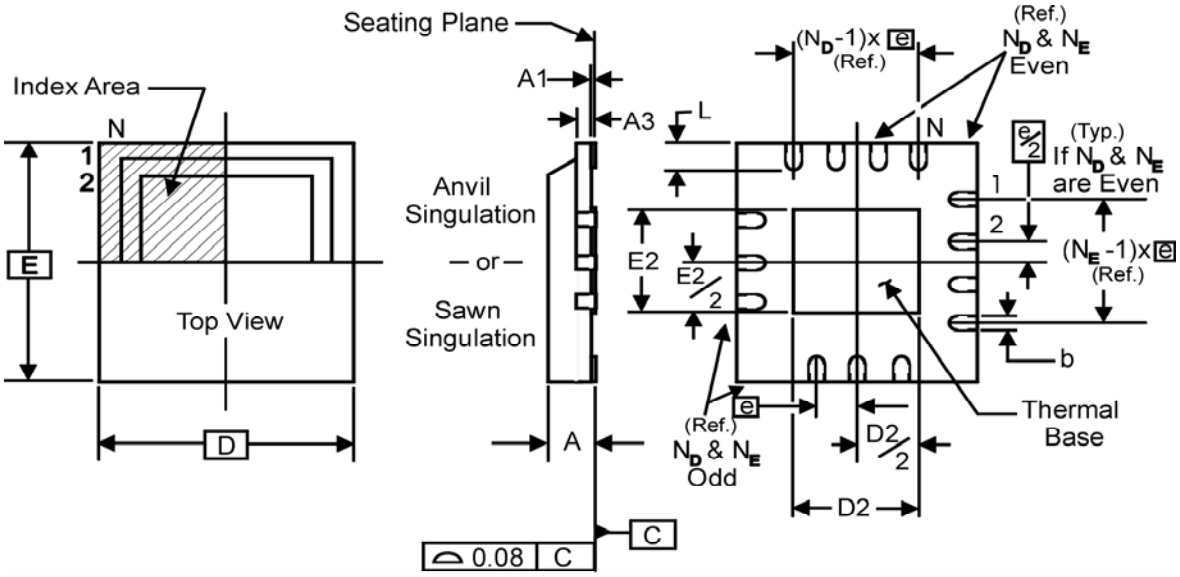


TABLE 7C. PACKAGE DIMENSIONS FOR 20 LEAD VFQFN

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	20	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	5	
N_E	5	
D	4.0	
D2	0.75	2.80
E	4.0	
E2	0.75	2.80
L	0.35	0.75

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83905AM	83905AM	16 Lead SOIC	tube	0°C to 70°C
ICS83905AMT	83905AM	16 Lead SOIC	2500 tape & reel	0°C to 70°C
ICS83905AMLF	83905AML	16 Lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS83905AMLFT	83905AML	16 Lead "Lead-Free" SOIC	2500 tape & reel	0°C to 70°C
ICS83905AG	TBD	16 Lead TSSOP	tube	0°C to 70°C
ICS83905AGT	TBD	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS83905AK	83905A	20 Lead VFQFN	tube	0°C to 70°C
ICS83905AKT	83905A	20 Lead VFQFN	2500 tape & reel	0°C to 70°C