



**GENERAL DESCRIPTION**



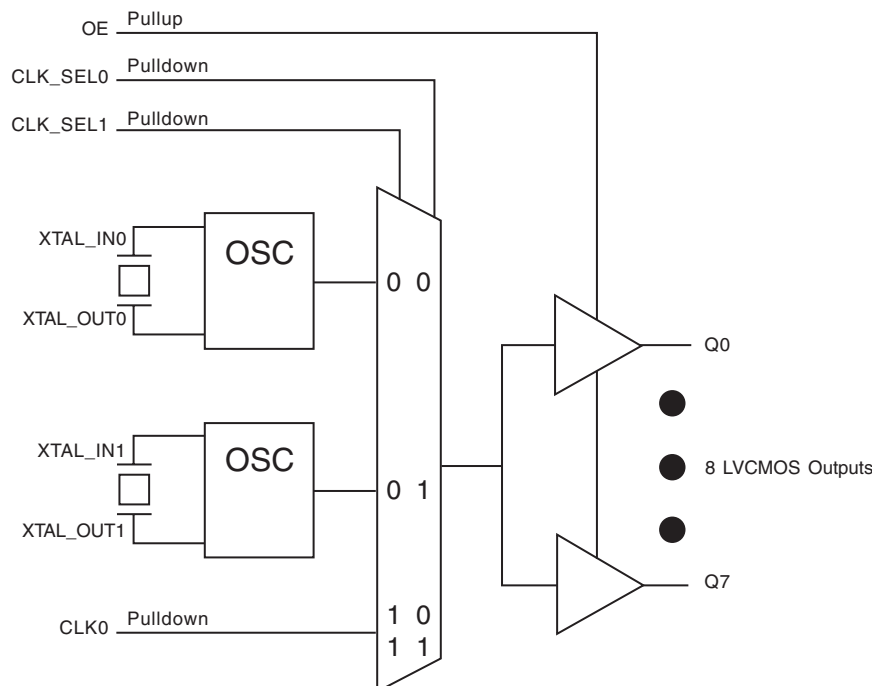
The ICS83908-02 is a low skew, high performance 1-to-8 Crystal Oscillator/3.3V LVCMOS-to-3.3V LVCMOS fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83908-02 has selectable single ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS83908-02 ideal for those applications demanding well defined performance and repeatability.

**FEATURES**

- 8 LVCMOS/LVTTL outputs (19Ω typical output impedance)
  - 2 Crystal oscillator input pairs  
1 LVCMOS/LVTTL clock input
  - Crystal input frequency range: 10MHz - 40MHz
  - Output frequency: 200MHz (typical) CLK0
  - Output Skew: TBD
  - Part to Part Skew: TBD
  - RMS phase jitter @ 25MHz (100Hz - 1MHz):  
0.22ps (typical)  $V_{DD} = V_{DDO} = 3.3V$
- | Offset | Noise Power   |
|--------|---------------|
| 100Hz  | -111.4 dBc/Hz |
| 1kHz   | -139.9 dBc/Hz |
| 10kHz  | -157.3 dBc/Hz |
| 100kHz | -157.5 dBc/Hz |
- Supply Voltage Modes:  
(Core/Output)  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
  - 0°C to 70°C ambient operating temperature
  - Industrial temperature available upon request

**BLOCK DIAGRAM**



**PIN ASSIGNMENT**

|                  |    |    |                  |
|------------------|----|----|------------------|
| V <sub>DD</sub>  | 1  | 24 | GND              |
| XTAL_IN0         | 2  | 23 | XTAL_IN1         |
| XTAL_OUT0        | 3  | 22 | XTAL_OUT1        |
| V <sub>DDO</sub> | 4  | 21 | V <sub>DDO</sub> |
| Q0               | 5  | 20 | Q7               |
| Q1               | 6  | 19 | Q6               |
| GND              | 7  | 18 | GND              |
| Q2               | 8  | 17 | Q5               |
| Q3               | 9  | 16 | Q4               |
| V <sub>DDO</sub> | 10 | 15 | V <sub>DDO</sub> |
| CLK_SEL0         | 11 | 14 | CLK_SEL1         |
| CLK0             | 12 | 13 | OE               |

**ICS83908-02**  
**24-Lead, 173-MIL TSSOP**  
 4.4mm x 7.8mm x 0.92mm  
 body package  
**G Package**  
 Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



**TABLE 1. PIN DESCRIPTIONS**

| Number                           | Name                                 | Type   |          | Description  |
|----------------------------------|--------------------------------------|--------|----------|--|
| 1                                | V <sub>DD</sub>                      | Power  |          | Core supply pin.   |
| 2, 3                             | XTAL_IN0,<br>XTAL_OUT0               | Input  |          | Crystal oscillator interface. XTAL_IN0 is the input.<br>XTAL_OUT0 is the output.   |
| 4, 10, 15, 21                    | V <sub>DDO</sub>                     | Power  |          | Output supply pins.  |
| 5, 6, 8,<br>9, 16, 17,<br>19, 20 | Q0, Q1, Q2,<br>Q3, Q4, Q5,<br>Q6, Q7 | Output |          | Single-ended clock outputs. LVCMOS/LVTTL interface levels.   |
| 7, 18, 24                        | GND                                  | Power  |          | Power supply ground.   |
| 11,<br>14                        | CLK_SEL0,<br>CLK_SEL1                | Input  | Pulldown | Clock select inputs. See Table 3, Input Reference Function Table.<br>LVCMOS / LVTTL interface levels.                            |
| 12                               | CLK0                                 | Input  | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels.   |
| 13                               | OE                                   | Input  | Pullup   | Output enable. When LOW, outputs are in HIGH impedance state.<br>When HIGH, outputs are active. LVCMOS / LVTTL interface levels. |
| 22, 23                           | XTAL_OUT1,<br>XTAL_IN1               | Input  |          | Crystal oscillator interface. XTAL_IN1 is the input.<br>XTAL_OUT1 is the output.   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter                                     | Test Conditions                | Minimum | Typical | Maximum | Units |
|-----------------------|---|--------------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                             |                                |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                         |                                |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                       |                                |         | 51      |         | kΩ    |
| C <sub>PD</sub>       | Power Dissipation Capacitance<br>(per output) | V <sub>DDO</sub> = 3.465V      |         | 7       |         | pF    |
|                       |   | V <sub>DDO</sub> = 2.625V      |         | 7       |         | pF    |
|                       |   | V <sub>DDO</sub> = 2V          |         | 6       |         | pF    |
| R <sub>OUT</sub>      | Output Impedance                              | V <sub>DDO</sub> = 3.3V ± 5%   |         | 19      |         | Ω     |
|                       |   | V <sub>DDO</sub> = 2.5V ± 5%   |         | TBD     |         | Ω     |
|                       |   | V <sub>DDO</sub> = 1.8V ± 0.2V |         | TBD     |         | Ω     |

**TABLE 3. INPUT REFERENCE FUNCTION TABLE**

| Control Inputs |          | Reference       |
|----------------|----------|-----------------|
| CLK_SEL1       | CLK_SEL0 |                 |
| 0              | 0        | XTAL0 (default) |
| 0              | 1        | XTAL1           |
| 1              | 0        | CLK0            |
| 1              | 1        | CLK0            |



**ABSOLUTE MAXIMUM RATINGS**

|  |                           |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 70°C/W (0 mps)            |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

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**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         | 25      |         | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         | 121     |         | mA    |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         | 26      |         | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         | 82      |         | mA    |

**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current  |                 |         | 26      |         | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         | 53      |         | mA    |

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         | 13      |         | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         | 77      |         | mA    |

**TABLE 4E. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current  |                 |         | 13      |         | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         | 51      |         | mA    |



**TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS,  $T_A = -40^{\circ}\text{C}$  TO  $85^{\circ}\text{C}$**

| Symbol   | Parameter           | Test Conditions   | Minimum | Typical | Maximum        | Units         |
|----------|---------------------|---|---------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage  | $V_{DD} = 3.3\text{V} \pm 5\%$                                      | 2.0     |         | $V_{DD} + 0.3$ | V             |
|          |                     | $V_{DD} = 2.5\text{V} \pm 5\%$                                      | 1.7     |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage   | $V_{DD} = 3.3\text{V} \pm 5\%$                                      | -0.3    |         | 0.8            | V             |
|          |                     | $V_{DD} = 2.5\text{V} \pm 5\%$                                      | -0.3    |         | 0.7            | V             |
| $I_{IH}$ | Input High Current  | CLK0, CLK_SEL0:1<br>$V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$ |         |         | 150            | $\mu\text{A}$ |
|          |                     | OE<br>$V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$               |         |         | 5              | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current   | CLK0, CLK_SEL0:1<br>$V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$ | -5      |         |                | $\mu\text{A}$ |
|          |                     | OE<br>$V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$               | -150    |         |                | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage | $V_{DDO} = 3.3\text{V} \pm 5\%$ ; NOTE 1                            | 2.6     |         |                | V             |
|          |                     | $V_{DDO} = 2.5\text{V} \pm 5\%$ ; NOTE 1                            | 1.8     |         |                | V             |
|          |                     | $V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ ; NOTE 1                    | 1.5     |         |                | V             |
| $V_{OL}$ | Output Low Voltage  | $V_{DDO} = 3.3\text{V} \pm 5\%$ ; NOTE 1                            |         |         | 0.5            | V             |
|          |                     | $V_{DDO} = 2.5\text{V} \pm 5\%$ ; NOTE 1                            |         |         | 0.5            | V             |
|          |                     | $V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ ; NOTE 1                    |         |         | 0.4            | V             |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, "Load Test Circuit" diagrams.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation / cut          |                 | Fundamental |         |         |          |
| Frequency                          |                 | 10          |         | 40      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |
| Drive Level                        |                 |             |         | 1       | mW       |



**TABLE 6A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                              | Test Conditions       | Minimum | Typical | Maximum | Units |
|----------------------|--|-----------------------|---------|---------|---------|-------|
| $f_{MAX}$            | Output Frequency                       | w/External XTAL       | 10      |         | 40      | MHz   |
|                      |  | w/External CLK        |         | 200     |         | MHz   |
| $t_{pLH}$            | Propagation Delay, Low-to-High; NOTE 1 |                       |         | 2       |         | ns    |
| $t_{sk(o)}$          | Output Skew; NOTE 2                    |                       |         | TBD     |         | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 2, 3           |                       |         | TBD     |         | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 2, 4    | 25MHz, (100Hz - 1MHz) |         | 0.22    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                  | 20% to 80%            |         | 457     |         | ps    |
| odc                  | Output Duty Cycle                      |                       |         | 50      |         | %     |
| $t_{EN}$             | Output Enable Time; NOTE 5             |                       |         |         | 10      | ns    |
| $t_{DIS}$            | Output Disable Time; NOTE 5            |                       |         |         | 8       | ns    |

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                              | Test Conditions       | Minimum | Typical | Maximum | Units |
|----------------------|--|-----------------------|---------|---------|---------|-------|
| $f_{MAX}$            | Output Frequency                       | w/External XTAL       | 10      |         | 40      | MHz   |
|                      |  | w/External CLK        |         | 200     |         | MHz   |
| $t_{pLH}$            | Propagation Delay, Low-to-High; NOTE 1 |                       |         | 2.2     |         | ns    |
| $t_{sk(o)}$          | Output Skew; NOTE 2                    |                       |         | TBD     |         | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 2, 3           |                       |         | TBD     |         | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 2, 4    | 25MHz, (100Hz - 1MHz) |         | 0.21    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                  | 20% to 80%            |         | 463     |         | ps    |
| odc                  | Output Duty Cycle                      |                       |         | 50      |         | %     |
| $t_{EN}$             | Output Enable Time; NOTE 5             |                       |         |         | 10      | ns    |
| $t_{DIS}$            | Output Disable Time; NOTE 5            |                       |         |         | 8       | ns    |

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.



**TABLE 6C. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                              | Test Conditions       | Minimum | Typical | Maximum | Units |
|----------------------|--|-----------------------|---------|---------|---------|-------|
| $f_{MAX}$            | Output Frequency                       | w/External XTAL       | 10      |         | 40      | MHz   |
|                      |  | w/External CLK        |         | 200     |         | MHz   |
| $t_{pLH}$            | Propagation Delay, Low-to-High; NOTE 1 |                       |         | 2.5     |         | ns    |
| $t_{sk(o)}$          | Output Skew; NOTE 2                    |                       |         | TBD     |         | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 2, 3           |                       |         | TBD     |         | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 2, 4    | 25MHz, (100Hz - 1MHz) |         | 0.22    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                  | 20% to 80%            |         | 487     |         | ps    |
| odc                  | Output Duty Cycle                      |                       |         | 50      |         | %     |
| $t_{EN}$             | Output Enable Time; NOTE 5             |                       |         |         | 10      | ns    |
| $t_{DIS}$            | Output Disable Time; NOTE 5            |                       |         |         | 8       | ns    |

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6D. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                              | Test Conditions       | Minimum | Typical | Maximum | Units |
|----------------------|--|-----------------------|---------|---------|---------|-------|
| $f_{MAX}$            | Output Frequency                       | w/External XTAL       | 10      |         | 40      | MHz   |
|                      |  | w/External CLK        |         | 200     |         | MHz   |
| $t_{pLH}$            | Propagation Delay, Low-to-High; NOTE 1 |                       |         | 2.3     |         | ns    |
| $t_{sk(o)}$          | Output Skew; NOTE 2                    |                       |         | TBD     |         | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 2, 3           |                       |         | TBD     |         | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 2, 4    | 25MHz, (100Hz - 1MHz) |         | 0.29    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                  | 20% to 80%            |         | 470     |         | ps    |
| odc                  | Output Duty Cycle                      |                       |         | 50      |         | %     |
| $t_{EN}$             | Output Enable Time; NOTE 5             |                       |         |         | 10      | ns    |
| $t_{DIS}$            | Output Disable Time; NOTE 5            |                       |         |         | 8       | ns    |

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.



**TABLE 6E. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                              | Test Conditions       | Minimum | Typical | Maximum | Units |
|----------------------|--|-----------------------|---------|---------|---------|-------|
| $f_{MAX}$            | Output Frequency                       | w/External XTAL       | 10      |         | 40      | MHz   |
|                      |  | w/External CLK        |         | 200     |         | MHz   |
| $t_{pLH}$            | Propagation Delay, Low-to-High; NOTE 1 |                       |         | 2.6     |         | ns    |
| $t_{sk(o)}$          | Output Skew; NOTE 2                    |                       |         | TBD     |         | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 2, 3           |                       |         | TBD     |         | ps    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 2, 4    | 25MHz, (100Hz - 1MHz) |         | 0.3     |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                  | 20% to 80%            |         | 518     |         | ps    |
| odc                  | Output Duty Cycle                      |                       |         | 50      |         | %     |
| $t_{EN}$             | Output Enable Time; NOTE 5             |                       |         |         | 10      | ns    |
| $t_{DIS}$            | Output Disable Time; NOTE 5            |                       |         |         | 8       | ns    |

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

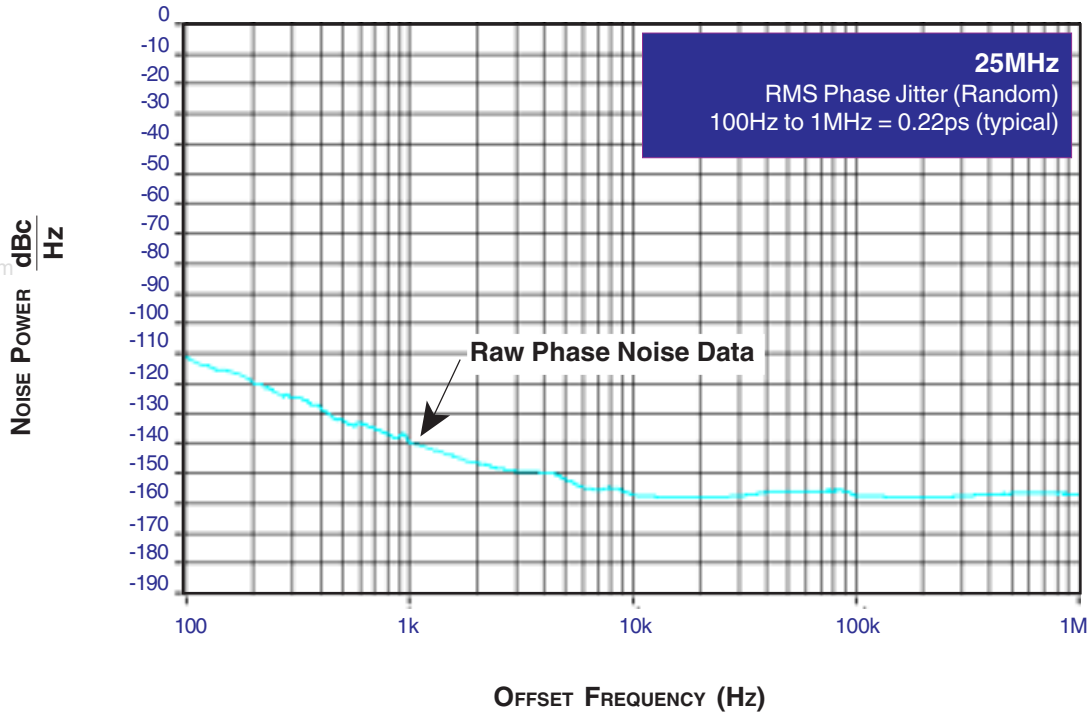
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.



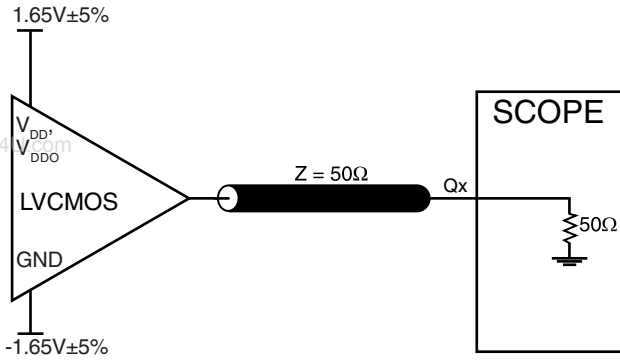
**TYPICAL PHASE NOISE AT 25MHz @ 3.3V**



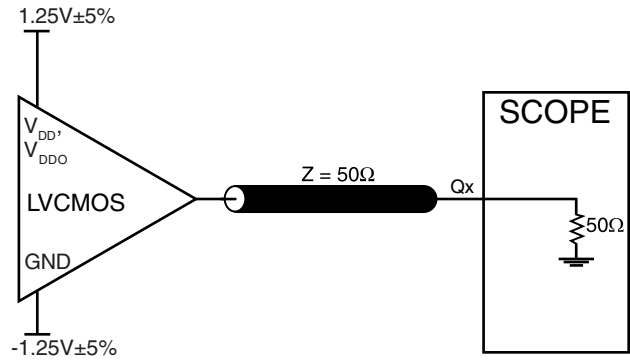




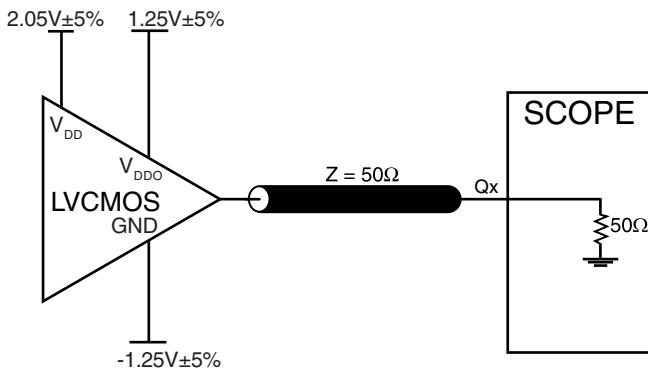
**PARAMETER MEASUREMENT INFORMATION**



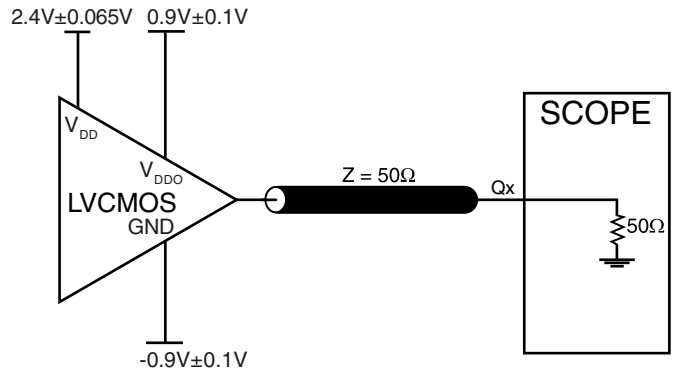
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



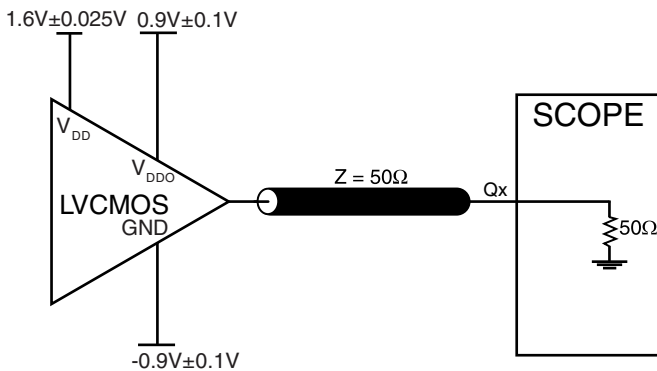
**2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



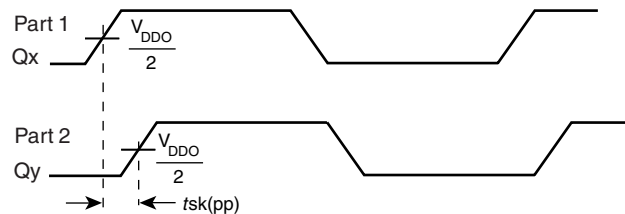
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



**3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT**



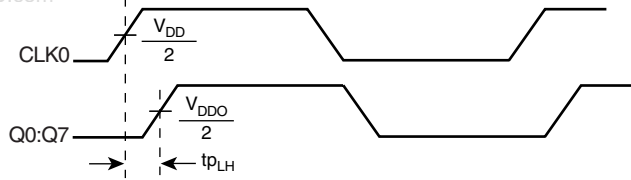
**2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT**



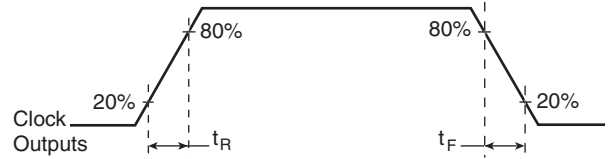
**PART-TO-PART SKEW**



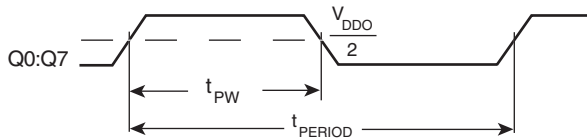
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**PROPAGATION DELAY**



**OUTPUT RISE/FALL TIME**



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

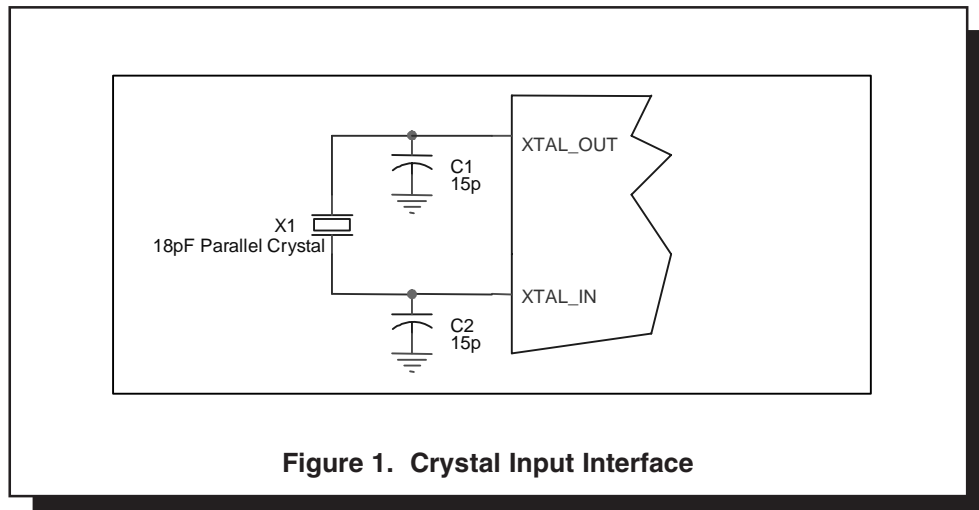


## APPLICATION INFORMATION

### CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS83908-02 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate fre-

quencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 1*. Typical results using parallel 18pF crystals are shown in Table 5.



### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_IN to ground.

##### CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

##### SELECT PINS:

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.



**RELIABILITY INFORMATION**

**TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 24 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) |        |        |        |
|---|--------|--------|--------|
|   | 0      | 1      | 2.5    |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 70°C/W | 65°C/W | 62°C/W |

**TRANSISTOR COUNT**

The transistor count for ICS83908-02 is: 277



PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

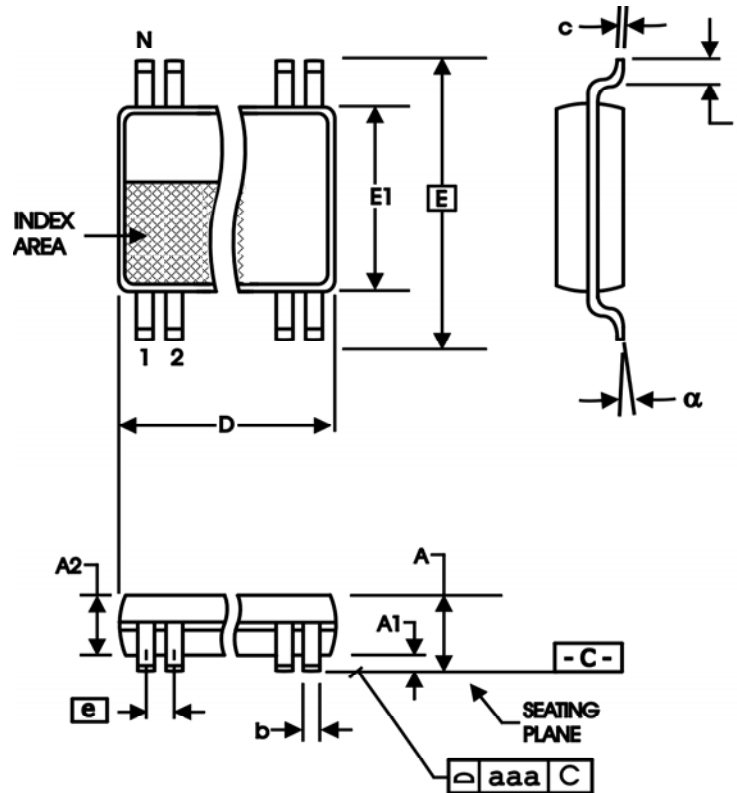


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |         |
|----------|-------------|---------|
|          | Minimum     | Maximum |
| N        | 24          |         |
| A        | --          | 1.20    |
| A1       | 0.05        | 0.15    |
| A2       | 0.80        | 1.05    |
| b        | 0.19        | 0.30    |
| c        | 0.09        | 0.20    |
| D        | 7.70        | 7.90    |
| E        | 6.40 BASIC  |         |
| E1       | 4.30        | 4.50    |
| e        | 0.65 BASIC  |         |
| L        | 0.45        | 0.75    |
| $\alpha$ | 0°          | 8°      |
| aaa      | --          | 0.10    |

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS83908-02**

LOW SKEW, 1-TO-8

CRYSTAL-TO-LVCMOS/LVTTL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking       | Package       | Shipping Packaging | Temperature |
|-------------------|---------------|---------------|--------------------|-------------|
| ICS83908AG-02     | ICS83908AG-02 | 24 Lead TSSOP | tube               | 0°C to 70°C |
| ICS83908AG-02T    | ICS83908AG-02 | 24 Lead TSSOP | 2500 tape & reel   | 0°C to 70°C |

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