Integrated Circuit Systems, Inc.

ICS839893I

LOW SKEW, 1-TO-13 LVCMOS/LVTTL BUFFER DIVIDER

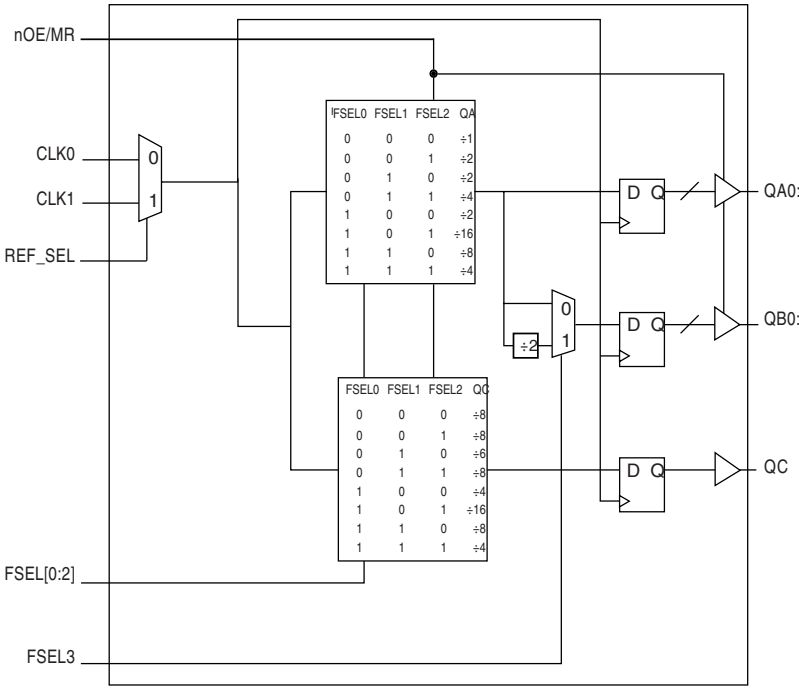
GENERAL DESCRIPTION

The ICS839893I is a high-performance one to thirteen LVCMOS/LVTTL buffer/divider and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The device has two selectable LVCMOS/LVTTL clock inputs and it generates 13 new LVCMOS/LVTTL clock outputs. The first bank of six outputs offers divide-by-1, 2, 4, 8 or 16. The second bank of six outputs can be configured to the same divide ratio as the first bank, or with an additional divide-by-two. The first two banks can be placed into a high-impedance output state with the assertion of a LOW on the nOE/MR input. One additional output can be configured to divide-by-4, 6, 8 or 16. This device is functional with full 3.3V or full 2.5V supplies.

FEATURES

- 13 LVCMOS/LVTTL outputs: 3 banks (6, 6, 1 outputs per bank respectively)
- Selectable CLK0 or CLK1 LVCMOS/LVTTL clock inputs
- CLK0, CLK1 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 40ps (maximum), within bank
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both, Standard and RoHS/Lead-Free compliant packages

SIMPLIFIED BLOCK DIAGRAM



PIN ASSIGNMENT

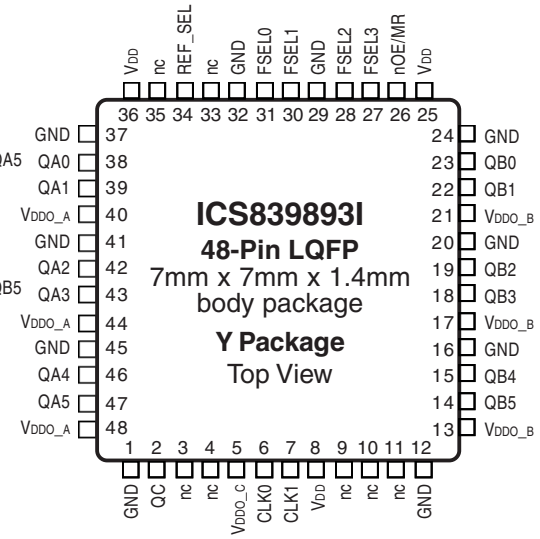


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12, 16, 20, 24, 29, 32, 37, 41, 45	GND	Power		Supply ground.
2	QC	Output		Bank C output. LVCMOS / LVTTL interface levels.
3, 4, 9, 10, 11, 33, 35	nc	Unused		No connect.
5	V_{DDO_C}	Power		Output supply pin for Bank C output.
6, 7	CLK0, CLK1	Input	Pulldown	LVCMOS / LVTTL clock inputs.
8, 25, 36	V_{DD}	Power		Core supply pins.
13, 17, 21	V_{DDO_B}	Power		Output supply pins for Bank B outputs.
14, 15, 18, 19, 22, 23	QB5, QB4 QB3, QB2 QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels.
26	nOE/MR	Input	Pulldown	Active High Master Reset. Active Low Output Enable. When logic LOW, the internal dividers and the outputs are enabled. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). LVCMOS / LVTTL interface levels.
27, 28, 30, 31	FSEL3, FSEL2, FSEL1, FSEL0	Input	Pulldown	Clock frequency selection and configuration of clock divider modes. LVCMOS / LVTTL interface levels.
34	REF_SEL	Input	Pulldown	Selects the primary reference clock. When LOW, selects CLK0 as the primary clock source. When HIGH, selects CLK1 as the primary clock source. LVCMOS / LVTTL interface levels.
38, 39 42, 43, 46, 47	QA0, QA1, QA2, QA3, QA4, QA5	Output		Bank A outputs. LVCMOS / LVTTL interface levels.
40, 44, 48	V_{DDO_A}	Power		Output supply pins for Bank A outputs.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DD} = V_{DDA} = V_{DDO\_x}$ = 3.465V		9		pF
		$V_{DD} = V_{DDA} = V_{DDO\_x}$ = 2.625V		9		pF
R_{OUT}	Ouput Impedance			14		Ω

NOTE: V_{DDO_X} denotes V_{DDO_A}, V_{DDO_B}, $V_{DDO—C.}$

TABLE 3. CLOCK FREQUENCY FUNCTION TABLE

Inputs				fREF Range (MHz)	Outputs		
					QAx	QBx	QC
FSEL0	FSEL1	FSEL2	FSEL3		fQAx (MHz)	fQBx (MHz)	fQC0 (MHz)
0	0	0	0	DC - 250	fREF ÷ 1	fREF ÷ 1	fREF ÷ 8
0	0	0	1			fREF ÷ 2	
0	0	1	0	DC - 250	fREF ÷ 2	fREF ÷ 2	fREF ÷ 8
0	0	1	1			fREF ÷ 4	
0	1	0	0	DC - 250	fREF ÷ 2	fREF ÷ 2	fREF ÷ 6
0	1	0	1			fREF ÷ 4	
0	1	1	0	DC - 250	fREF ÷ 4	fREF ÷ 4	fREF ÷ 8
0	1	1	1			fREF ÷ 8	
1	0	0	0	DC - 250	fREF ÷ 2	fREF ÷ 2	fREF ÷ 4
1	0	0	1			fREF ÷ 4	
1	0	1	0	DC - 250	fREF ÷ 16	fREF ÷ 16	fREF ÷ 16
1	0	1	1			fREF ÷ 32	
1	1	0	0	DC - 250	fREF ÷ 8	fREF ÷ 8	fREF ÷ 8
1	1	0	1			fREF ÷ 16	
1	1	1	0	DC - 250	fREF ÷ 4	fREF ÷ 4	fREF ÷ 4
1	1	1	1			fREF ÷ 8	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO_X} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A}, V_{DDO_B}, V_{DDO_C}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				155	mA
I_{DDO_A}, I_{DDO_B}, I_{DDO_C}	Output Supply Current				20	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C}$ = 2.5±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO_A}, V_{DDO_B}, V_{DDO_C}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				150	mA
I_{DDO_A}, I_{DDO_B}, I_{DDO_C}	Output Supply Current				20	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, nOE/MR, REF_SEL FSEL0:FSEL3	$V_{DD} = V_{IN}$ = 3.465V			200	µA
I_{IL}	Input Low Current	CLK0, CLK1, nOE/MR, REF_SEL FSEL0:FSEL3	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

Note 1: Outputs terminated with 50Ω to V_{DDO_x}/2. See Parameter Measurement Information, 3.3V Output Load Test Circuit diagram.

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, nOE/MR, REF_SEL FSEL0:FSEL3	$V_{DD} = V_{IN}$ = 2.625V			200	µA
I_{IL}	Input Low Current	CLK0, CLK1, nOE/MR, REF_SEL FSEL0:FSEL3	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

Note 1: Outputs terminated with 50Ω to V_{DDO_x}/2. See Parameter Measurement Information, 2.5V Output Load Test Circuit diagram.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			DC		250	MHz
f_{REF}	Input Frequency			DC		250	MHz
t_{PD}	Propagation Delay;NOTE 1			4.5		6.5	ns
*t*sk(o)	Output Skew; NOTE 2	within bank				40	ps
		bank-to-bank	Excludes QC			115	ps
		any output to QC				465	ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	250		600	ps
t_{PZL}, t_{PZH}	Output Enable Time					10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					10	ns
odc	Output Duty Cycle			47		53	%

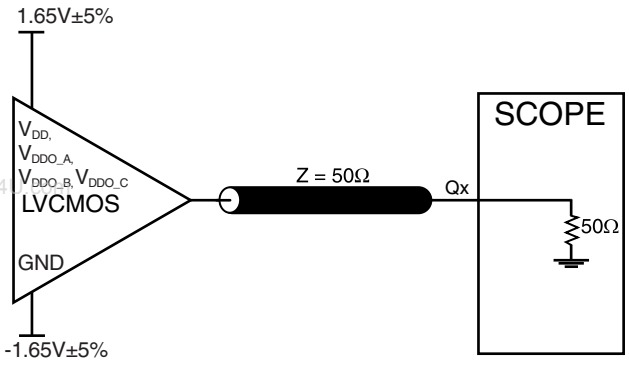
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ output crossing point.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C} = 2.5V±5\%$, T_A = -40°C TO 85°C

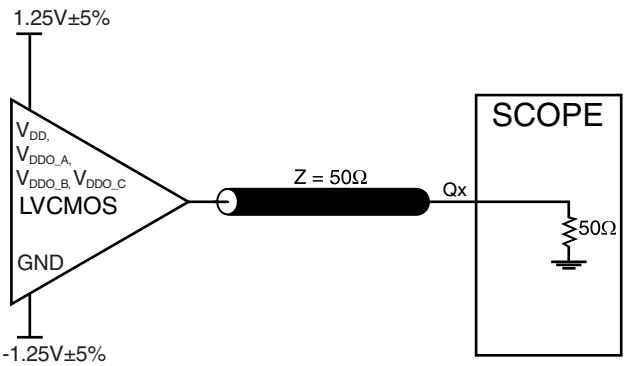
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			DC		250	MHz
f_{REF}	Input Frequency			DC		250	MHz
t_{PD}	Propagation Delay; NOTE 1			5		7	ns
*t*sk(o)	Output Skew; NOTE 2	within bank				40	ps
		bank-to-bank	Excludes QC			110	ps
		any output to QC				410	ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	250		600	ps
t_{PZL}, t_{PZH}	Output Enable Time					10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					10	ns
odc	Output Duty Cycle			47		53	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ output crossing point.

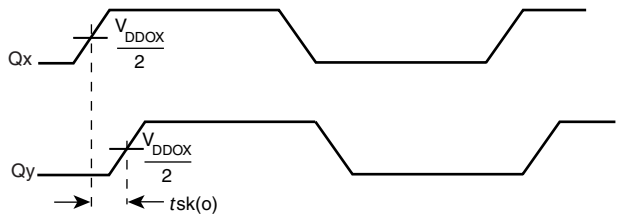
PARAMETER MEASUREMENT INFORMATION



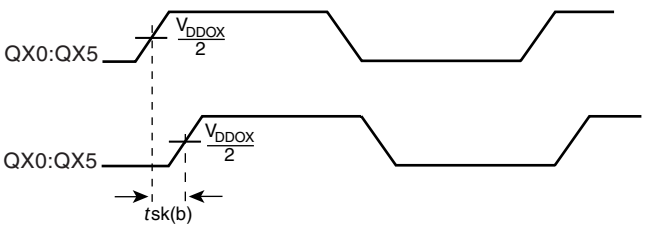
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



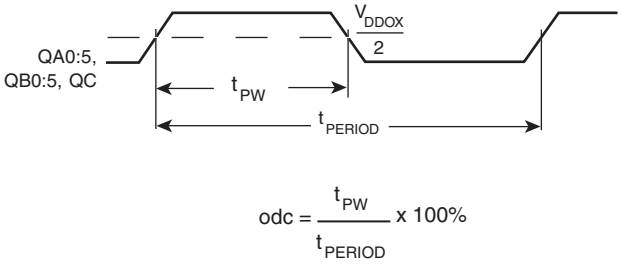
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



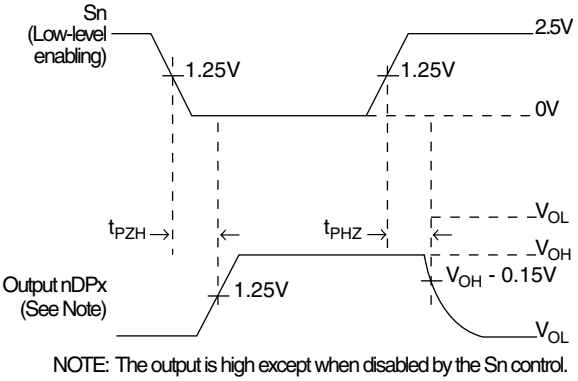
OUTPUT SKEW



BANK SKEW (where X denotes outputs in the same bank)

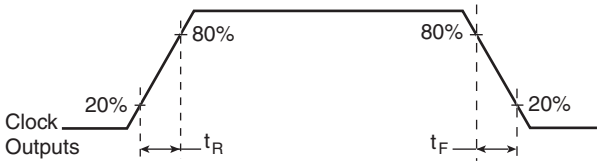


OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

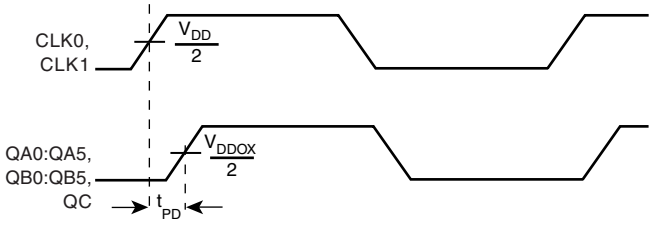


NOTE: The output is high except when disabled by the Sn control.

OUTPUT ENABLE/DISABLE TIME



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from the CLK input to ground.

CONTROL PINS:
All control pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resister can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS839893I is: 4615

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

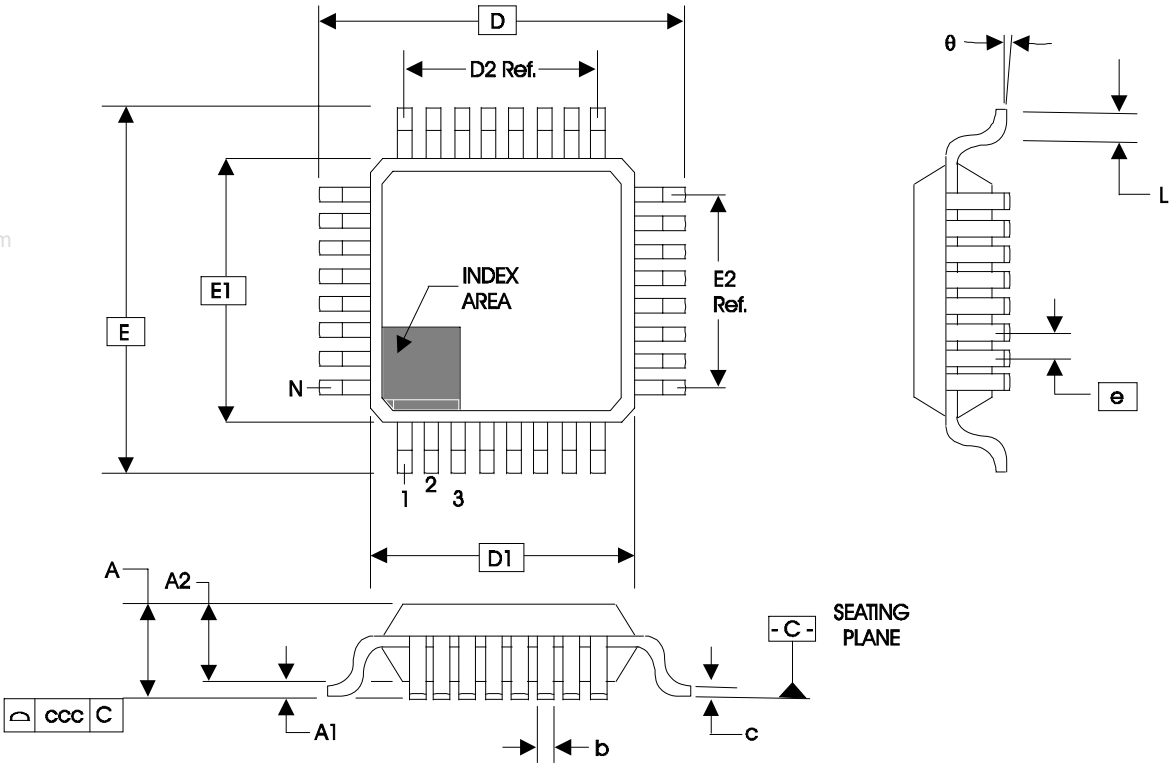


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS839893AYI	ICS839893AYI	48 Lead LQFP	tray	-40°C to 85°C
ICS839893AYIT	ICS839893AYI	48 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS839893AYILF	TBD	48 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS839893AYILFT	TBD	48 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.