PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840022

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS840022 is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840022 uses a 25MHz crystal to synthesize 125MHz or 62.5MHz. The ICS840022 has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS840022 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 LVCMOS/LVTTL output, 7Ω output impedence
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequencies: 125MHz or 62.5MHz (selectable)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.55ps (typical)
- RMS phase noise at 125MHz:

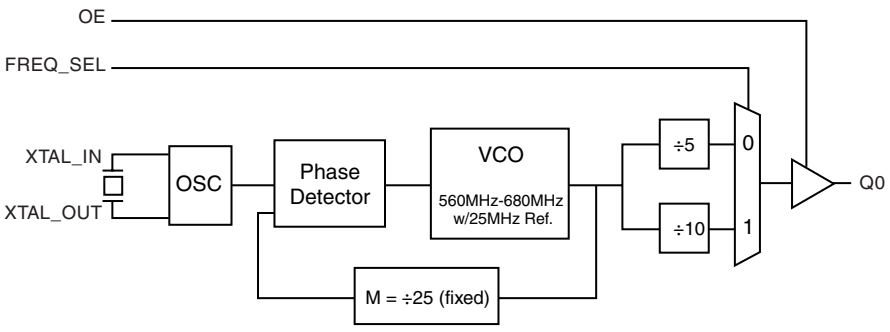
Offset	Noise Power
100Hz	-106.3 dBc/Hz
1KHz	-126.3 dBc/Hz
10KHz	-131.7 dBc/Hz
100KHz	-130.8 dBc/Hz

- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

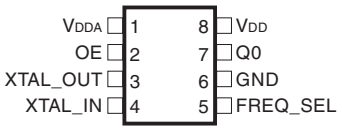
FUNCTION TABLE

Inputs	Output Frequencies
FREQ_SEL	(with a 25MHz crystal)
0	125MHz
1	62.5MHz

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840022

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	OE	Input	Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to HiZ state. LVCMOS/LVTTL interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 7Ω output impedence.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA} = 3.465V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			15		Ω

TABLE 3. CONROL FUNCTION TABLE

Control Inputs	Output
OE	**Q0**
0	Hi-Z
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			45		mA
I_{DDA}	Analog Supply Current			8		

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
		FREQ_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		FREQ_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

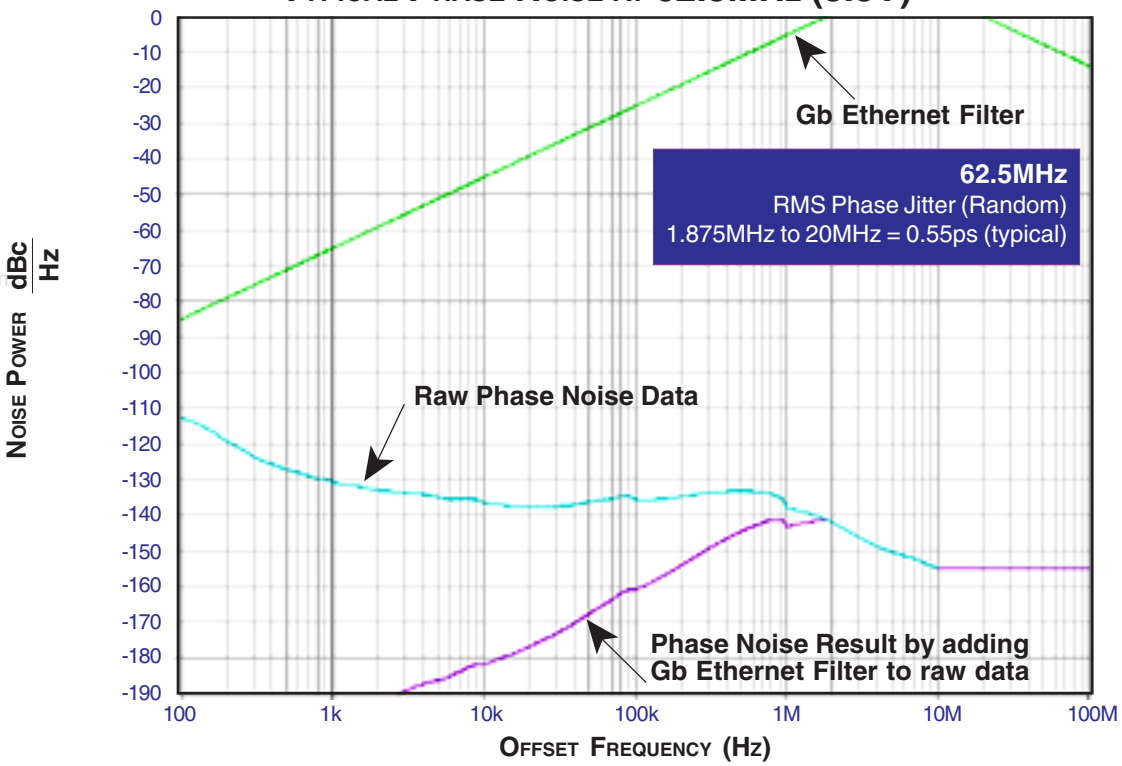
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

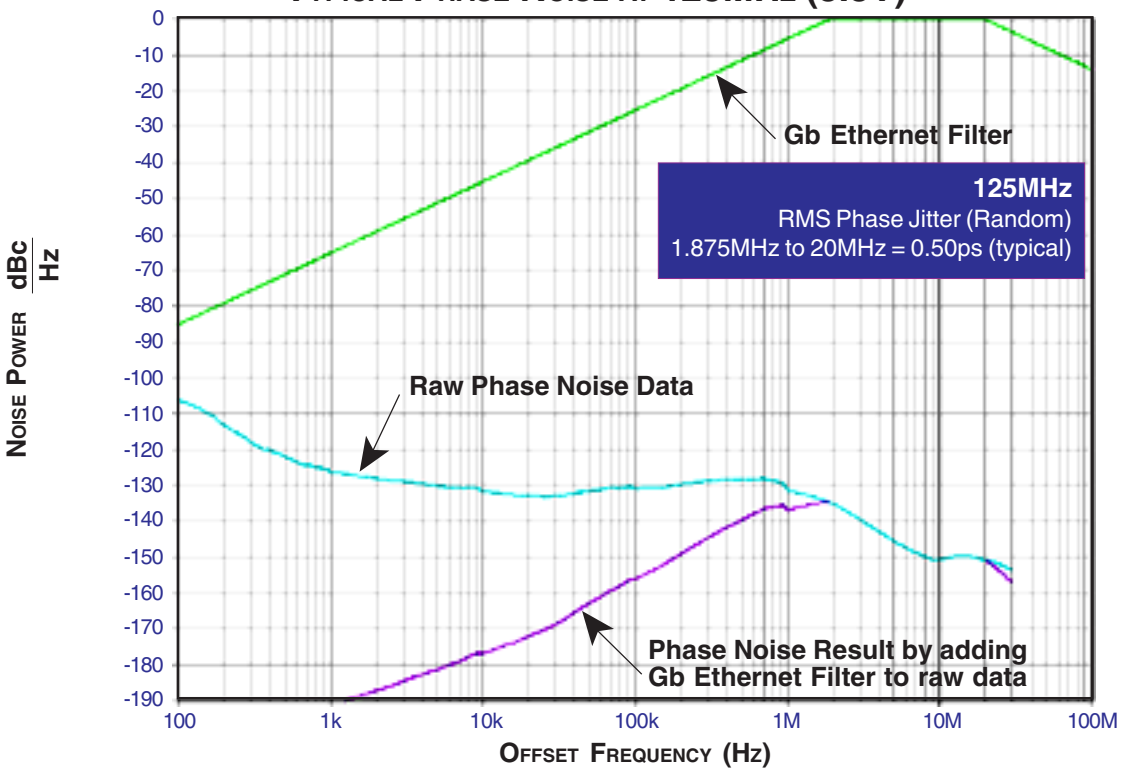
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
				62.5		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1	125MHz, (Intergration Range: 1.875MHz - 20MHz)		0.55		ps
		62.5MHz, (Intergration Range: 1.875MHz - 20MHz)		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plot.

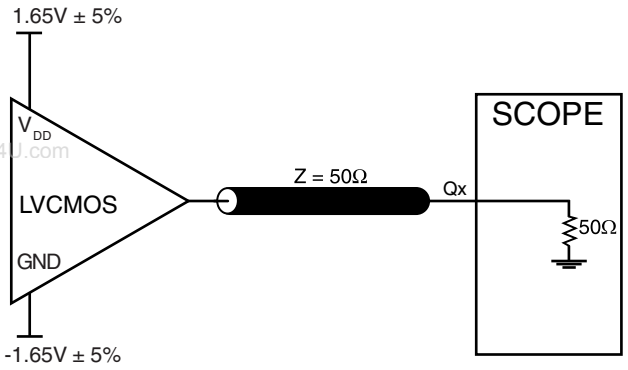
TYPICAL PHASE NOISE AT 62.5MHZ (3.3V)



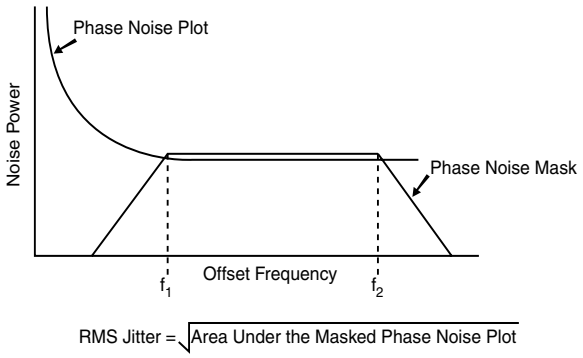
TYPICAL PHASE NOISE AT 125MHZ (3.3V)



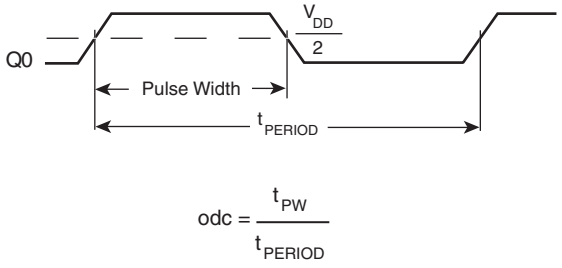
PARAMETER MEASUREMENT INFORMATION



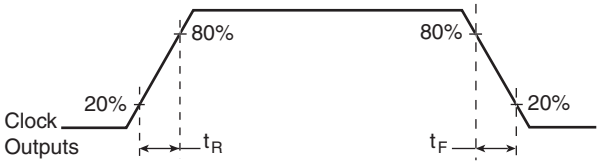
3.3V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840022 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

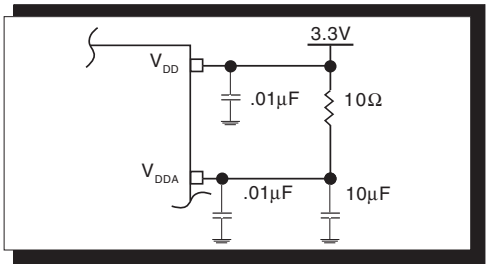


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840022 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

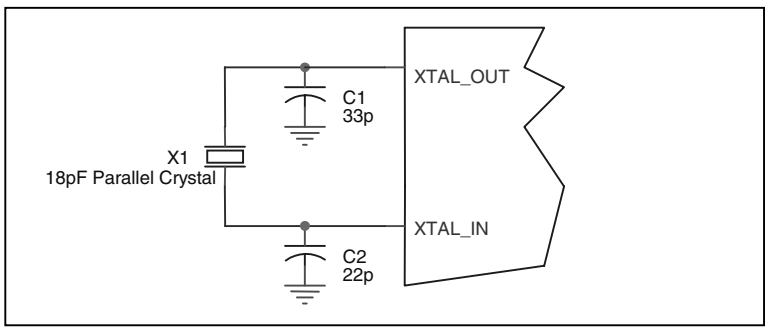


Figure 2. CRYSTAL INPUT INTERFACE

APPLICATION SCHEMATIC

Figure 3A shows a schematic example of the ICS840022. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz output frequency. The C1 = 22pF and C2pF = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

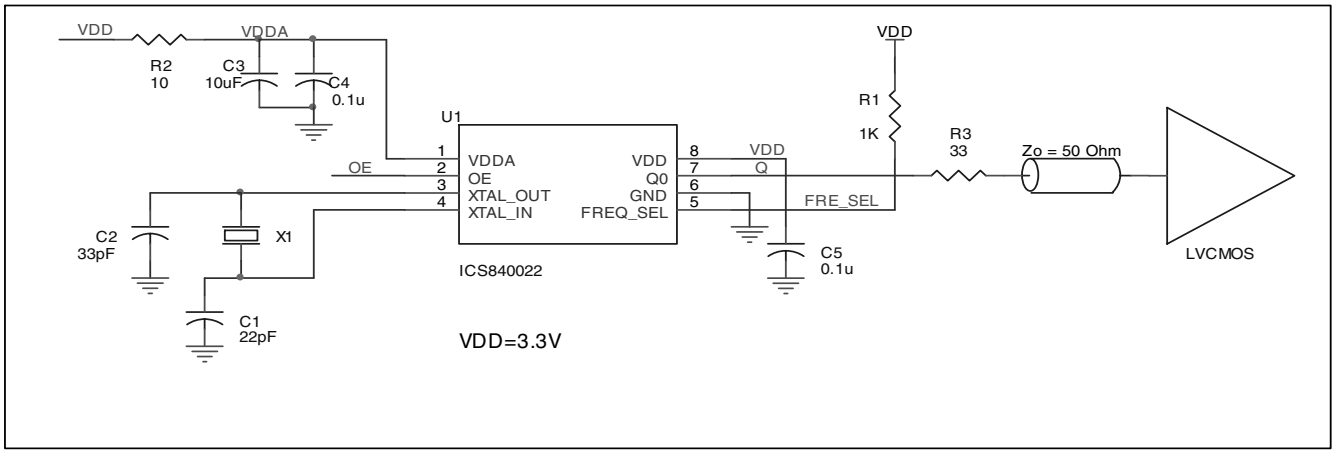


FIGURE 3A. ICS840022 SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of ICS840022 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 7.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

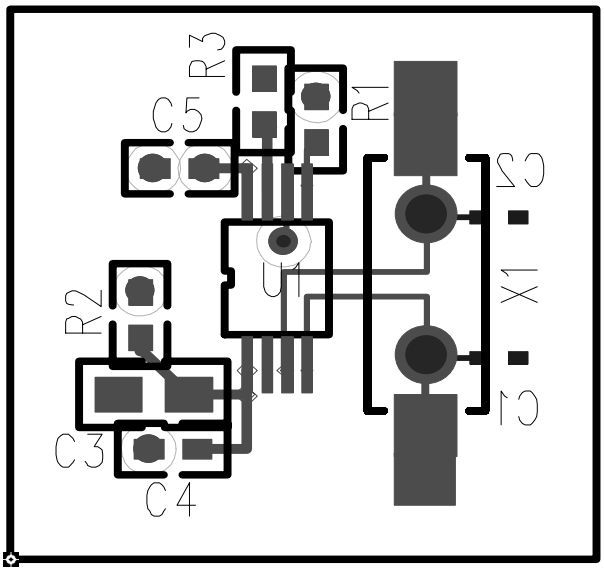


FIGURE 3B. ICS840022 PC BOARD LAYOUT EXAMPLE

TABLE 7. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R1, R2, R3	0603

NOTE: Table 7, lists component sizes shown in this layout example.

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS840022 is: 1984

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

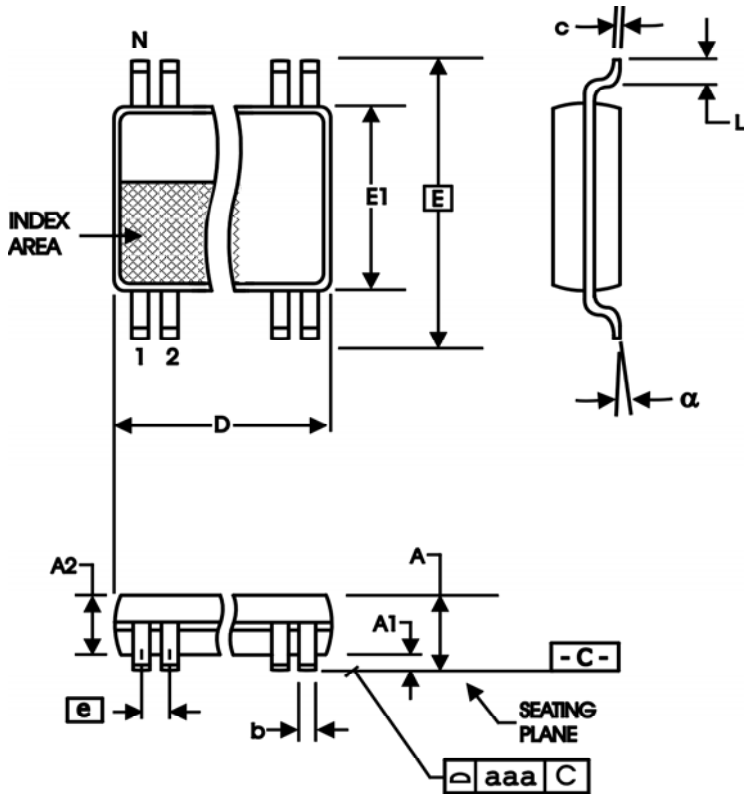


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS840022AG	0022A	8 lead TSSOP	tube	0°C to 70°C
ICS840022AGT	0022A	8 lead TSSOP	2500 tape & reel	0°C to 70°C