DATA SHEET

General Description

The ICS8430002 is a general purpose, high-performance, fractional-n LVPECL frequency synthesizer which can generate frequencies for a wide variety of applications with output frequency step sizes of <10ppm. The ICS8430002 has a 2:1 input Multiplexer from which either a crystal input or a differential input can be selected. The differential input can be wired to accept single-ended signals (see the applications section of this datasheet).

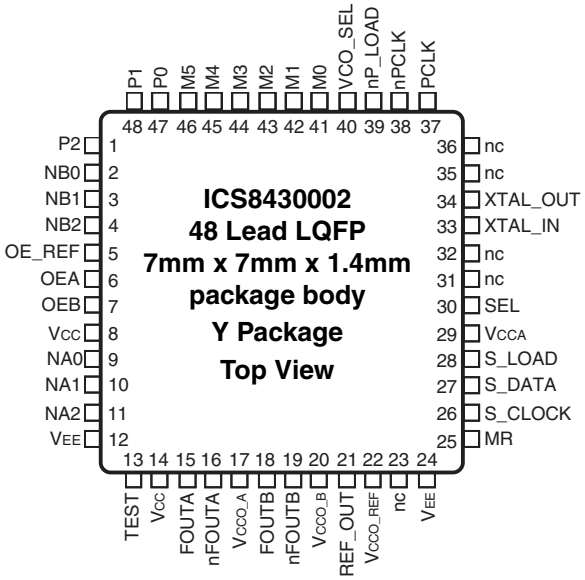
Each of the differential LVPECL outputs has an output divider which can be independently set so that two different frequencies can be generated. Additionally, each LVPECL output pair has a dedicated power supply pin so the outputs can run at 3.3V or 2.5V. The ICS8430002 also supplies a buffered copy of the reference clock or crystal frequency on the single-ended REF_OUT pin which can be enabled or disabled (disabled by default). The output frequency can be programmed using either a serial or parallel programming interface.

The device features a fractional feedback divider with a 6-bit integer and 12-bit fractional value. The minimum step value of the feedback divider is 1/4096.

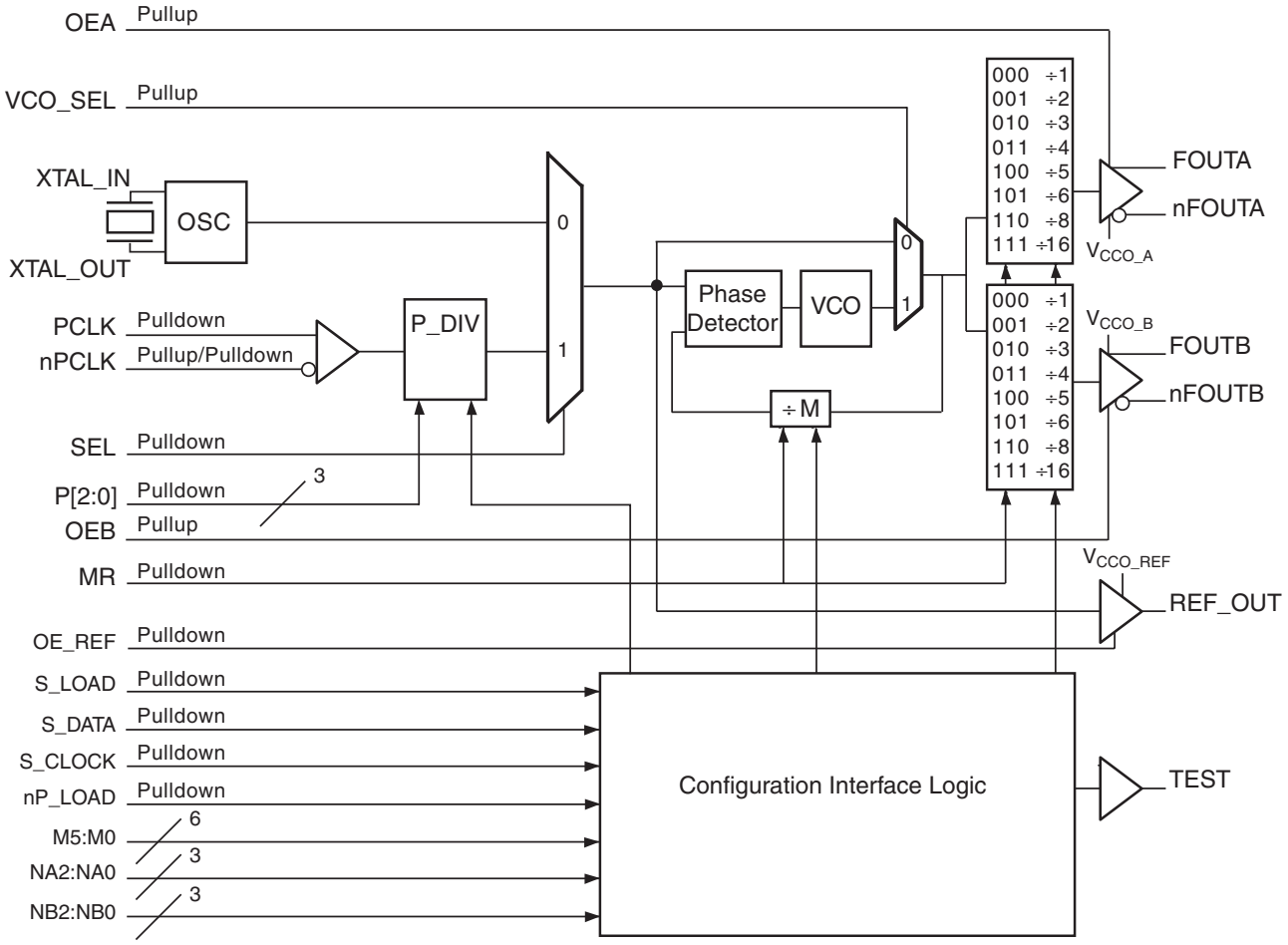
Features

- 6-Bit Integer and 12-Bit Fractional Feedback Divider
- Dual differential 3.3V LVPECL outputs which can be set independently for either 3.3V or 2.5V
- 2:1 Input Mux:
  One differential input
  One crystal oscillator interface
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Output frequency range: 30.625MHz to 640MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 490MHz to 650MHz
- Parallel or serial interface for programming feedback divider and output dividers
- Supply voltage modes:
  Core/Outputs:
  3.3V/3.3V
  3.3V/2.5V
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



Block Diagram



Functional Description

NOTE: The functional description that follows describes the operation using a 25MHz crystal or clock input. Valid PLL loop divider values for different crystal or clock input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1 and NOTE 2. When a crystal is being used, there is no pre-divider therefore set P = 1 when referencing all following equations on this page.

The ICS8430002 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. It has a 2:1 multiplexer from which either a crystal input or a differential input can be selected.

An external fundamental-mode quartz crystal can be used as the input to the on-chip crystal oscillator. The range of allowable crystal frequencies is 12MHz to 40MHz. When selected, the crystal frequency is the reference frequency input to the phase detector. The relationship between the VCO frequency, the crystal input frequency and the M divider (M) is as follows:

$$F_{VCO} = XTAL \times M$$

A differential input clock can also be used. (See the Application Information section for *Wiring the Differential Input to Accept Single-Ended Levels.*) The differential input is followed by a pre-divider that divides down the clock input frequency. This allows an equal or lower reference frequency for the phase detector. See Table 3C for available pre-divider values. The pre-divider value is set through the P[2:0] pins or by using the serial programming interface. The output frequency of the pre-divider is the reference frequency input to the phase detector. The input frequency range of the phase detector is 9MHz to 50MHz. The relationship between the VCO frequency, the clock input frequency, the pre-divider (P) and the M divider (M) is as follows:

$$F_{VCO} = \frac{F_{IN}}{P} \times M$$

Input Min (MHz)	Input Max (MHz)	Pre-Divider
9	50	÷1
18	100	÷2
36	200	÷4
45	250	÷5
72	400	÷8
144	800	÷16
225	800	÷25
288	800	÷32

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. The VCO of the PLL operates over a range of 490MHz to 650MHz. Note that for some values of M (either too high or too low), the PLL will not achieve lock.

Using a 25MHz input, the M value integer-only range is shown in Table 3B, *Programmable VCO Frequency Table, P = ÷1*. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $19.6 \leq M \leq 25.6$. For different reference frequencies, the range of valid M values may be calculated as follows:

$$\frac{490MHz}{F_{IN}/P} \leq M \leq \frac{650MHz}{F_{IN}/P}$$

The output of the VCO is scaled by output dividers prior to being sent to each of the LVPECL output buffers. The output divider settings and output frequency ranges are shown in table 3D.

Combining all the values of input frequency, pre-divider setting, integer and fractional feedback divider settings, and output divider setting, the output frequency may be calculated. The frequency out is defined as follows:

$$F_{OUT} = \frac{F_{VCO}}{N} = \frac{F_{IN}}{P} \times \frac{M}{N}$$

The fractional-n M divider is composed of a 6-bit integer portion and a 12-bit fractional portion. The decimal value obtained from these settings can be determined as follows:

$$M = M_{INT} + \frac{M_{FRAC}}{4096}$$

Where:M_{INT} is the 6-bit integer portion

M_{FRAC} is the 12-bit fractional portion

For a given required M divider, the value to program into the M_{FRAC} register is calculated by taking the fractional portion and multiplying by 4096. For example, assuming a 25MHz crystal is being used, and the desired VCO frequency is 515.625 (to support ethernet with 64B/66B encoding) the feedback setting required would be 20.625. The integer portion of this number (20) is programed into the M_{INT} register. The fractional portion (0.625) is multiplied by 4096. The result (2560) is programmed into the M_{FRAC} register. The full M divider setting is then:

$$20 + \frac{2560}{4096} = 20.625$$

The frequency step size in ppm can be calculated using the following:

$$stepsize = \left|\frac{F_0 - F_1}{F_0}\right| \times 10^6 ppm$$

Substituting the combined equation $\frac{F_{IN}}{P} \times \frac{M}{N}$ for the F terms in the step size equation, the equation can be reduced to just the change in M values.

$$stepsize = \left|\frac{M_0 - M_1}{M_0}\right| \times 1 \times 10^6 ppm$$

Assuming a 25MHz reference frequency and a VCO frequency of 637.5MHz (which, with an output divider of 6 would give an output frequency of 106.25MHz, a common Fibre channel reference frequency), requires an M setting of 25.5 (the integer portion being 25 and the fractional portion being 2048/4096). If you decrease the fractional portion of the M divider by one bit (from 2048 to 2047), the frequency change in ppm is calculated by:

$$stepsize = \left| \frac{(25.5 - 25.499755859375)}{25.5} \right| \times 1 \times 10^{6} ppm$$

Which, for these conditions, is a step size of 9.6 ppm.

The ICS8430002 supports either serial or parallel programming modes to program the P pre-divider, M feedback divider and N output divider, however the parallel interface can only program the integer portion of the feedback divider. The fractional portion of the feedback divider must be programmed serially. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on the M, NA, and NB inputs are passed directly to the M divider and both N output dividers. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M and N dividers remain loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and Nx bits can be hardwired to set the M divider and Nx output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode.

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the P pre-divider, M divider and Nx output divider when S_LOAD transitions from LOW-to-HIGH. The P pre-divider, M divider and Nx output divider values are latched on the HIGH-to-LOW transition of S_LOAD. The serial mode can be used to program the P, M and Nx bits and test bits T1 and T0. The data bits are clocked in the following order as in the table below.

T1	T0	NB2	NB1	NB0	NA2	NA1	NA0	P2	P1	P0	DS1	DS0

. . .

$M_{FRAC}11$	$M_{FRAC}10$	$M_{FRAC}9$	$M_{FRAC}8$	$M_{FRAC}7$	$M_{FRAC}6$	$M_{FRAC}5$	$M_{FRAC}4$	$M_{FRAC}3$	$M_{FRAC}2$	$M_{FRAC}1$	$M_{FRAC}0$

. . .

$M_{INT}5$	$M_{INT}4$	$M_{INT}3$	$M_{INT}2$	$M_{INT}1$	$M_{INT}0$

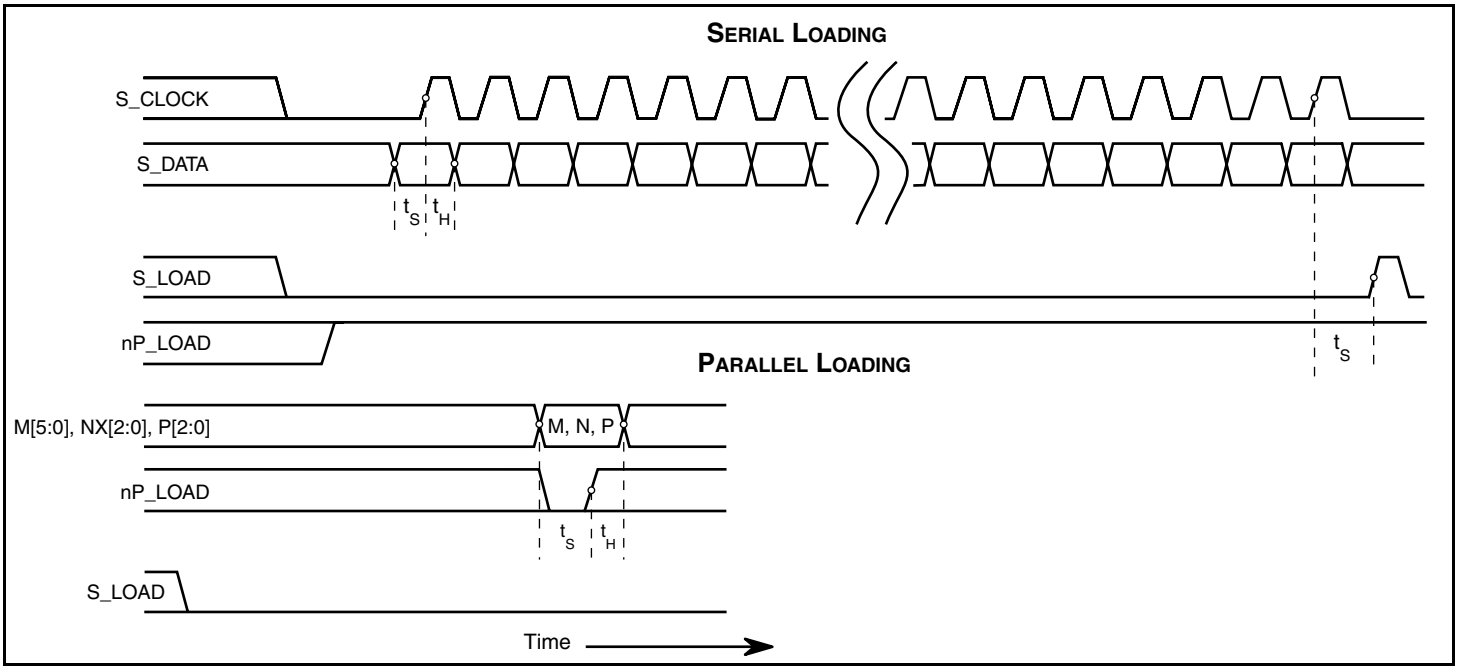


Figure 1. Parallel & Serial Load Operations

The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_DATA, Shift Register Output
1	0	Reserved
1	1	Reserved

The function of the DS1, and DS0 bits is as follows:

DS1	DS0	Function
0	0	Integer Mode Only
1	1	Fractional Mode Only
0	1	Do Not Use
1	0	Do Not Use

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 47, 48	P2, P0, P1	Input	Pulldown	Pre-divider control input pins. See table 3C. LVCMOS/LVTTL interface levels.
2, 3	NB0, NB1	Input	Pullup	Determines output divider value as defined in Table 3D, Function Table. LVCMOS/LVTTL interface levels.
4	NB2	Input	Pulldown	
5	OE_REF	Input	Pulldown	Output enable. Controls enabling and disabling of REF_OUT output. When HIGH, the output is active. When LOW, the output is high-impedance. LVCMOS/LVTTL interface levels.
6	OEA	Input	Pullup	Output enable. Controls enabling and disabling of FOUTA, nFOUTA outputs. When HIGH, the outputs are active. When LOW, the true output is low and the compliment output is high. LVCMOS/LVTTL interface levels.
7	OEB	Input	Pullup	Output enable. Controls enabling and disabling of FOUTB, nFOUTB outputs. When HIGH, the outputs are active. When LOW, the true output is low and the compliment output is high. LVCMOS/LVTTL interface levels.
8, 14	V_{CC}	Power		Core supply pins.
9, 10	NA0, NA1	Input	Pullup	Determines output divider value as defined in Table 3D, Function Table. LVCMOS/LVTTL interface levels.
11	NA2	Input	Pulldown	
12, 24	V_{EE}	Power		Negative supply pins.
13	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
15, 16	FOUTA, nFOUTA	Output		Differential output pair for the synthesizer. LVPECL interface levels.
17	V_{CCO_A}	Power		Output supply pin for FOUTA/nFOUTA LVPECL outputs.
18, 19	FOUTB, nFOUTB	Output		Differential output pair for the synthesizer. LVPECL interface levels.
20	V_{CCO_B}	Power		Output supply pin for FOUTB/nFOUTB LVPECL outputs.
21	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels.
22	V_{CCO_REF}	Power		Output supply pin for REF_OUT.
23, 31, 32, 35, 36	nc	Unused		No internal connection.
25	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When Logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels.
26	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.

continued on next page.

Number	Name	Type		Description
27	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
28	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
29	V_{CCA}	Power		Analog supply pin.
30	SEL	Input	Pulldown	Selects between the crystal oscillator or the PCLK/nPCLK inputs as the PLL reference source. Selects XTAL inputs when LOW. Selects PCLK/nPCLK when HIGH. LVCMOS/LVTTL interface levels.
33, 34	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
37	PCLK	Input	Pulldown	Non-inverting differential clock input.
38	nPCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
39	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M5:M0 is loaded into M divider, and when data present at NA2:NA0 and NB2:NB0 is loaded into the N output divider value. LVCMOS/LVTTL interface levels.
40	VCO_SEL	Input	Pullup	Determines whether the synthesizer is in PLL or Bypass mode. LVCMOS/LVTTL interface levels.
41, 42, 43, 44, 45	M0, M1, M2, M3, M4	Input	Pulldown	M divider integer inputs. The fractional portion of M divider can only be programmed by serial interface. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
46	M5	Input	Pullup	

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_OUT			7		Ω

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs							
MR	**nP_LOAD**	**M**	**N**	**S_LOAD**	**S_CLOCK**	**S_DATA**	**Conditions**
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input does not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table, P = ÷1

VCO Frequency (MHz)	M Divide	32	16	8	4	2	1
		M5	**M4**	**M3**	**M2**	**M1**	**M0**
500	20	0	1	0	1	0	0
•	•	•	•	•	•	•	•
550	22	0	1	0	1	1	0
•	•	•	•	•	•	•	•
625	25	0	1	1	0	0	1

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 25MHz.

Table 3C. Programmable Pre Divider Function Table

Inputs			
P2	**P1**	**P0**	**Pre Divider Value**
0	0	0	1 (default)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	5
1	1	1	25

Table 3D. Programmable Output Divider Function Table

Inputs			N Divider Value	Output Frequency (MHz)	
Nx2	**Nx1**	**Nx0**		**Minimum**	**Maximum**
0	0	0	1	490	640
0	0	1	2	245	325
0	1	0	3	163.33	216.67
0	1	1	4 (default)	122.5	162.5
1	0	0	5	98	130
1	0	1	6	81.67	108.33
1	1	0	8	61.25	81.25
1	1	1	16	30.625	40.625

NOTE: “x” denotes Bank A or Bank B.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, V_O (LVCMOS)	 50mA 100mA -0.5V to V_{CCO_REF} + 0.5V
Package Thermal Impedance, θ_{JA}	65.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = V_{CCO_REF} = 3.3V±5% or 2.5V±5%, V_{EE} =0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.13	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}, V_{CCO_REF}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				182	mA
I_{CCA}	Analog Supply Current				13	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, V_{CCO_REF} = 3.3V±5% or 2.5V±5%, V_{EE} =0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	P[2:0], NB2, NA2, MR, OE_REF, SEL, M[4:0], S_CLOCK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = V_{IN} = 3.465V			150	µA
		M5, NA[1:0], NB[1:0], VCO_SEL, OEA, OEB	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	P[2:0], NB2, NA2, MR, OE_REF, SEL, M[4:0], S_CLOCK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		M5, NA[1:0], NB[1:0], VCO_SEL, OEA, OEB	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	REF_OUT; NOTE 1	V_{CCO_REF} = 3.3V±%	2.6			V
			V_{CCO_REF} = 2.5V±5%	1.8			V
		TEST; NOTE 2	V_{CC} = 3.3V±%	2.6			V
V_{OL}	Output Low Voltage	REF_OUT; NOTE 1	V_{CCO_REF} = 3.3V±5% or 2.5V±5%			0.5	V
		TEST; NOTE 2	V_{CC} = 3.3V±%			0.5	V

NOTE 1: Output terminated with 50Ω to V_{CCO_REF}/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*
NOTE 2: Output terminated with 50Ω to V_{CC}/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4C. LVPECL DC Characteristics, V_{CC} =3.3V±5%, V_{CCO_A} = V_{CCO_B} = 3.3V±5% or 2.5V±5%,V_{EE} =0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK/nPCLK	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CCO} – 1.4		V_{CCO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CCO} – 2.0		V_{CCO} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to $V_{CCO\_A, \_B}$ – 2V.

Table 5. Input Frequency Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL_IN, XTAL_OUT; NOTE 1		12		40	MHz
		PCLK/nPCLK; NOTE 2		9		800	MHz
		S_CLOCK				40	MHz
t_R / t_F	Rise/Fall Time	S_CLOCK, S_DATA, S_LOAD			6		ns

$M = M_{INT} + M_{CALC}$. The M value must be set for the VCO range to operate within the 490MHz - 650MHz range.
When M_{FRAC} = 0, set bits DS1=0 and DS0 = 0

NOTE 1: Using the minimum crystal input frequency of 12MHz, valid values of M are 40.8333 ≤ M ≤ 54.1667. This means that M_{INT} has a range of 40 ≤ M_{INT} ≤ 54 assuming the M_{FRAC} is used to meet the requirement 40.8333 ≤ M ≤ 54.1667. When used, adjust M_{FRAC} to adjust the value of M according to the instructions on page 3. Using the maximum crystal input frequency of 40MHz, valid values of M are 12.25 ≤ M ≤ 16.25. This means that M_{INT} has a range of 12 ≤ M_{INT} ≤ 16.25 assuming the M_{FRAC} is used to meet the requirement 12.25 ≤ M ≤16.25. When used, adjust M_{FRAC} to adjust the value of M according to the instructions on page 3.

NOTE 2: Using the PCLK/nPCLK input frequency of 9MHz, when the pre-divider = 1, valid values of M are 54.4444 ≤ M_{INT} ≤ 58. This means that M_{INT} has a range of 54 ≤ M_{INT} ≤ 58 assuming the M_{FRAC} is used to meet the requirement 54.4444 ≤ M ≤ 58. M_{INT} must not be set higher than 58. Using the PCLK/nPCLK input frequency of 50MHz, when the pre-divider = 1, valid values of M are 10 ≤ M ≤ 13. This means that M_{INT} has a range of 10 ≤ M_{INT} ≤ 13 assuming the M_{FRAC} is used to meet the requirement 10 ≤ M ≤ 13. M_{INT} must not be set lower than 10.

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

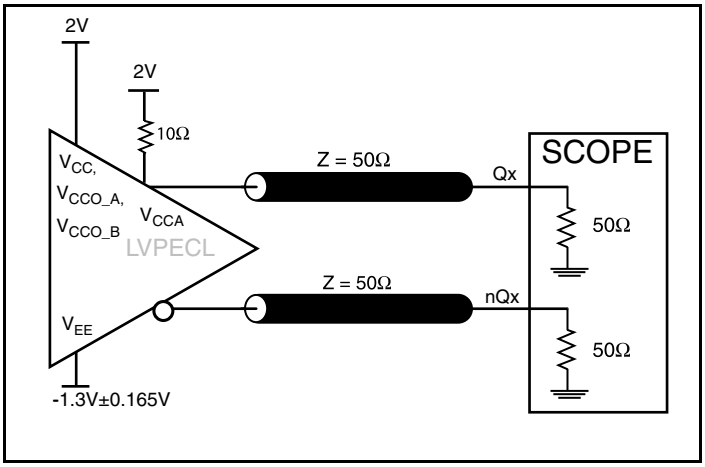
Table 7. AC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_REF}$ = 3.3V±5% or 2.5V±5%, V_{EE} =0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{PD}	Phase Detector Input Frequency			9		50	MHz
f_{VCO}	VCO Frequency			490		650	MHz
f_{OUT}	Output Frequency			30.625		640	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1		V_{IN} = 77.76MHz, V_{OUT} = 155.52MHz, Integer Mode is N = ÷4			60	ps
			V_{IN} = 77.76MHz, V_{OUT} = 194.4MHz, Integer Mode is N = ÷3			130	ps
			V_{IN} = 77.76MHz, V_{OUT} = 161.1322MHz, Frac-N Mode is N = ÷4			100	ps
			V_{IN} = 77.76MHz, V_{OUT} = 173.3714MHz, Frac-M Mode is N = ÷3			170	ps
*t*jit(per)	Period Jitter, RMS		V_{IN} = 77.76MHz, V_{OUT} = 155.52MHz, Integer Mode is N = ÷4			8	ps
			V_{IN} = 77.76MHz, V_{OUT} = 194.4MHz, Integer Mode is N = ÷3			5	ps
			V_{IN} = 77.76MHz, V_{OUT} = 161.1322MHz, Frac-N Mode is N = ÷4			18	ps
			V_{IN} = 77.76MHz, V_{OUT} = 173.3714MHz, Frac-M Mode is N = ÷3			6	ps
t_{DJ}	Deterministic Jitter		Output Divider = 3, M_{frac} = 0			100	ps
			Output Divider = 3, $M_{frac} \neq 0$			125	ps
*t*sk(o)	Output Skew; NOTE 1, 2					170	ps
t_R / t_F	Output Rise/Fall Time	FOUTx/nFOUTx	20% to 80%	200		700	ps
odc	Output Duty Cycle	FOUTx/nFOUTx	Output Divider = 1	40		60	%
		FOUTx/nFOUTx	Output Divider = 2	43		57	%
		FOUTx/nFOUTx	Output Divider ≠ 1, 2	46		54	%
t_{LOCK}	PLL Lock Time					200	ms

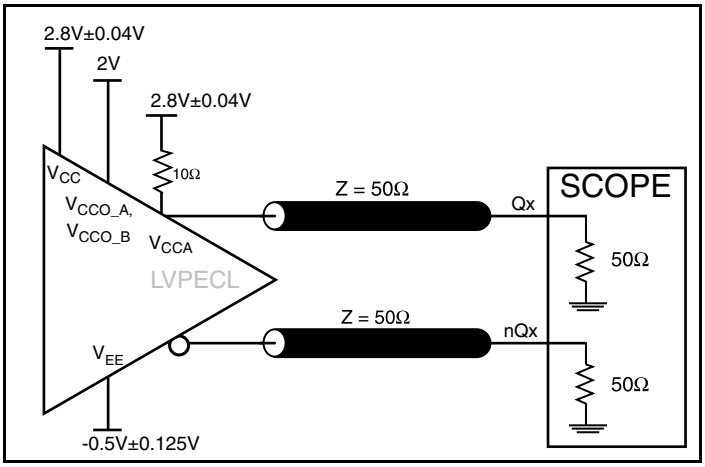
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: See Parameter Measurement Information section.

NOTE 1:This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

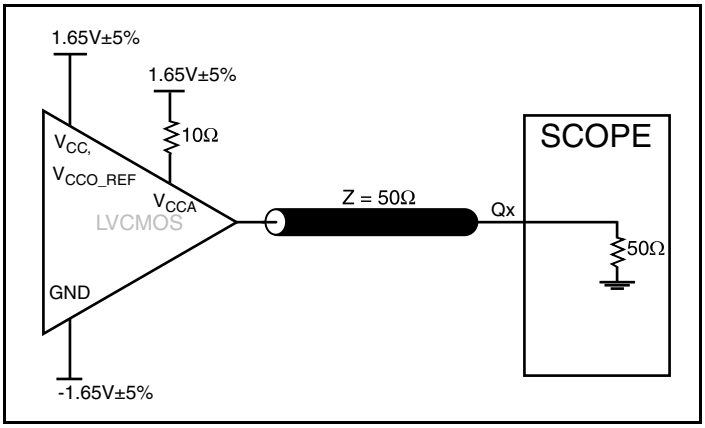
Parameter Measurement Information



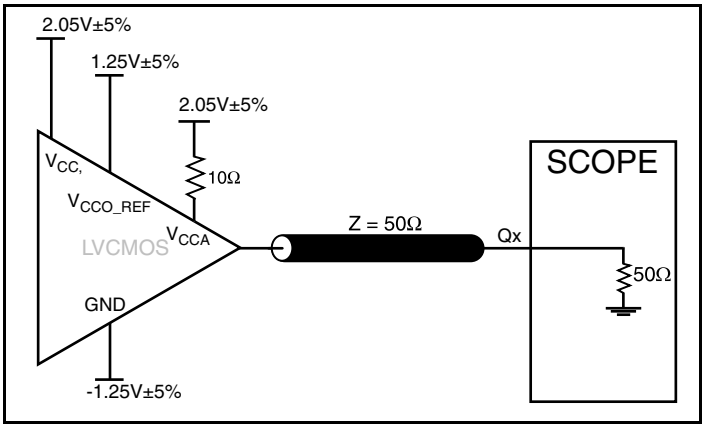
3.3/3.3V LVPECL Output Load AC Test Circuit



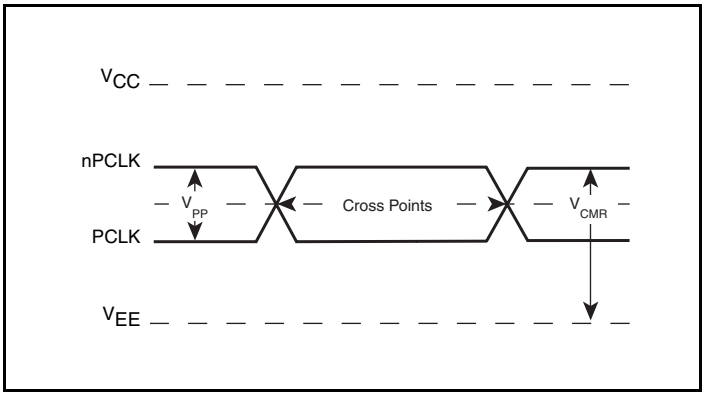
3.3V/2.5V LVPECL Output Load AC Test Circuit



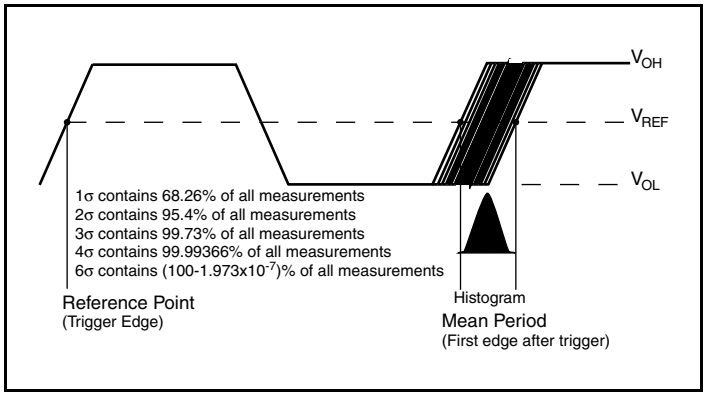
3.3/3.3V LVCMOS Output Load AC Test Circuit



3.3/2.5V LVCMOS Output Load AC Test Circuit

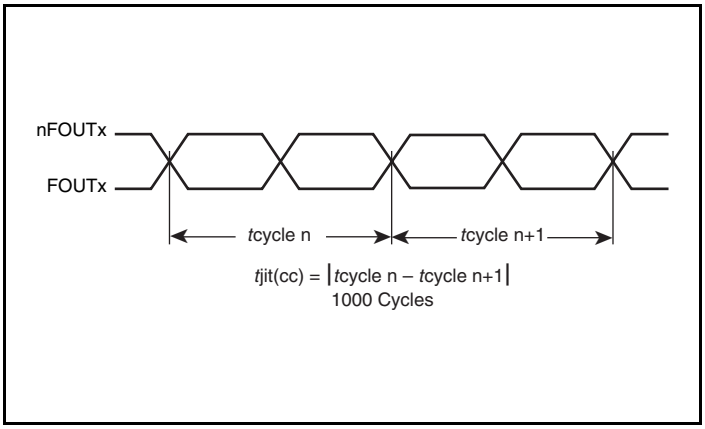


Differential Input Level

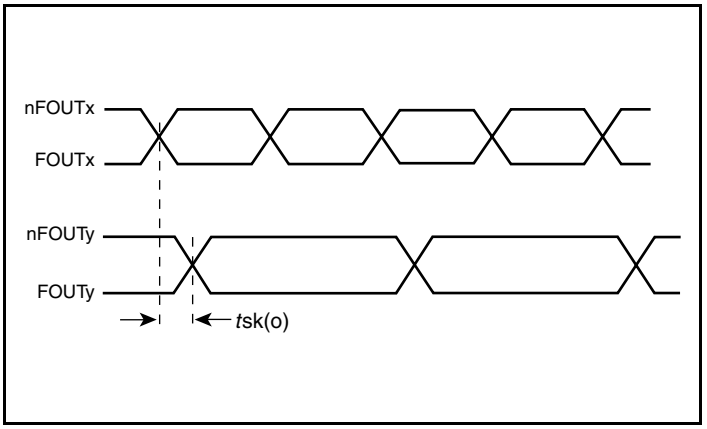


Period Jitter

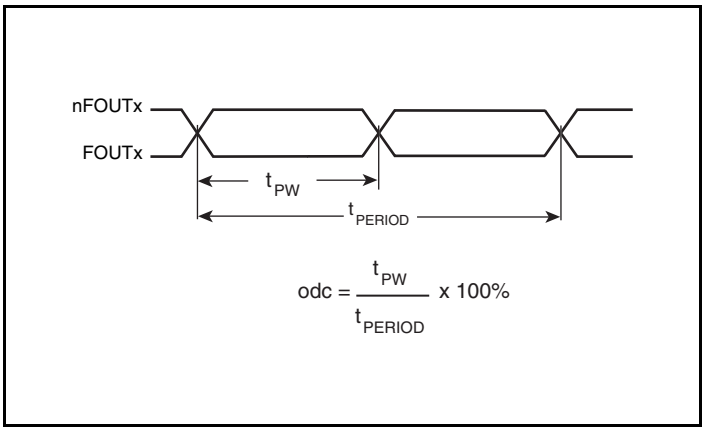
Parameter Measurement Information, continued



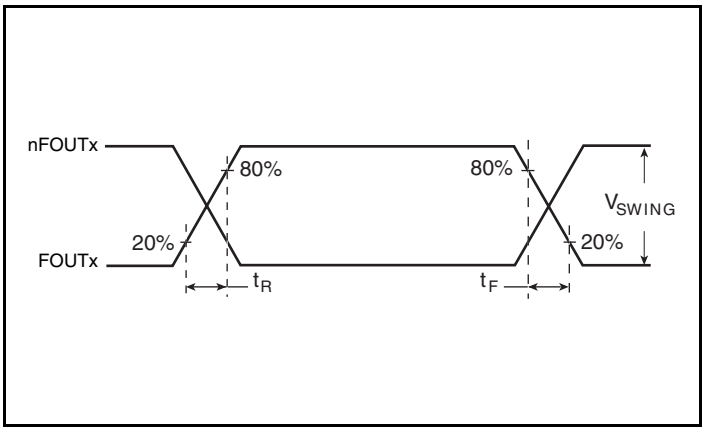
Cycle-to-Cycle Jitter



LVPECL Output Skew



LVPECL Output Duty Cycle/Pulse Width/Period



LVPECL Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8430002 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

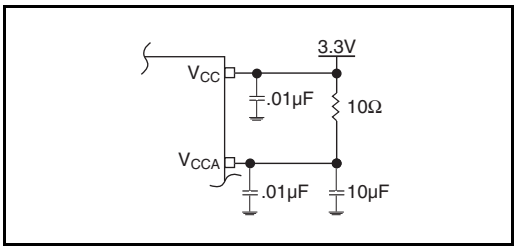


Figure 2. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

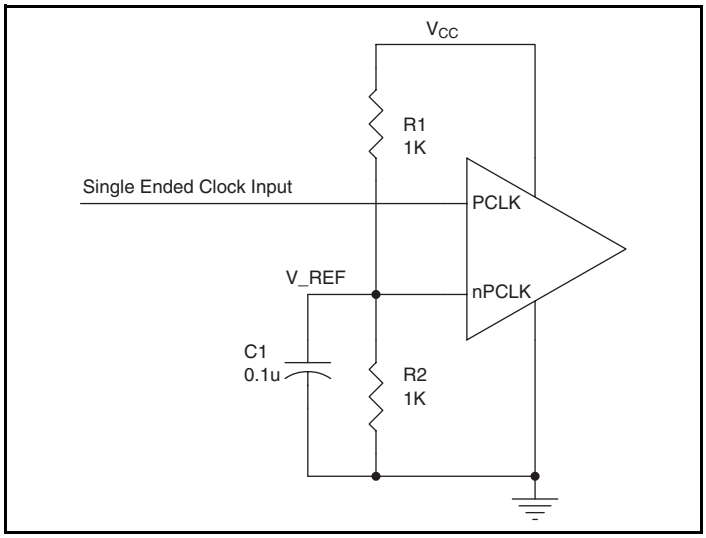


Figure 3. Single-Ended Signal Driving Differential Input

Crystal Input Interface

The ICS8430002 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 4* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

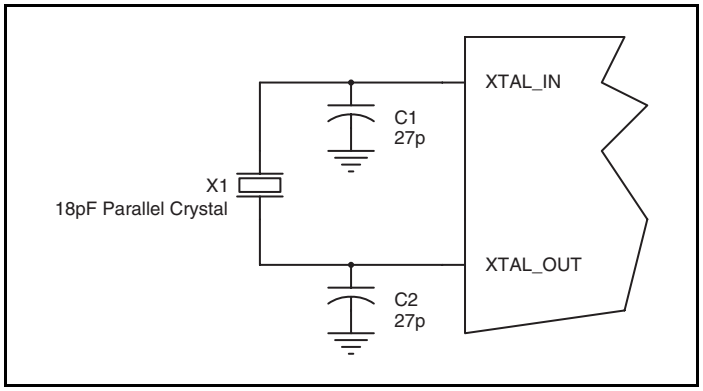


Figure 4. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 5.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

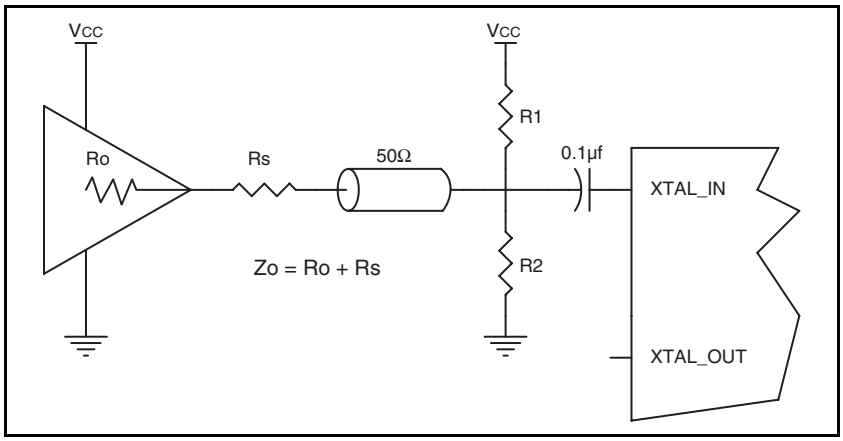


Figure 5. General Diagram for LVCMOS Driver to XTAL Input Interface

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 6A to 6E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

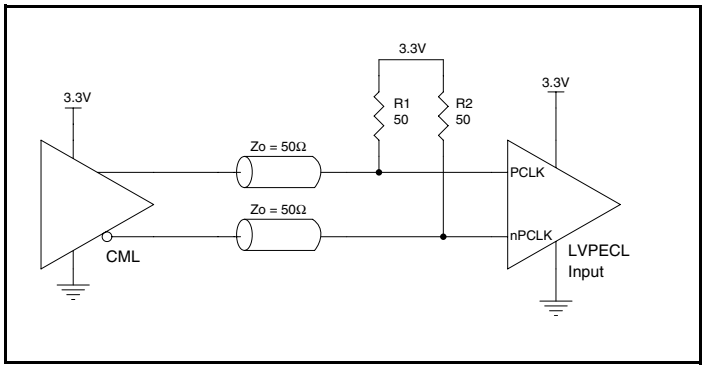


Figure 6A. PCLK/nPCLK Input Driven by an Open Collector CML Driver

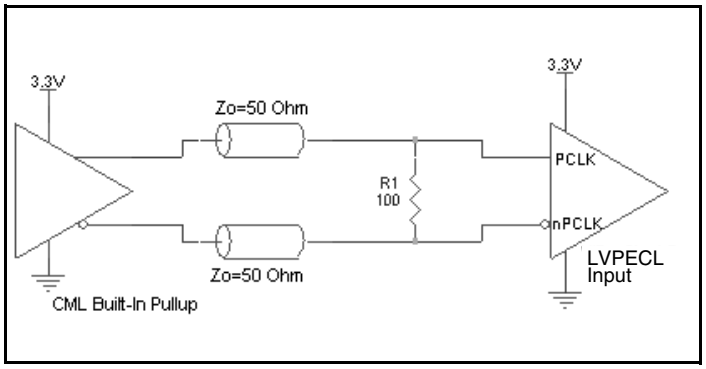


Figure 6B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

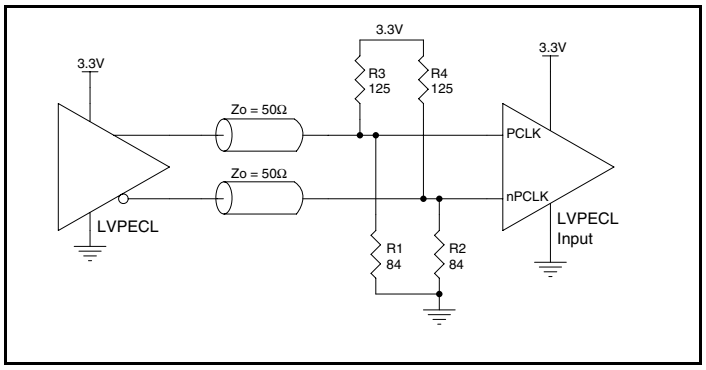


Figure 6C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

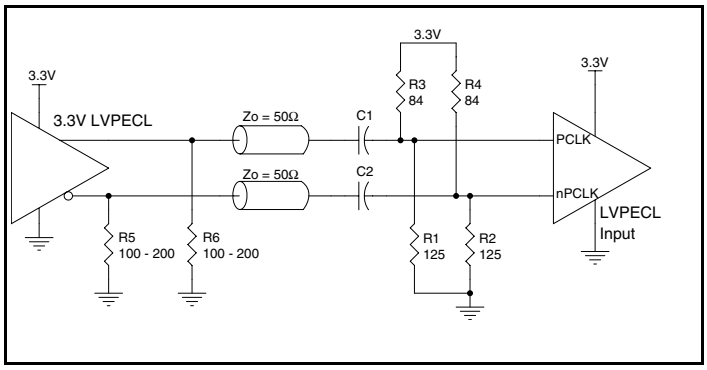


Figure 6D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

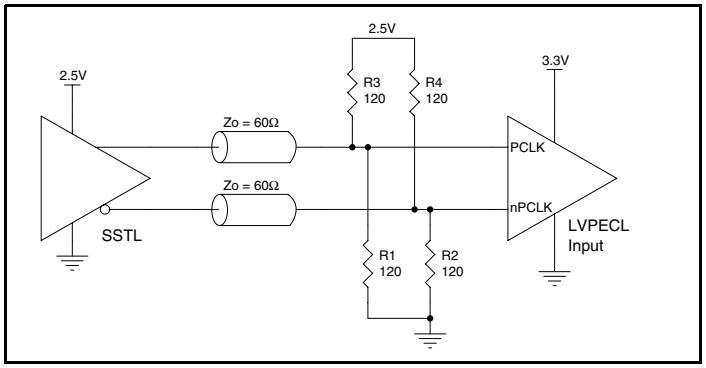


Figure 6E. PCLK/nPCLK Input Driven by an SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

TEST Output

The unused TEST output can be left floating. There should be no trace attached.

LVCMOS Output

All unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

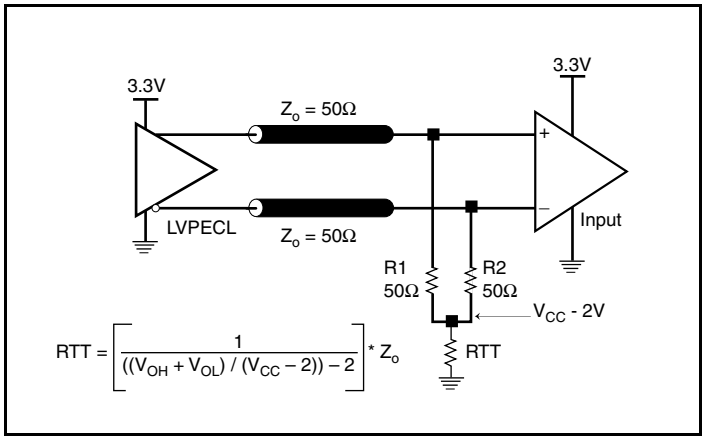


Figure 7A. 3.3V LVPECL Output Termination

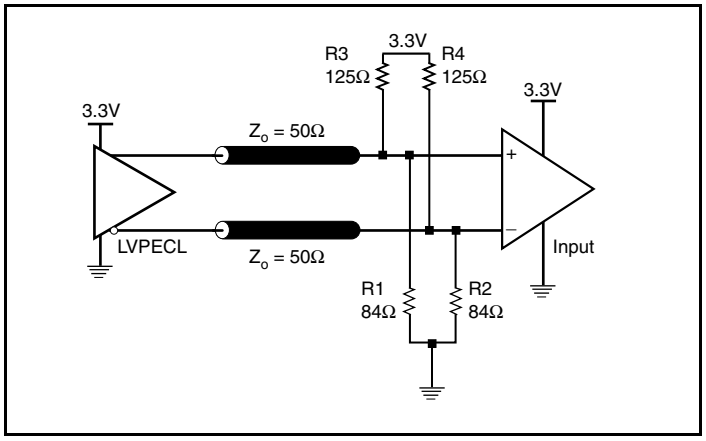


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 8B can be eliminated and the termination is shown in *Figure 8C.*

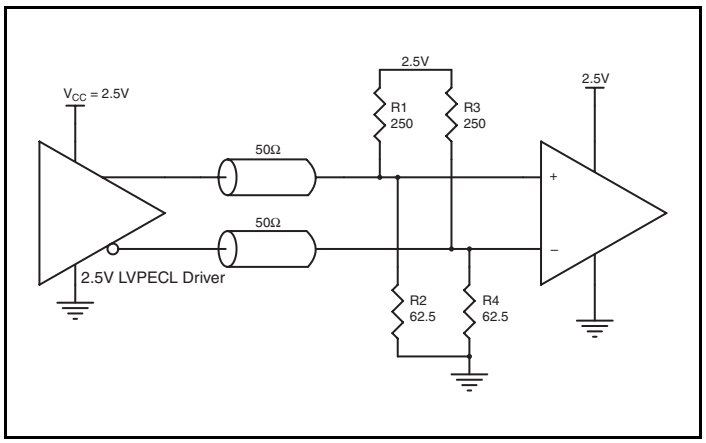


Figure 8A. 2.5V LVPECL Driver Termination Example

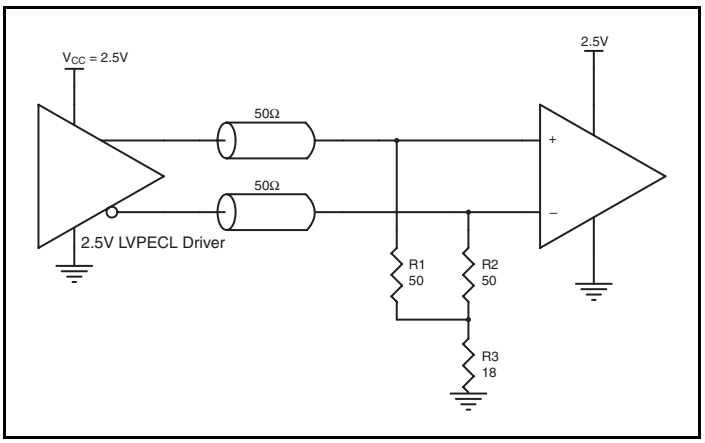


Figure 8B. 2.5V LVPECL Driver Termination Example

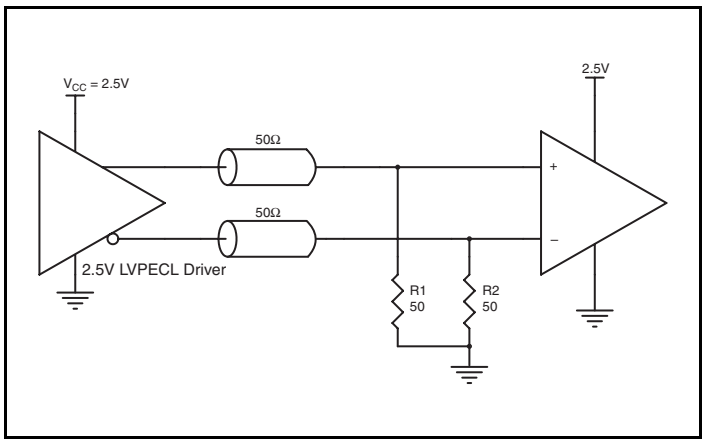


Figure 8C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 9 shows an example of ICS8430002 application schematic. In this example, the device is operated at V_{CC} = V_{CCO} = 3.3V. The device are be driven by a crystal, LVCMOS or LVPECL input sources. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. For the LVPECL output drivers, only two termination examples are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

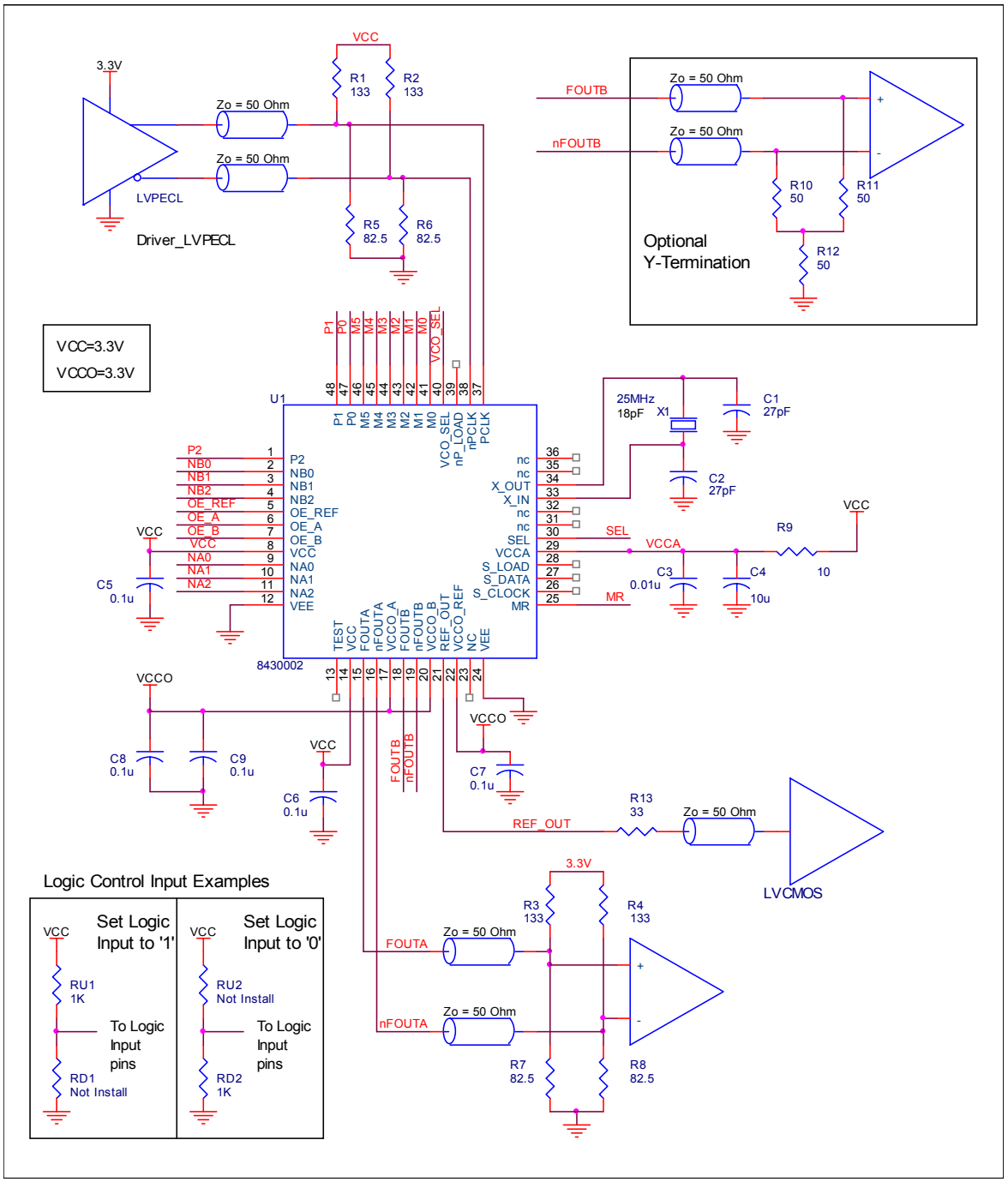


Figure 9. ICS8430002 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8430002.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8430002 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 182mA = **630.63mW**
- Power (LVPECL outputs)$_{MAX}$ = **30mW/Loaded Output pair**
- Power (LVPECL output) = 2 * 30mW = **60mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2
  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 7Ω)] = **30.4mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 7Ω * (30.4mA)^2 = **6.47mW per output**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (LVPECL output) + Power (R_{OUT})
  = 630.63mW + 60mW + 6.47mW **= 697.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.697W * 65.7°C/W = 115.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 8. Thermal Resistance θ_{JA} for 48 Lead TQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10.*

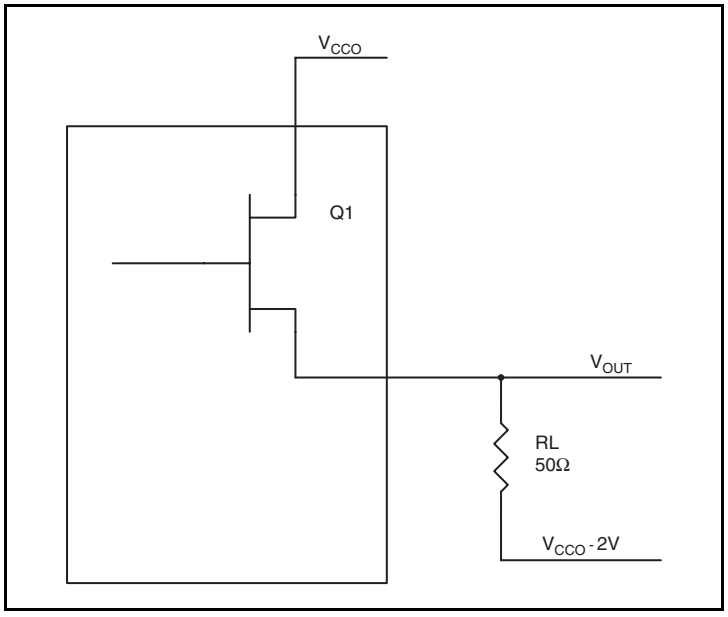


Figure 10. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.9V**
  ($V_{CCO\_MAX} - V_{OH\_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.7V**
  ($V_{CCO\_MAX} - V_{OL\_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 48 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

Transistor Count

The transistor count for ICS8430002 is: 7495

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead LQFP

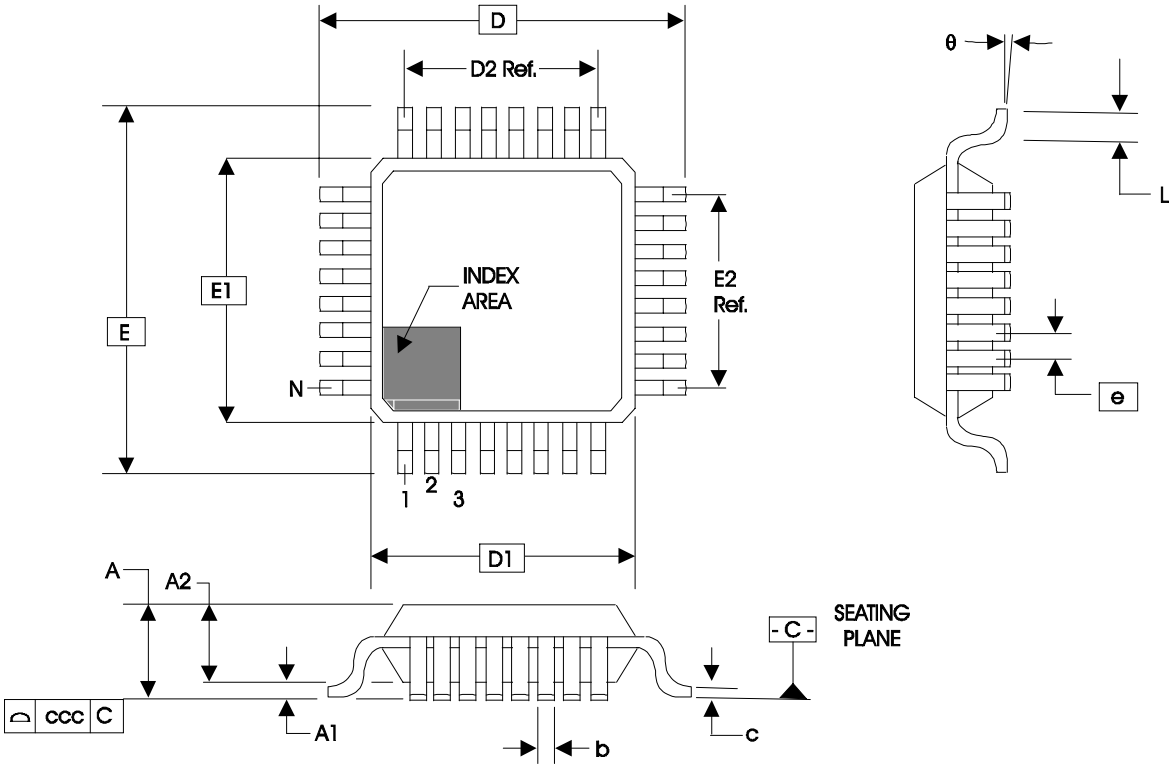


Table 10. Package Dimensions for 48 Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
e		0.5 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8430002AYLF	ICS8430002AL	“Lead-Free” 48 Lead LQFP	Tray	0°C to 70°C
8430002AYLFT	ICS8430002AL	“Lead-Free” 48 Lead LQFP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T1	5	Pin 5, 6, 7 added to descriptions. Changed max VCO from 640MHz to 650MHz throughout the datasheet.	5/5/09
C	 T1 T3D T5	2 4 5 8 11	Block Diagram - changed OE_A, OE_B to OEA, OEB. Figure 1, Parallel & Serial Load Operations - correct M[11:0] to M[5:0]. Pin Descriptions Table - changed OE_A, OE_B to OEA, OEB. Programmable Output Divider Table - corrected Output Frequency max. column. Input Frequency Characteristics - corrected equations in NOTE 1 and NOTE 2.	8/24/09
C		1	General Description - deleted the word possible at the end of the first sentence.	11/12/09

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