PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843251-04

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS843251-04 is a 10Gb/12Gb Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843251-04 can synthesize 10 Gigabit Ethernet and 12 Gigabit Ethernet with a 25MHz crystal. It can also generate SATA and 10Gb Fibre Channel reference clock frequencies with the appropriate choice of crystals. The ICS843251-04 has excellent phase jitter performance and is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 differential 3.3V LVPECL output
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Crystal input frequency range: 19.33MHz - 30MHz
- Output frequency range: 145MHz - 187.5MHz
- VCO frequency range: 580MHz - 750MHz
- RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.39ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free compliant packages

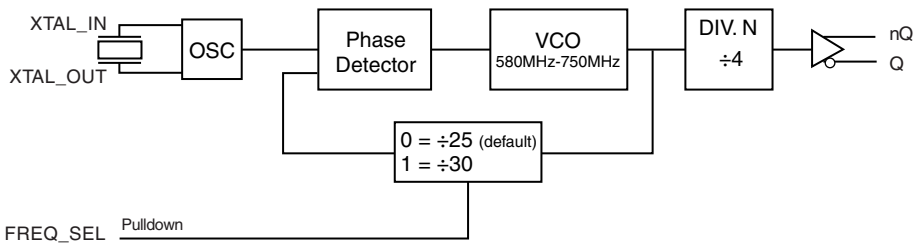
CONFIGURATION TABLE WITH 25MHZ CRYSTAL

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
25	30	750	4	187.5	12 Gigabit Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet

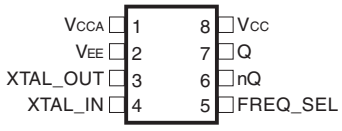
CONFIGURATION TABLE WITH SELECTABLE CRYSTALS

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
20	30	600	4	150	SATA
21.25	30	637.5	4	159.375	10 Gigabit Fibre Channel
24	25	600	4	150	SATA
25.5	25	637.5	4	159.375	10 Gigabit Fibre Channel
30	25	750	4	187.5	12 Gigabit Ethernet

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS843251-04

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: Pulldown refers to internal input resistors. See Table 2, Pin Characterristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			TBD		mA
I_{CCA}	Analog Supply Current			TBD		mA
I_{EE}	Power Supply Current			TBD		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	FREQ_SEL		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	FREQ_SEL		-0.3		0.8	V
I_{IH}	Input High Current	FREQ_SEL	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 3C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

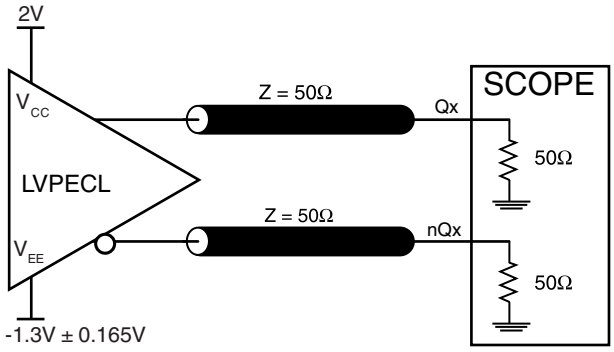
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.33		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA=0°C TO 70°C

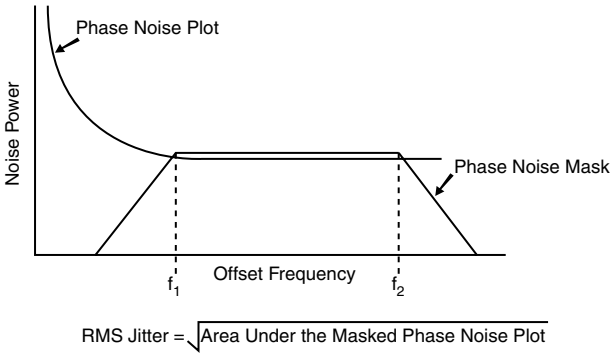
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		145		187.5	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.39		ps
		159.375MHz @ Integration Range: 1.875MHz - 20MHz		TBD		ps
		187.5MHz @ Integration Range: 1.875MHz - 20MHz		0.48		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		340		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

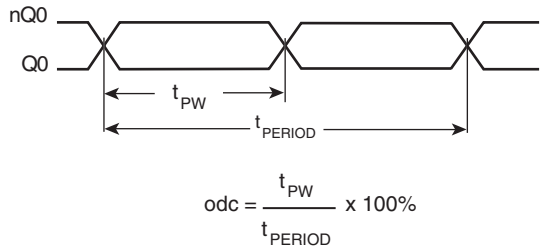
PARAMETER MEASUREMENT INFORMATION



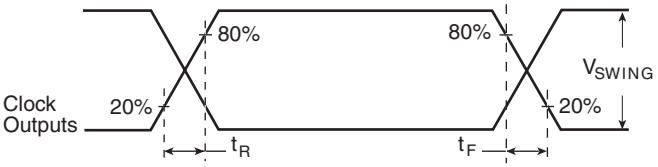
3.3V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843251-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

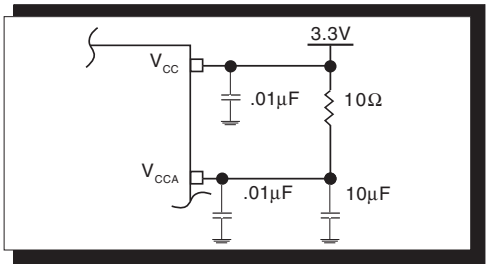


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843251-04 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

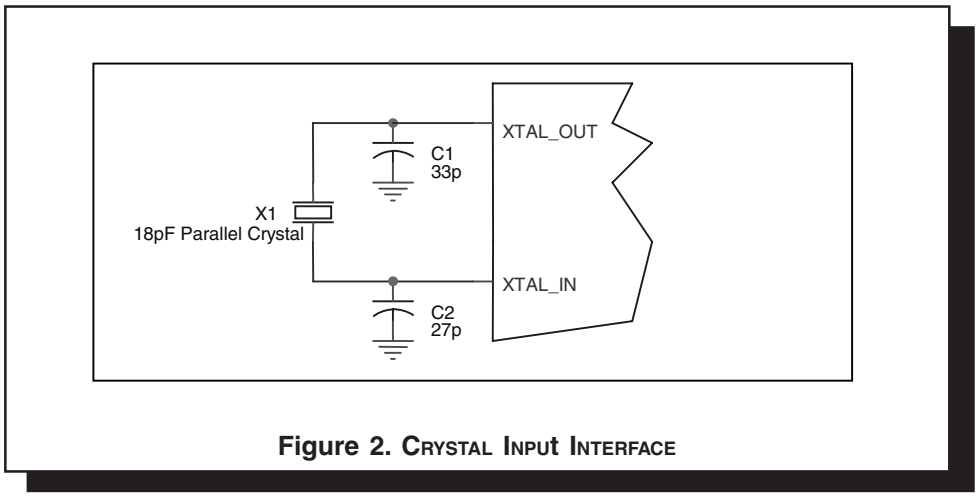


Figure 2. CRYSTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

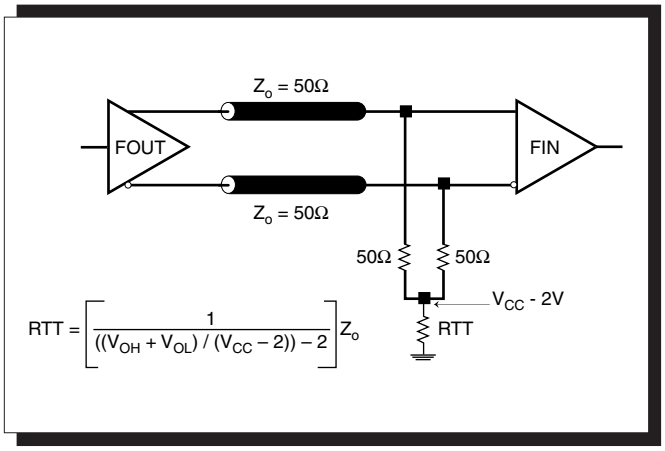


FIGURE 3A. LVPECL OUTPUT TERMINATION

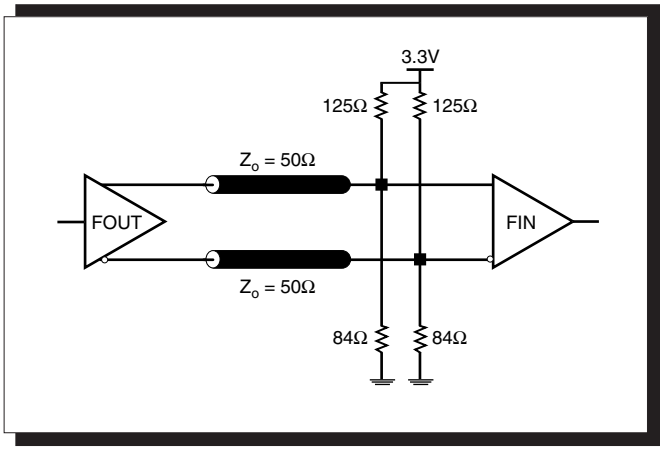


FIGURE 3B. LVPECL OUTPUT TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS843251-04 is: 1891

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

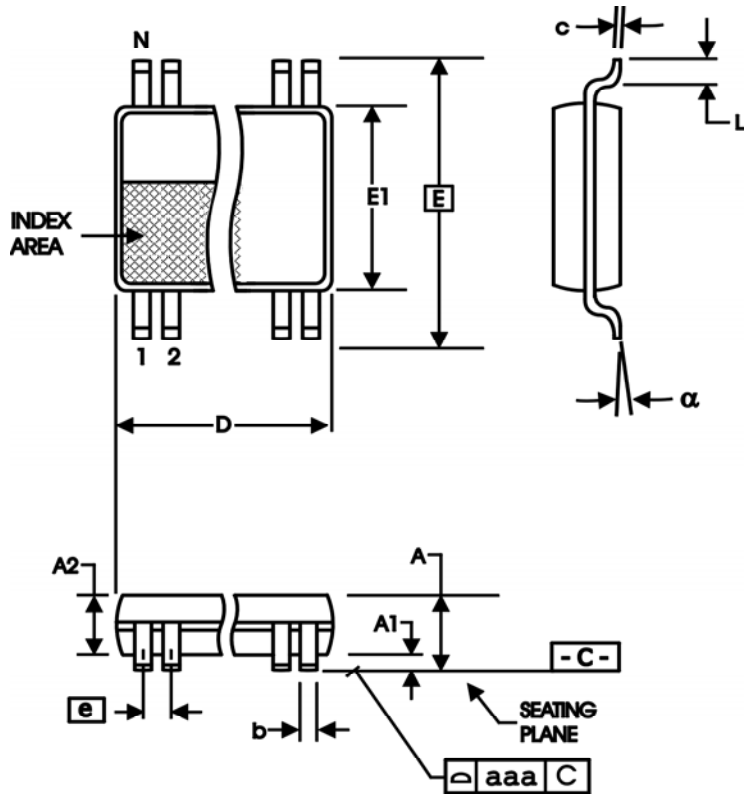


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843251AG-04	51A04	8 Lead TSSOP	tube	0°C to 70°C
ICS843251AG-04T	51A04	8 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843251AG-04LF	1A04L	8 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843251AG-04LFT	1A04L	8 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.