FEMTOCLOCK™ CRYSTAL-TO-LVPECL/LVDS/LVCMOS CLOCK GENERATOR

ICS843S2807

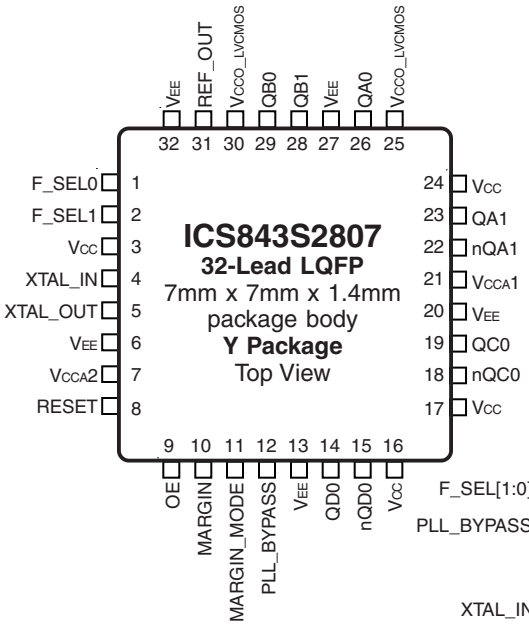
General Description

ICS843S2807 is a low phase noise Clock Generator and is a member of the HiperClockS™ family of high performance clock solutions from IDT. The device provides five banks of outputs and a reference clock. The banks can be enabled by using a common output enable pin. A 25MHz crystal is used to generate the 50MHz, 66.67MHz, 87.5MHz, 100MHz, 125MHz, 133MHz and 350MHz frequencies.

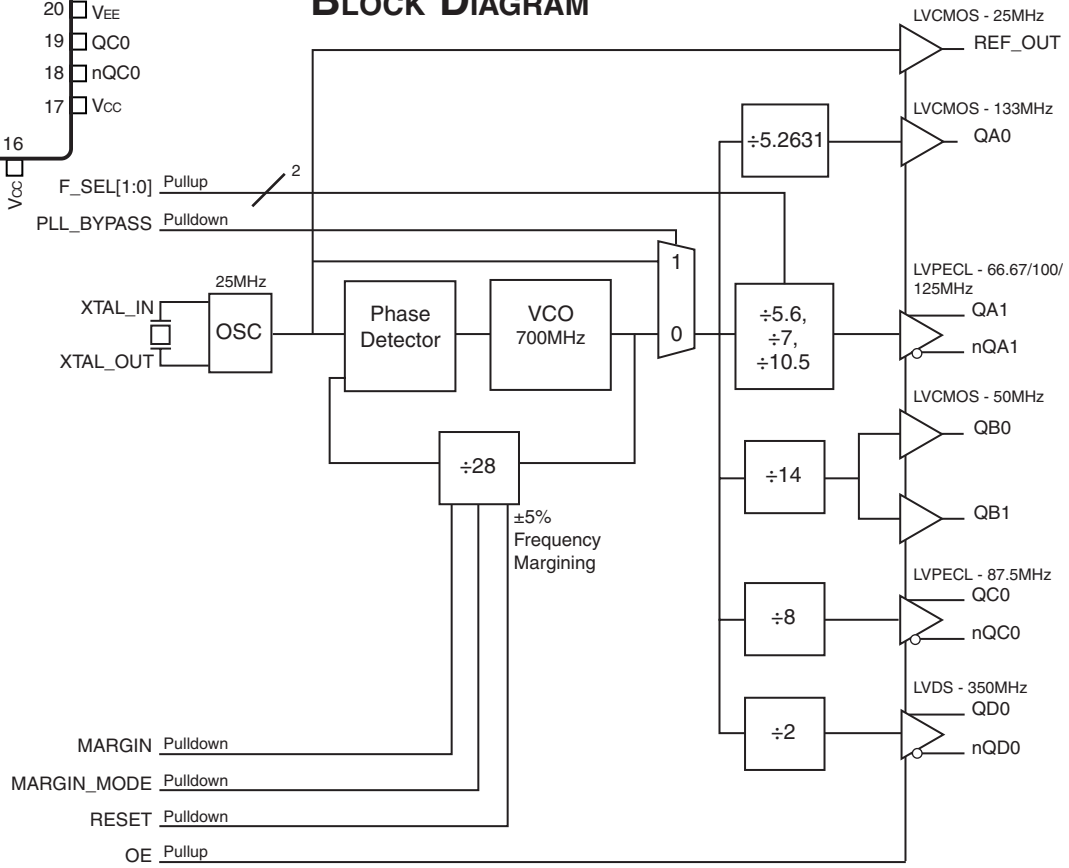
Features

- Five banks of outputs:
  Bank A: one single-ended (QA0) LVCMOS output at: 133MHz and one (QA1/nQA1) LVPECL output at: 66.67MHz, 100MHz and 125MHz
  Bank B: two (QB0, QB1) LVCMOS outputs at: 50MHz
  Bank C: one (QC0/nQC0) differential LVPECL output at: 87.5MHz
  Bank D: one (QD0/nQD0) differential LVDS output at: 350MHz
  One single-ended LVCMOS reference clock output at: 25MHz
- Crystal input frequency: 25MHz
- Maximum output frequency: 350MHz
- ±5% frequency margining
- Full 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS6) packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	F_SEL0, F_SEL1	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3A.
3, 16, 17, 24	V_{CC}	Power		Core supply pins.
4, 5	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
6, 13, 20, 27, 32	V_{EE}	Power		Negative supply pins.
7, 21	V_{CCA2}, V_{CCA1}	Power		Analog supply pins.
8	RESET	Input	Pulldown	Resets the dividers and PLL. LVCMOS/LVTTL interface levels.
9	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels.
10	MARGIN	Input	Pulldown	Selects between the margin and normal mode. LVCMOS/LVTTL interface levels. See Table 3B.
11	MARGIN_MODE	Input	Pulldown	Selects between ±5% margin. LVCMOS/LVTTL interface levels. See Table 3B.
12	PLL_BYPASS	Input	Pulldown	Selects between the PLL and XTAL as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL. LVCMOS/LVTTL interface levels.
14, 15	QD0, nQD0	Output		Differential Bank D clock outputs. LVDS interface levels.
18, 19	nQC0, QC0	Output		Differential Bank C clock outputs. LVPECL interface levels.
22, 23	nQA1, QA1	Output		Differential Bank A clock outputs. LVPECL interface levels.
25, 30	V_{CCO_LVCMOS}	Power		Output supply pins for LVCMOS/LVTTL outputs.
26	QA0	Output		Single-ended Bank A clock output. LVCMOS/LVTTL interface levels. 15Ω impedance.
28, 29	QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 15Ω impedance.
31	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels. 15Ω impedance.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance	QA0, QB0, QB1, REF_OUT	V_{CC}, V_{CCO_LVCMOS} = 3.465V		TBD		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	QA0, QB0, QB1, REF_OUT	V_{CCO_LVCMOS} = 3.465V		15		Ω

TABLE 3A. F_SELx FUNCTION TABLE

Inputs		QA1 Output Frequency (MHz)
F_SEL1	F_SEL0	
0	1	100
1	0	125
1	1	66.67 (default)

TABLE 3B. MARGIN/MARGIN_MODE FUNCTION TABLE

Inputs		
MARGIN	MARGIN_MODE	Operation
0	1	-5%
X	0	Nominal
1	1	+5%

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{CCO_LVCMOS} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA} Junction-to-Case	71.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		$V_{CC} – I_{CCA} * 10\Omega$	3.3	V_{CC}	V
V_{CCO_LVCMOS}	Output Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current			TBD		mA
I_{CCA}	Analog Supply Current			TBD		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PLL_BYPASS, RESET, MARGIN, MARGIN_MODE	$V_{CC} = V_{IN} = 3.465V$			150	µA
		OE, F_SEL[1:0]				5	µA
I_{IL}	Input Low Current	PLL_BYPASS, RESET, MARGIN, MARGIN_MODE	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OE, F_SEL[1:0]		-150			µA
V_{OH}	Output High Voltage; NOTE 1	REF_OUT, QA0, QB0, QB1	$V_{CCO\_LVCMOS} = 3.465V \pm 5\%$	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	REF_OUT, QA0, QB0, QB1	$V_{CCO\_LVCMOS} = 3.465V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_LVCMOS}/2$. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

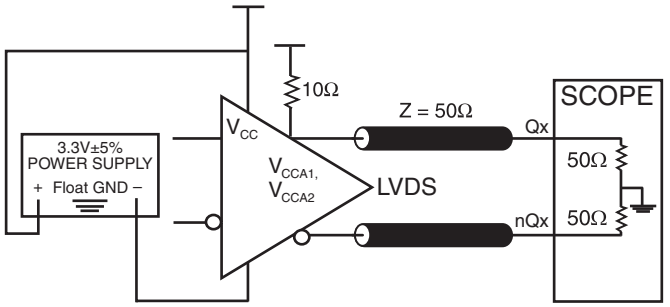
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

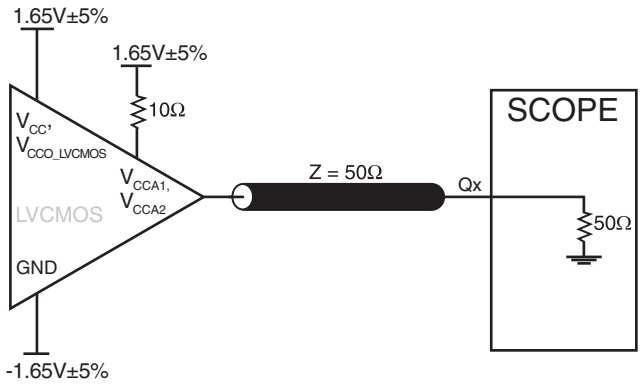
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QD0/nQD0			350		MHz
		QA0			133		MHz
		QA1/nQA1	F_SEL1 = 1, F_SEL0 = 1		66.67		MHz
		QA1/nQA1	F_SEL1 = 0, F_SEL0 = 1		100		MHz
		QA1/nQA1	F_SEL1 = 1, F_SEL0 = 0		125		MHz
		QB0, QB1			50		MHz
		QC0/nQC0			87.5		MHz
		REF_OUT			25		MHz
*t*sk(b)	Bank Skew; NOTE 1, 2	QB0, QB1			TBD		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2	REF_OUT			75		ps
		QA0			150		ps
		QB0, QB1			75		ps
		QA1/nQA1			200		ps
		QC0/nQC0			50		ps
		QD0/nQD0			50		ps
t_R / t_F	Output Rise/Fall Time	REF_OUT, QA0, QB0, QB1	20% to 80%		350		ps
		QA1/nQA1, QC0/nQC0	20% to 80%		250		ps
		QD0/nQD0	20% to 80%		400		ps
odc	Output Duty Cycle	REF_OUT, QA0, QB0, QB1		45		55	%
		QA1/nQA1, QC0/nQC0		45		55	%
		QD0/nQD0		45		55	%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

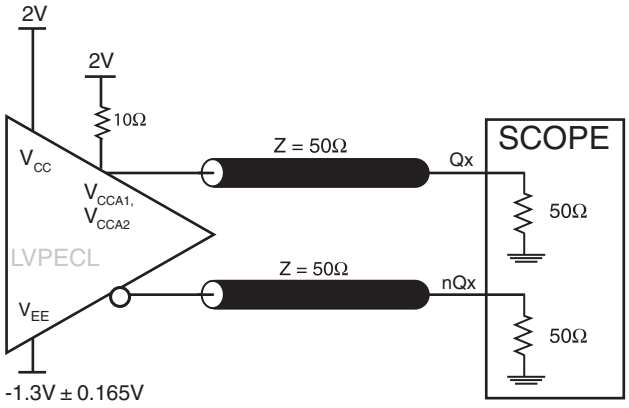
PARAMETER MEASUREMENT INFORMATION



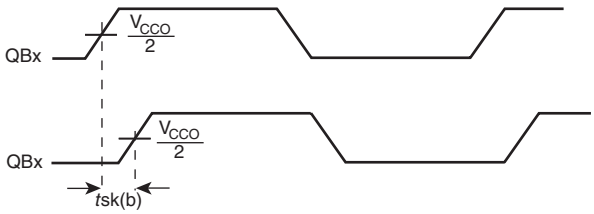
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



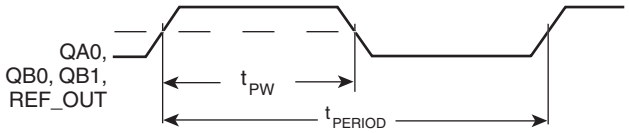
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT

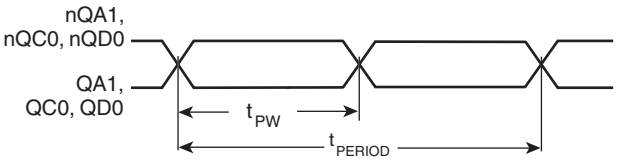


LVCMOS BANK SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

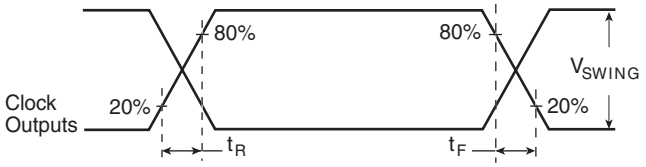
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



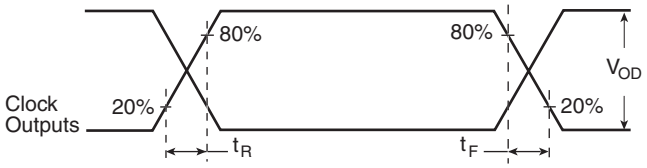
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

DIFFERENTIAL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

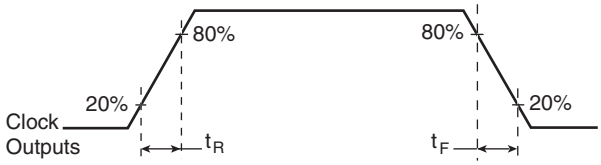
PARAMETER MEASUREMENT INFORMATION, CONTINUED



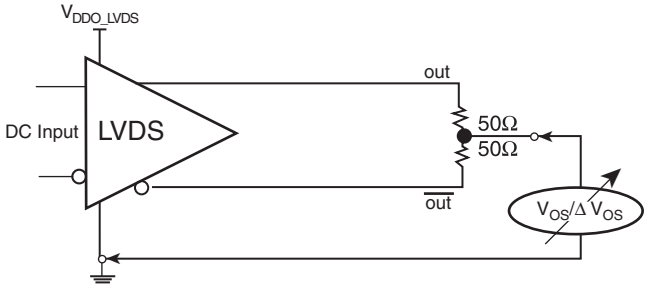
LVPECL OUTPUT RISE/FALL TIME



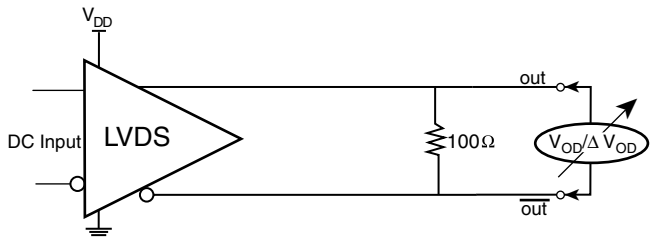
LVDS OUTPUT RISE/FALL TIME



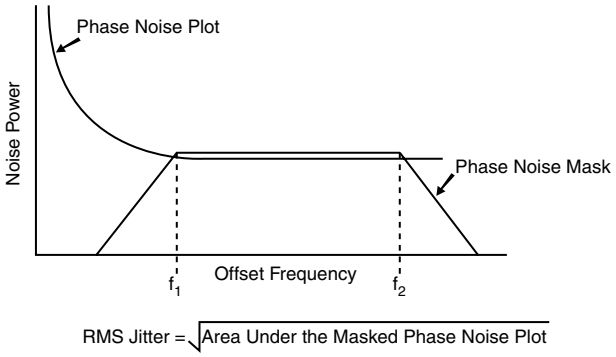
LVCMOS OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP



RMS PHASE JITTER

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843S2807 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, $V_{CCA1,}$ V_{CCA2} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

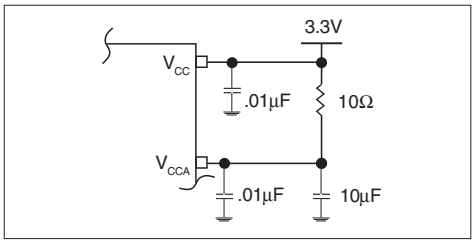


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUTS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS843S2807 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz crystal and were chosen to minimize the ppm error.

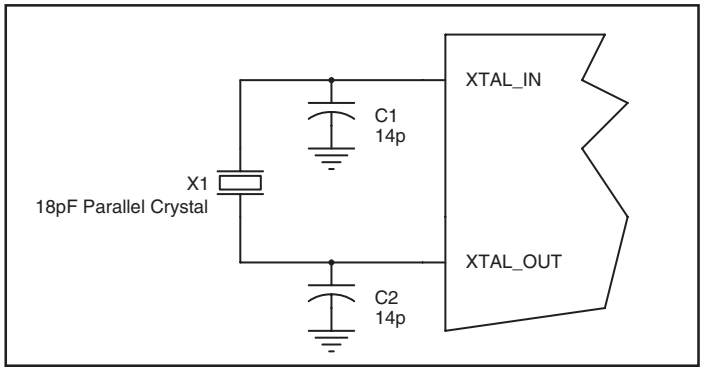


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

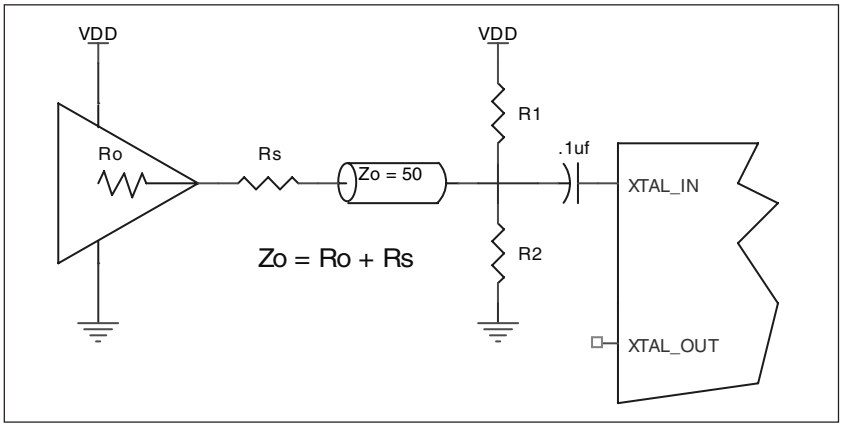


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

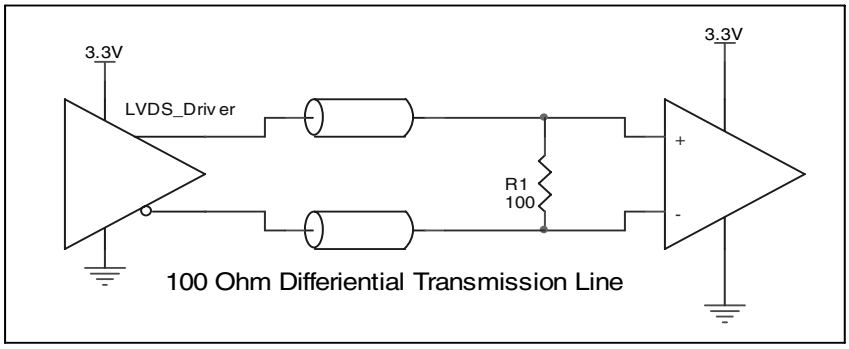


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

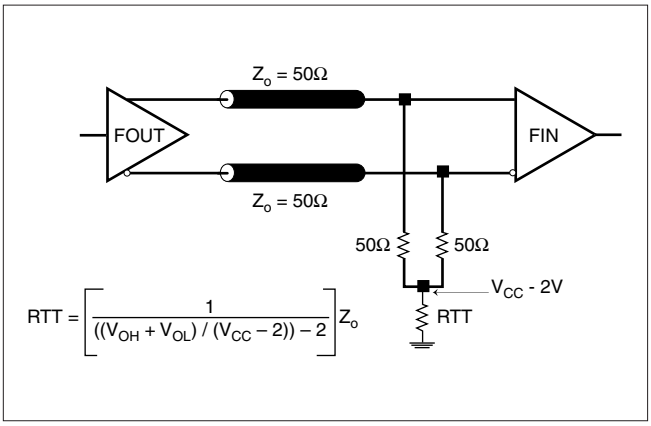


FIGURE 5A. LVPECL OUTPUT TERMINATION

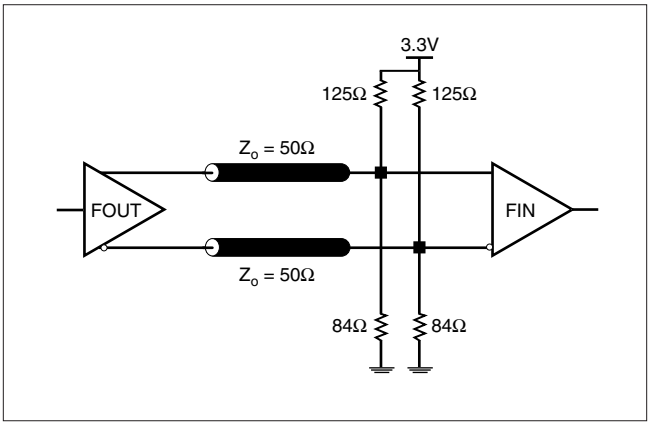


FIGURE 5B. LVPECL OUTPUT TERMINATION

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	71.9°C/W	62.1°C/W	58.5°C/W

TRANSISTOR COUNT

The transistor count for ICS843S2807 is: 11,230

Package Outline - Y Suffix for 32 Lead LQFP

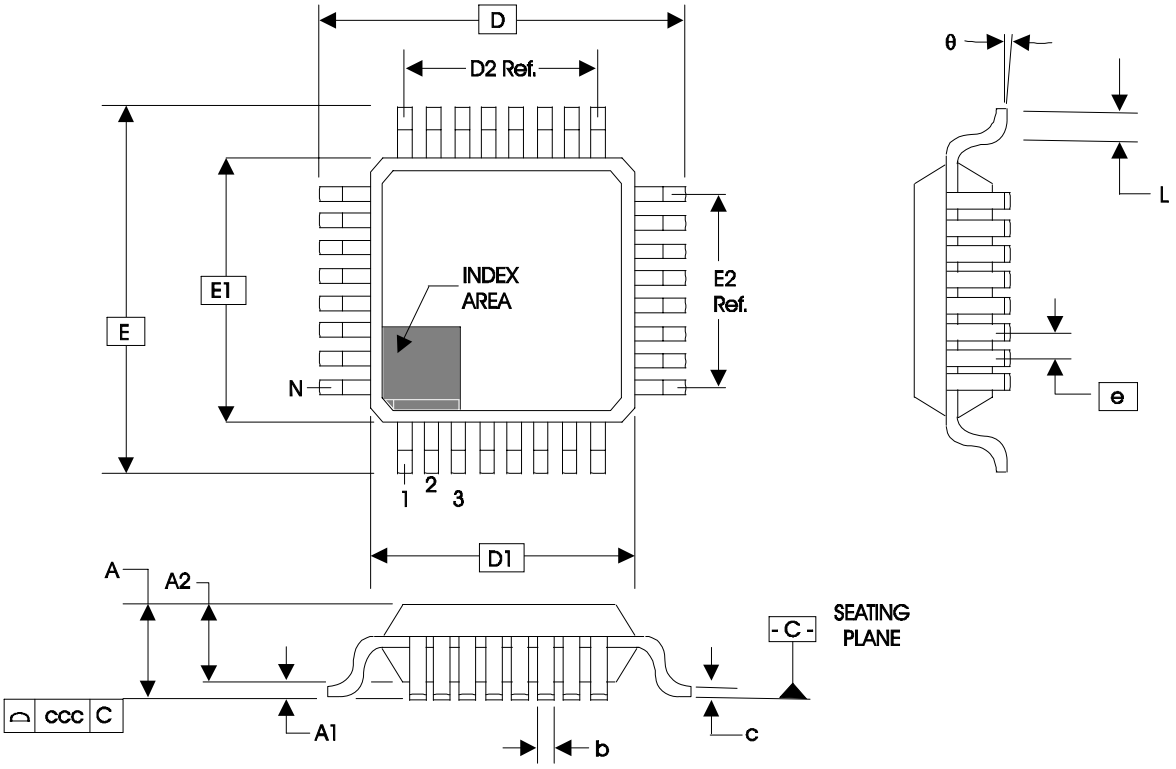


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843S2807BY	TBD	32 Lead LQFP	tray	0°C to 70°C
843S2807BYT	TBD	32 Lead LQFP	1000 tape & reel	0°C to 70°C
843S2807BYLF	ICS43S2807BL	32 Lead "Lead-Free" LQFP	tray	0°C to 70°C
843S2807BYLFT	ICS43S2807BL	32 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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