PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844004I-01

FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS844004I-01 is a 4 output LVDS Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz and 62.5MHz. The ICS844004I-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844004I-01 is packaged in a small 24-pin TSSOP package.

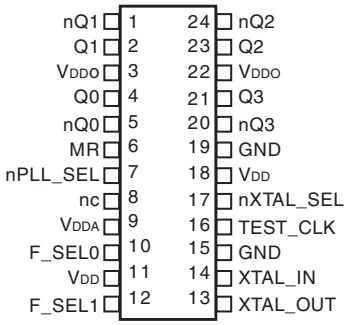
FEATURES

- Four LVDS outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.41ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature

FREQUENCY SELECT FUNCTION TABLE

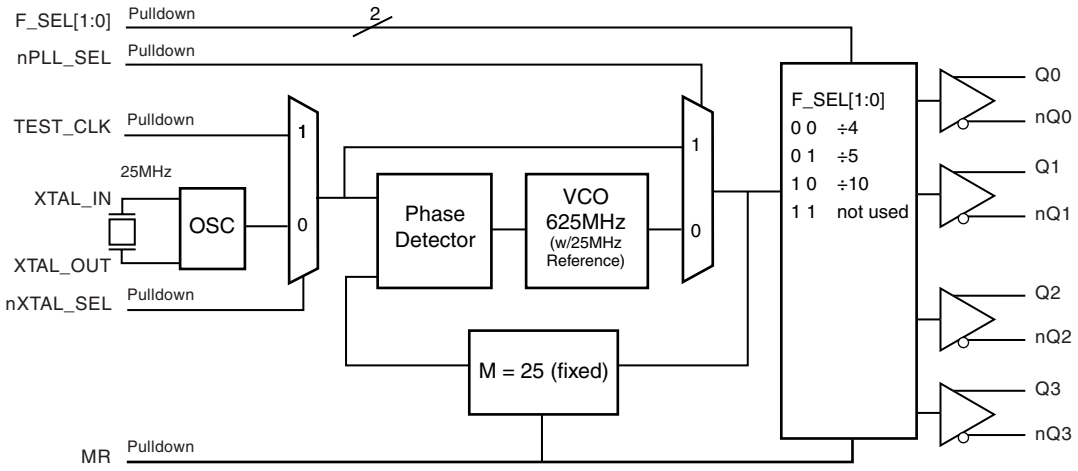
F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	Output Frequency (25MHz Ref.)
0	0	25	4	6.25	156.5
0	1	25	5	5	125
1	0	25	10	2.5	62.5
1	1	25	Not Used		Not Used

PIN ASSIGNMENT



ICS844004I-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. LVDS interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11, 18	V_{DD}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	GND	Power		Power supply ground.
16	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
17	nXTAL_SEL	Input	Pulldown	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	$V_{DD} = V_{IN}$ = 3.465 or 2.5V			150	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	V_{DD} = 3.465V or 2.5V, V_{IN} = 0V	-150			µA

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.2		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00		156.5		MHz
		F_SEL[1:0] = 01		125		MHz
		F_SEL[1:0] = 10		62.5		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.41		ps
		125MHz, (1.875MHz - 20MHz)		0.44		ps
		62.5MHz, (1.875MHz - 20MHz)		0.47		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

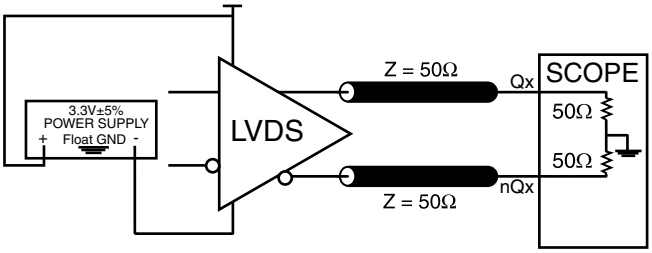
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

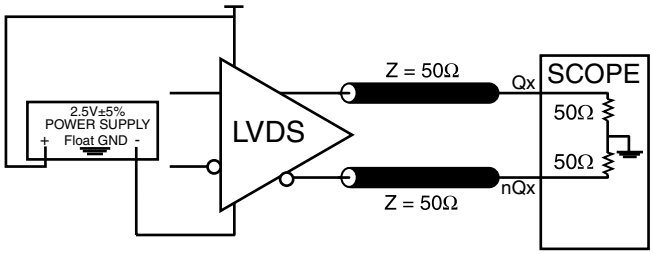
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00		156.5		MHz
		F_SEL[1:0] = 01		125		MHz
		F_SEL[1:0] = 10		62.5		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.41		ps
		125MHz, (1.875MHz - 20MHz)		0.44		ps
		62.5MHz, (1.875MHz - 20MHz)		0.47		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		480		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

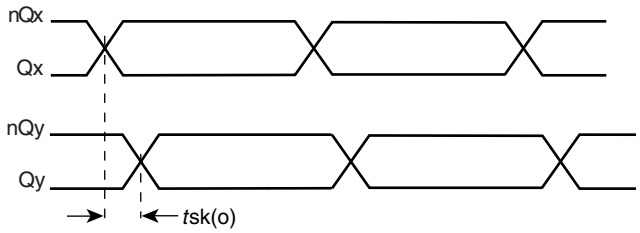
PARAMETER MEASUREMENT INFORMATION



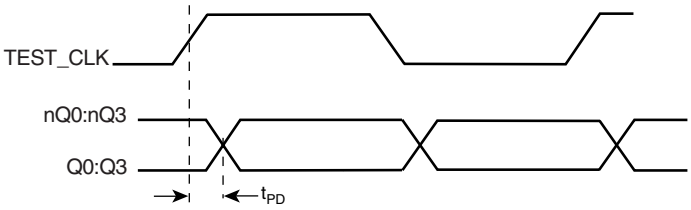
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



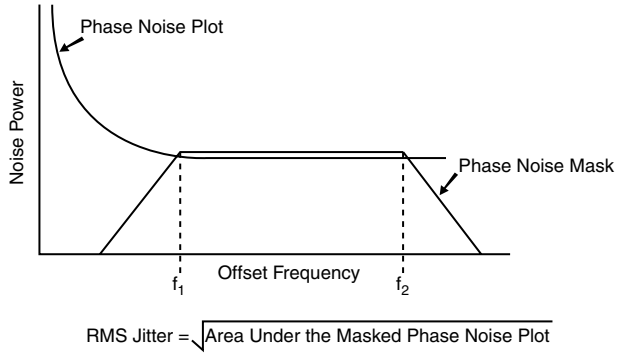
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



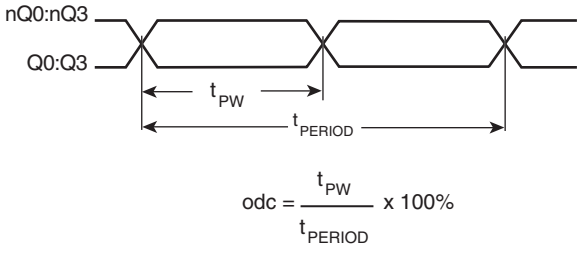
OUTPUT SKEW



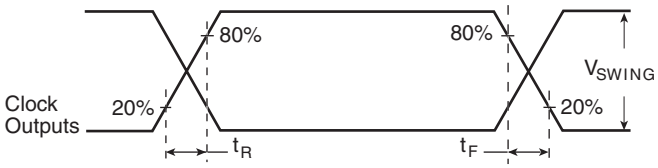
PROPAGATION DELAY



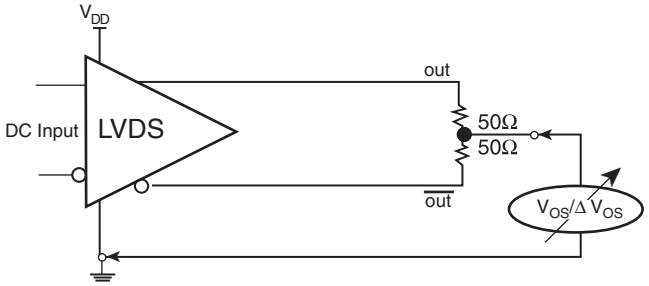
RMS PHASE JITTER



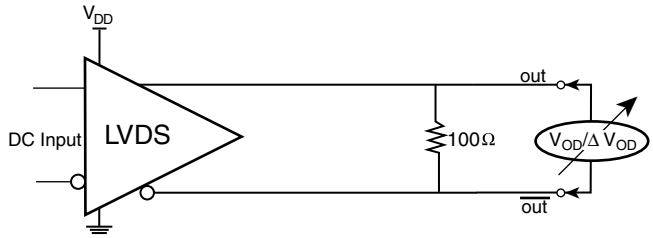
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844004I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

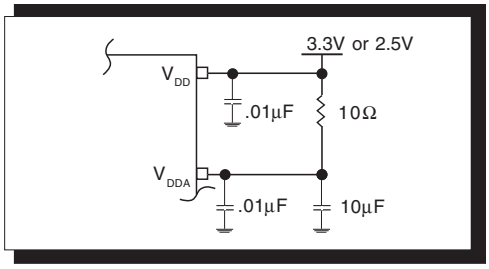


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844004I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

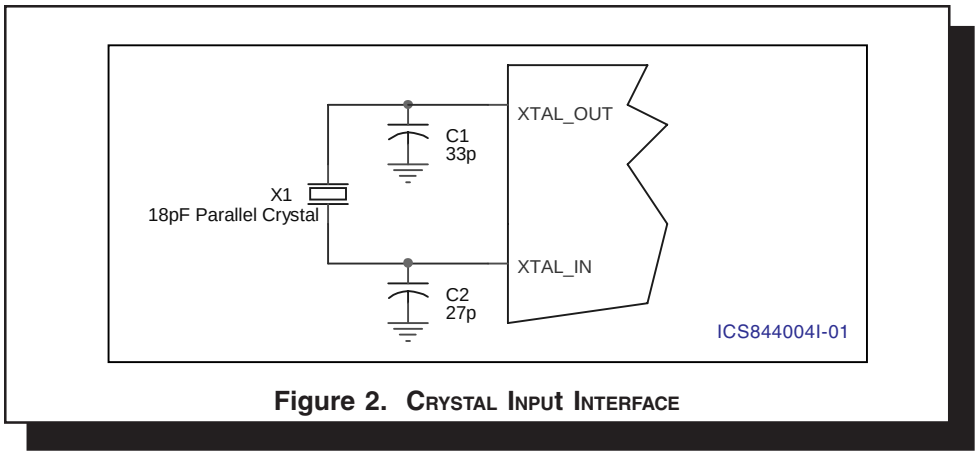


Figure 2. CRYSTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

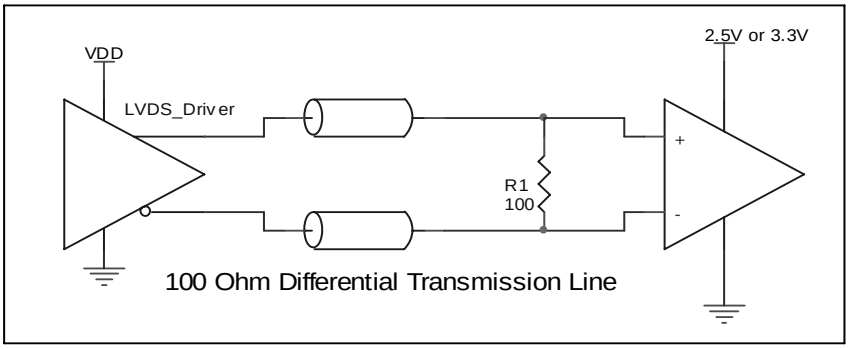


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS844004I-01 is: 2914

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

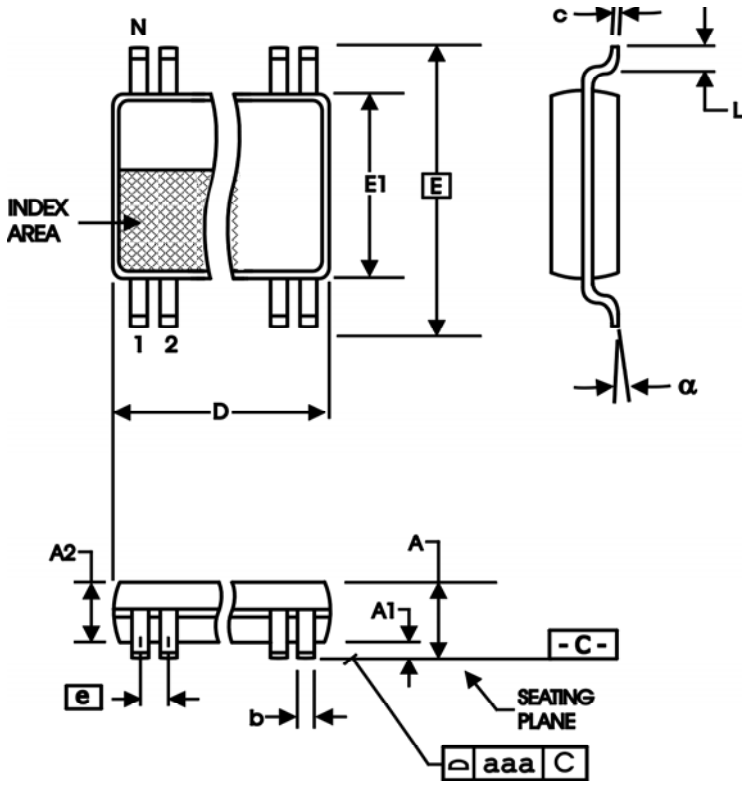


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844004AGI-01	ICS844004AI01	24 Lead TSSOP	tube	-40°C to 85°C
ICS844004AGI-01T	ICS844004AI01	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C