



Integrated
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ICS844256

FEMTOCLOCKS™ CRYSTAL-TO-LVDS

FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

GENERAL DESCRIPTION



The ICS844256 is a Crystal-to-LVDS Clock Synthesizer/Fanout Buffer designed for SONET and Gigabit Ethernet applications and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 19.44MHz crystal for SONET. The low phase noise characteristics of the ICS844256 make it an ideal clock for these demanding applications.

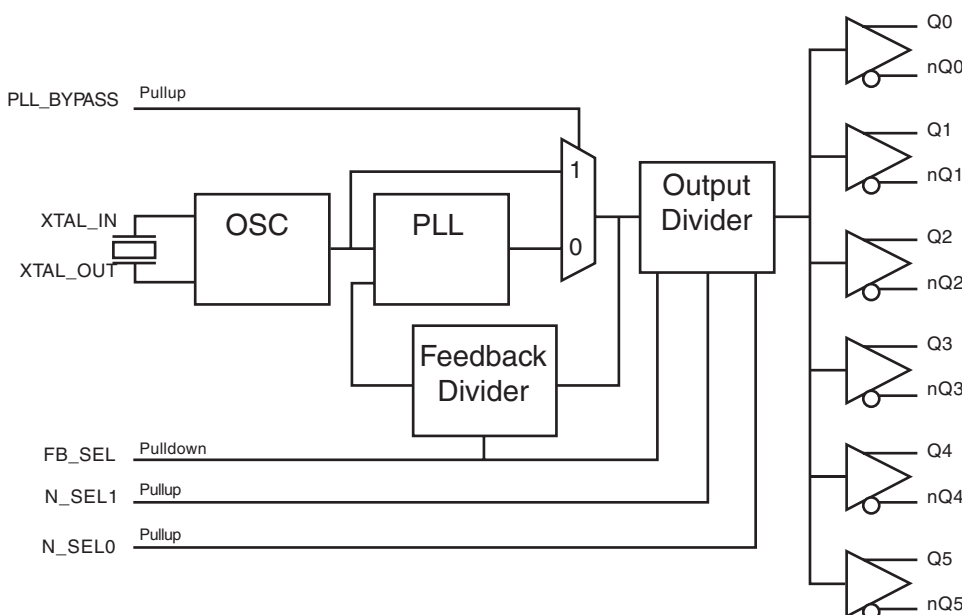
FEATURES

- Six LVDS outputs
- Crystal oscillator interface
- Output frequency range: 62.5MHz to 622.08MHz
- Crystal input frequency range: 15.625MHz to 25.5MHz
- RMS phase jitter at 125MHz, using a 25MHz crystal (1.875MHz to 20MHz): 0.48ps (typical)
- Full 3.3V or 3.3V core, 2.5V output supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

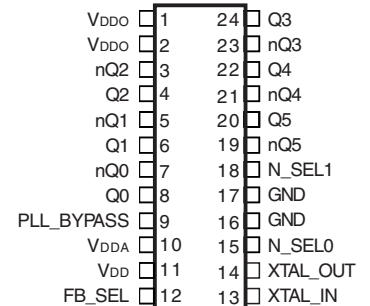
SELECT FUNCTION TABLE

Inputs			Function		
FB_SEL	N_SEL1	N_SELO	M Divide	N Divide	M/N
0	0	0	25	1	25
0	0	1	25	2	12.5
0	1	0	25	4	6.25
0	1	1	25	5	5
1	0	0	32	1	32
1	0	1	32	2	16
1	1	0	32	4	8
1	1	1	32	8	4

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS844256
24-Lead, 300-MIL SOIC
 7.5mm x 15.33mm x 2.3mm
 body package
M Package
 Top View

24-Lead TSSOP
 4.40mm x 7.8mm x 0.92mm
 body package
G Package
 Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	V _{DDO}	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
9	PLL_BYPASS	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTTL interface levels.
10	V _{DDA}	Power		Analog supply pin.
11	V _{DD}	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0 N_SEL1	Input	Pullup	Output frequency select pin. LVCMOS/LVTTTL interface levels.
16, 17	GND			Power supply ground.
19, 20	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ



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TABLE 3. CRYSTAL FUNCTION TABLE

Inputs				Function			
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M	VCO (MHz)	N	Output (MHz)
20	0	0	0	25	500	1	500
20	0	0	1	25	500	2	250
20	0	1	0	25	500	4	125
20	0	1	1	25	500	5	100
21.25	0	1	1	25	531.25	5	106.25
24	0	0	0	25	600	1	600
24	0	0	1	25	600	2	300
24	0	1	0	25	600	4	150
24	0	1	1	25	600	5	120
25	0	0	0	25	625	1	625
25	0	0	1	25	625	2	312.5
25	0	1	0	25	625	4	156.25
25	0	1	1	25	625	5	125
25.5	0	1	0	25	637.5	4	159.375
15.625	1	1	1	32	500	8	62.5
18.5625	1	1	1	32	594	8	74.25
18.75	1	0	0	32	600	1	600
18.75	1	0	1	32	600	2	300
18.75	1	1	0	32	600	4	150
18.75	1	1	1	32	600	8	75
19.44	1	0	0	32	622.08	1	622.08
19.44	1	0	1	32	622.08	2	311.04
19.44	1	1	0	32	622.08	4	155.52
19.44	1	1	1	32	622.08	8	77.76
19.53125	1	0	0	32	625	1	625
19.53125	1	0	1	32	625	2	312.5
19.53125	1	1	0	32	625	4	156.25
19.53125	1	1	1	32	625	8	78.125
20	1	1	1	32	640	8	80



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	
24 Lead SOIC	50°C/W (0 lfpm)
24 Lead TSSOP	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	$V_{DD} = V_{IN} = 3.465V$		150	μA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{DD} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	FB_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		μA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		μA



TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			TBD		mV
ΔV_{OD}	V_{OD} Magnitude Change			TBD		mV
V_{OS}	Offset Voltage			TBD		V
ΔV_{OS}	V_{OS} Magnitude Change			TBD		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15.625		25.5	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.



TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.48		ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.44		ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

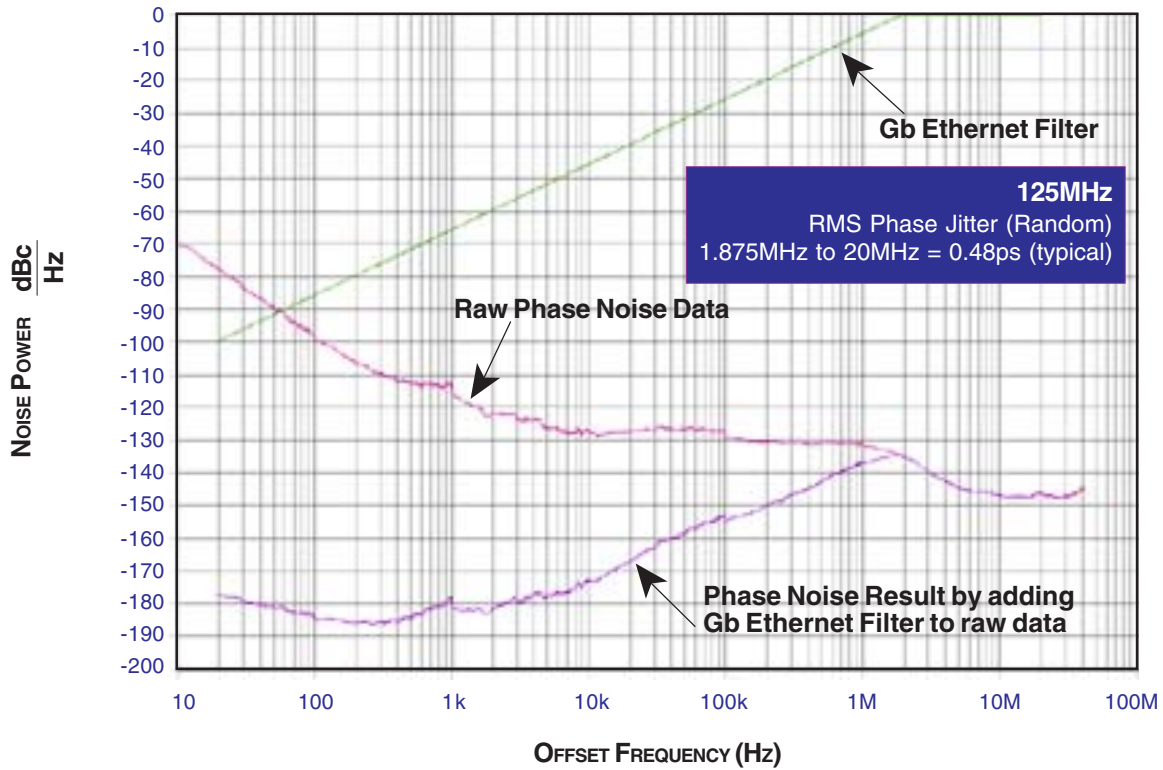
See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.

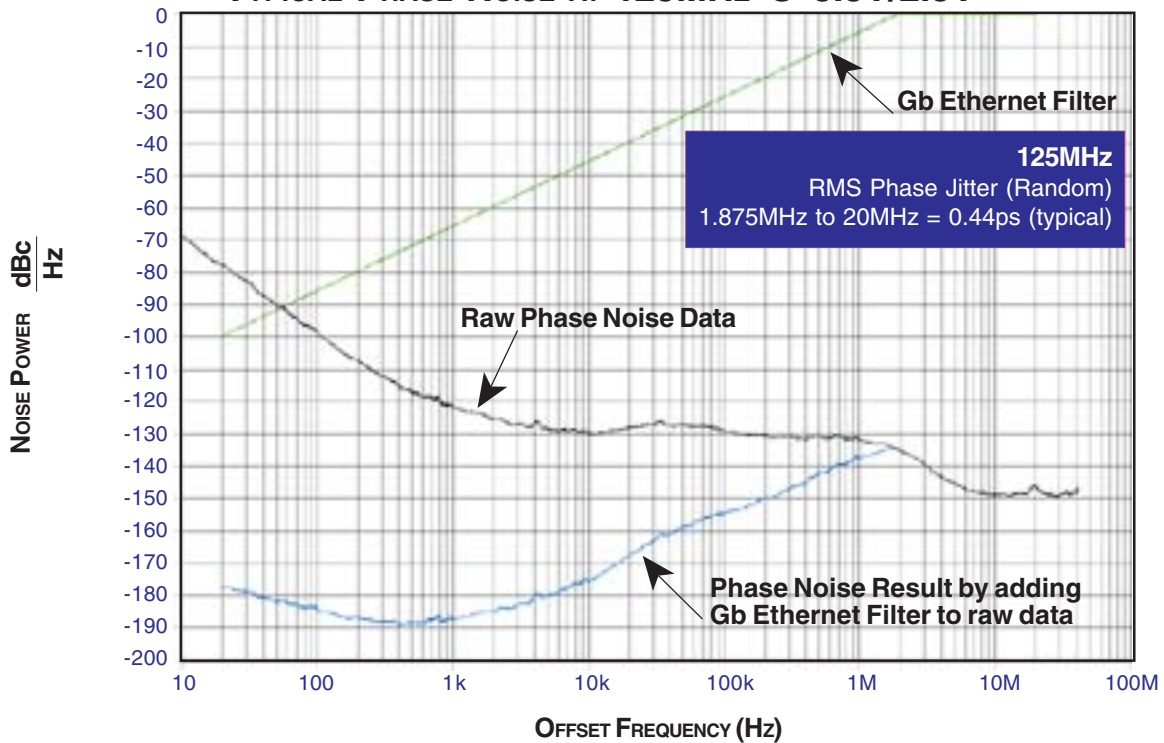
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.



TYPICAL PHASE NOISE AT 125MHz @ 3.3V

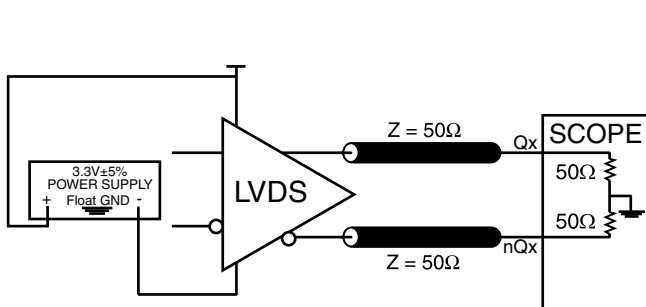


TYPICAL PHASE NOISE AT 125MHz @ 3.3V/2.5V

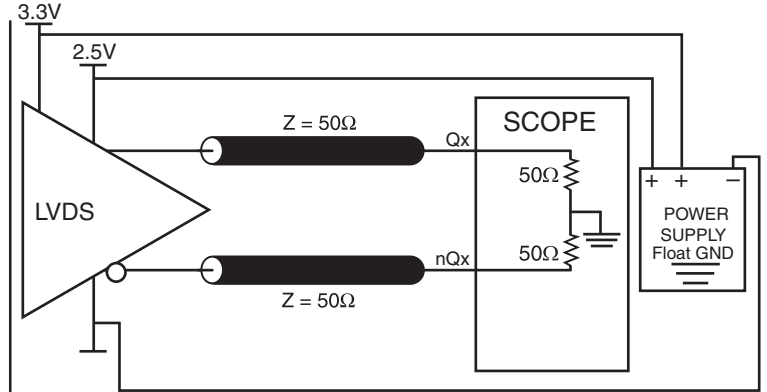




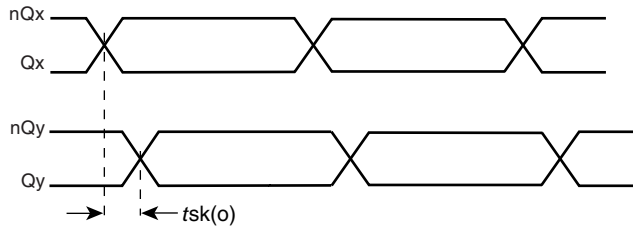
PARAMETER MEASUREMENT INFORMATION



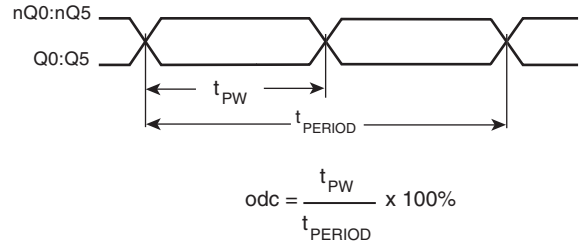
3.3V OUTPUT LOAD AC TEST CIRCUIT



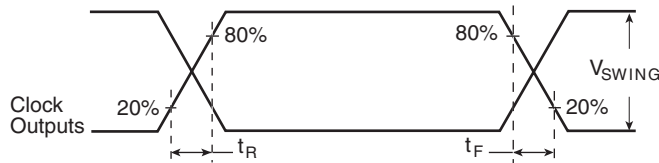
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



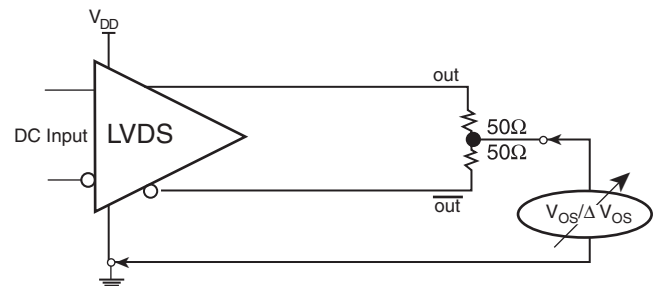
OUTPUT SKEW



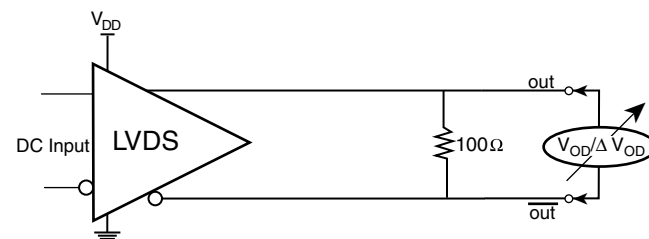
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844256 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

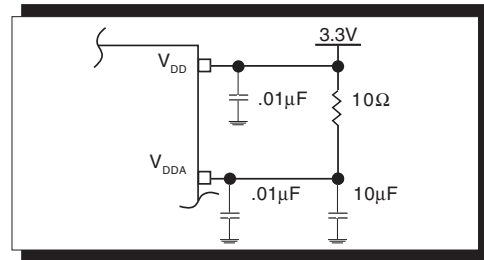


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844256 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

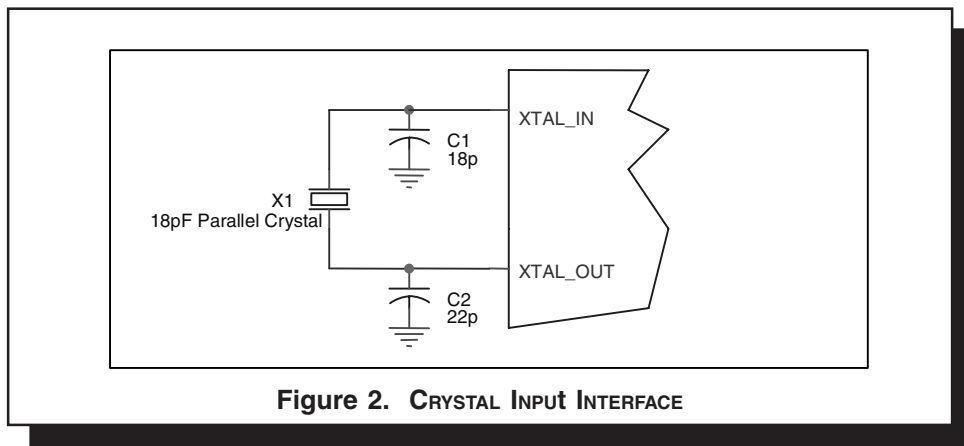


Figure 2. CRYSTAL INPUT INTERFACE



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

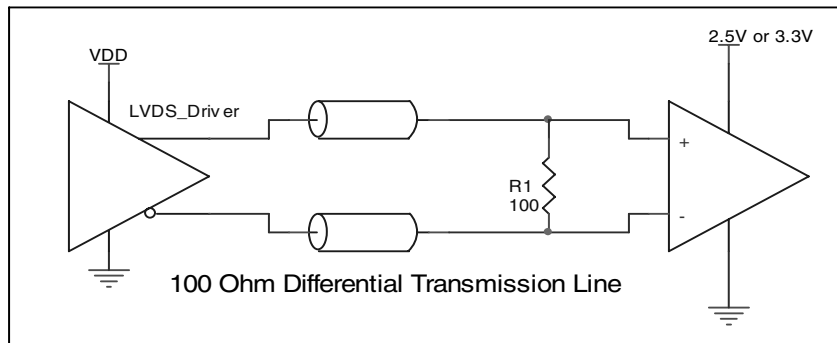


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION



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RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS844256 is: 3887



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PACKAGE OUTLINE - M SUFFIX FOR 24 LEAD SOIC

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

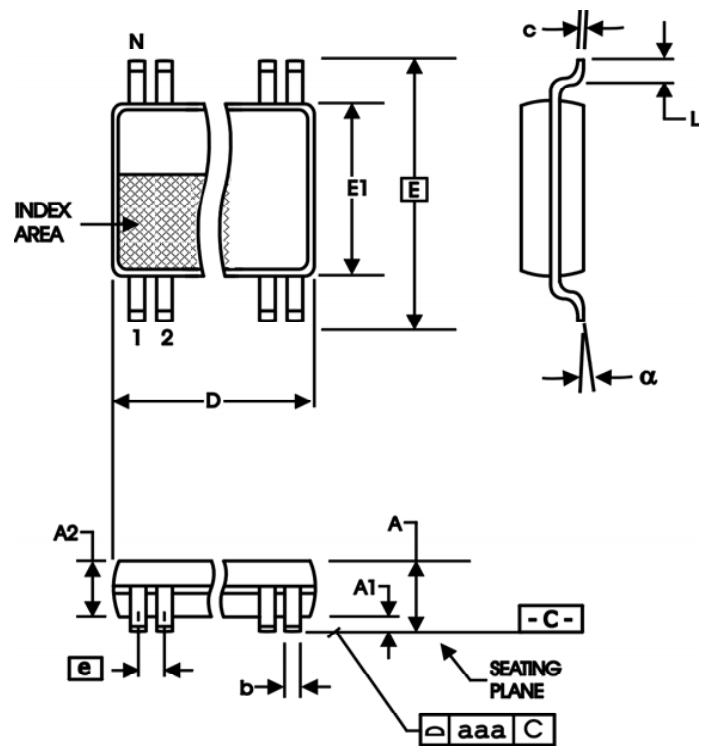
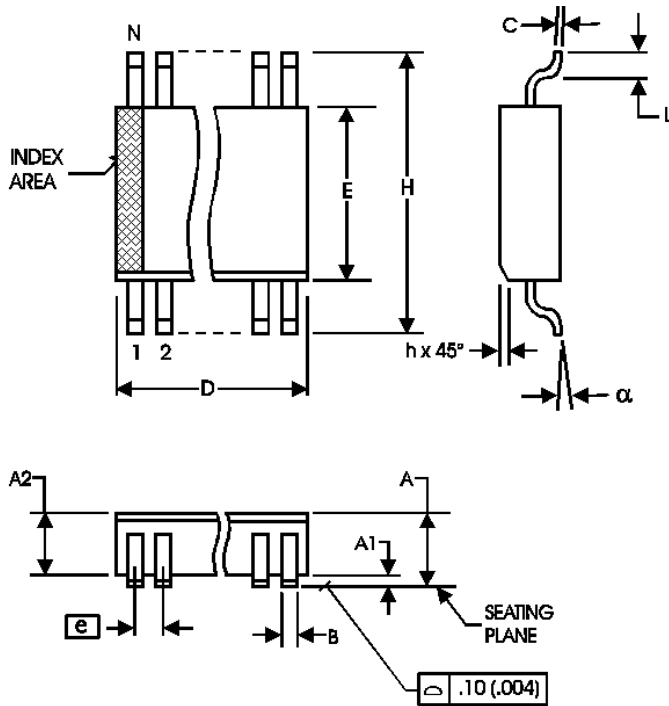


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844256AM	TBD	24 Lead SOIC	tube	0°C to 70°C
ICS844256AMT	TBD	24 Lead SOIC	1000 tape & reel	0°C to 70°C
ICS844256AMLf	TBD	24 Lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS844256AMLfT	TBD	24 Lead "Lead-Free" SOIC	1000 tape & reel	0°C to 70°C
ICS844256AG	ICS844256AG	24 Lead TSSOP	tube	0°C to 70°C
ICS844256AGT	ICS844256AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS844256AGLf	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS844256AGLfT	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "Lf" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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