



## GENERAL DESCRIPTION



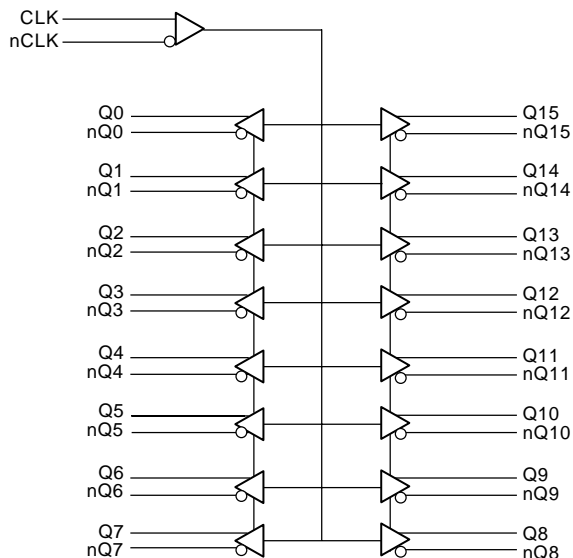
The ICS8530-01 is a low skew, 1-to-16 Differential-to-3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The high gain differential amplifier accepts peak-to-peak input voltages as small as 150mV as long as the common mode voltage is within the specified minimum and maximum range.

Guaranteed output and part-to-part skew characteristics make the ICS8530-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

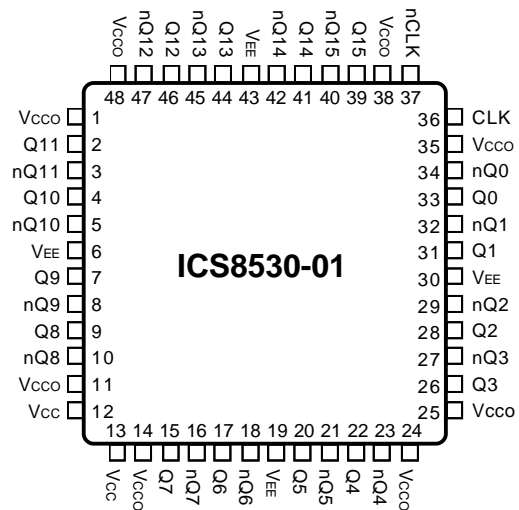
## FEATURES

- 16 differential 3.3V LVPECL outputs
- CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 500MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with a resistor bias on nCLK input
- Output skew: 75ps (maximum)
- Part-to-part skew: 250ps (maximum)
- 3.3V output operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**48-Pin LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	V <sub>CCO</sub>	Power		Output supply pins. Connect to 3.3V.
2, 3	Q11, nQ11	Output		Differential output pair. LVPECL interface levels.
4, 5	Q10, nQ10	Output		Differential output pair. LVPECL interface levels.
6, 19, 30, 43	V <sub>EE</sub>	Power		Negative supply pins. Connect to ground.
7, 8	Q9, nQ9	Output		Differential output pair. LVPECL interface levels.
9, 10	Q8, nQ8	Output		Differential output pair. LVPECL interface levels.
12, 13	V <sub>CC</sub>	Power		Positive supply pins. Connect to 3.3V.
15, 16	Q7, nQ7	Output		Differential output pair. LVPECL interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVPECL interface levels.
20, 21	Q5, nQ5	Output		Differential output pair. LVPECL interface levels..
22, 23	Q4, nQ4	Output		Differential output pair. LVPECL interface levels.
26, 27	Q3, nQ3	Output		Differential output pair. LVPECL interface levels.
28, 29	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
36	CLK	Input	Pulldown	Non-inverting differential clock input.
37	nCLK	Input	Pullup	Inverting differential clock input.
39, 40	Q15, nQ15	Output		Differential output pair. LVPECL interface levels.
41, 42	Q14, nQ14	Output		Differential output pair. LVPECL interface levels.
44, 45	Q13, nQ13	Output		Differential output pair. LVPECL interface levels.
46, 47	Q12, nQ12	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	CLK, nCLK				4	pF
R <sub>PULLUP</sub>	Input Pullup Resistor				51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				51		KΩ

**TABLE 3. FUNCTION TABLE**

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 7, Figure 8, which discusses wiring the differential input to accept single ended levels.



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CCx}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{CCO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W
Storage Temperature, $T_{STG}$	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Input/core Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				120	mA

**TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nCLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .



**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = V_{CC0} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Maximum Output Frequency				500	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 500MHz$	1		2	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				75	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			88	250	ps
$t_R$	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
$t_F$	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47	50	53	%

All parameters measured at 250MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

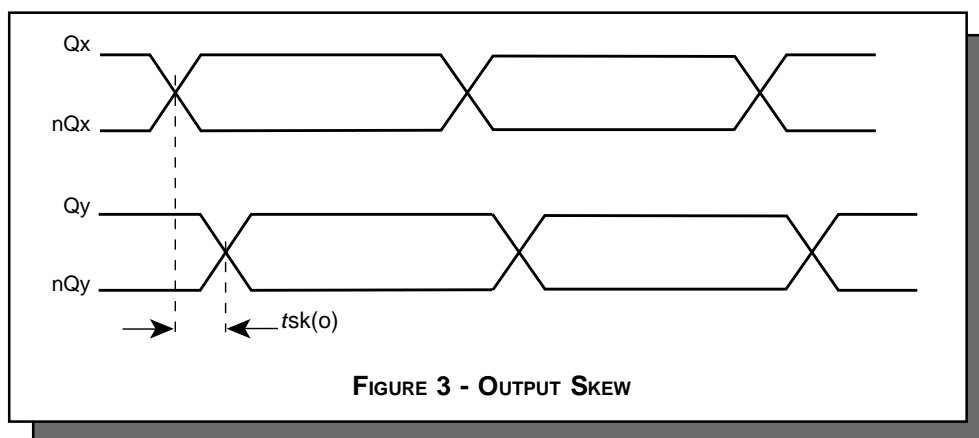
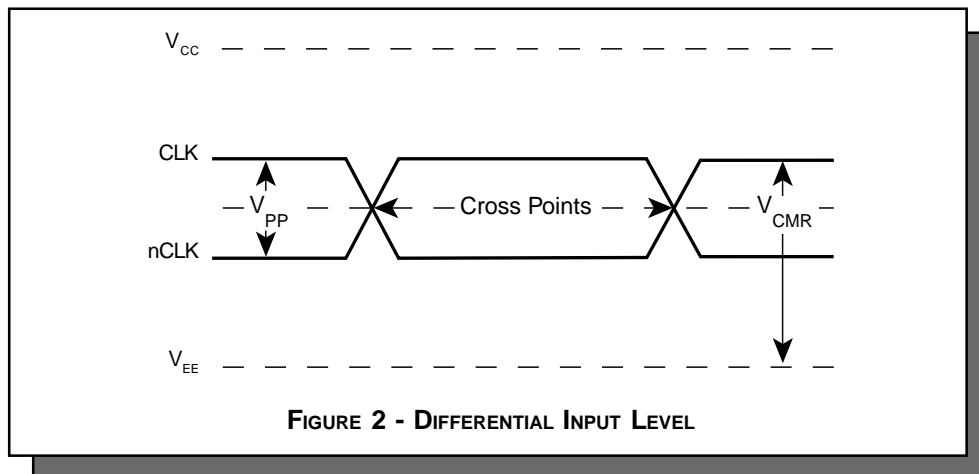
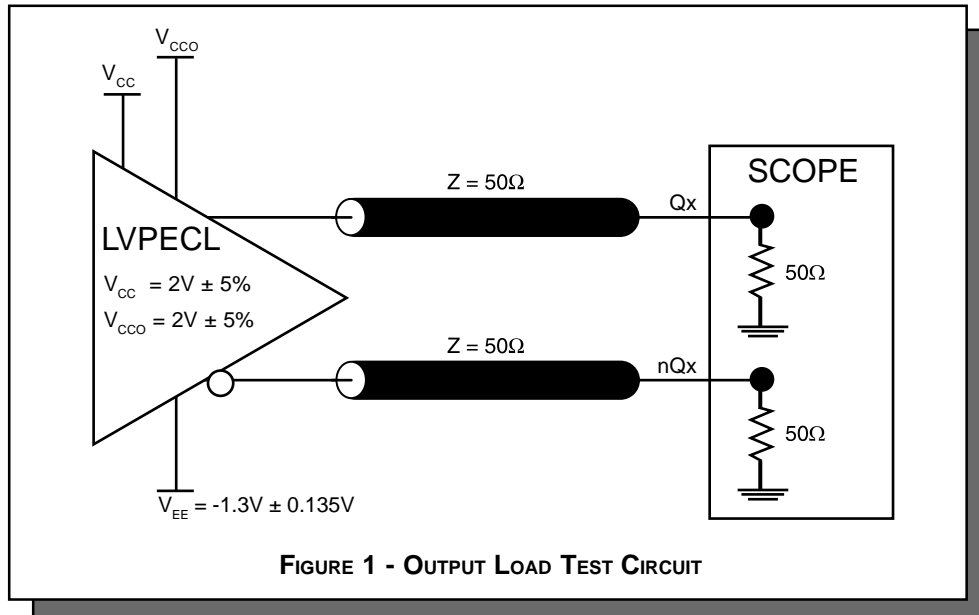
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

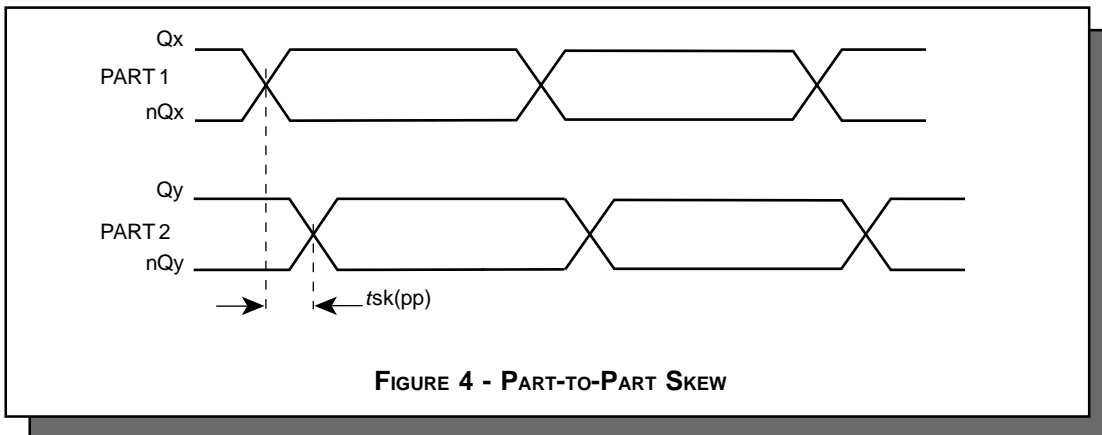
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

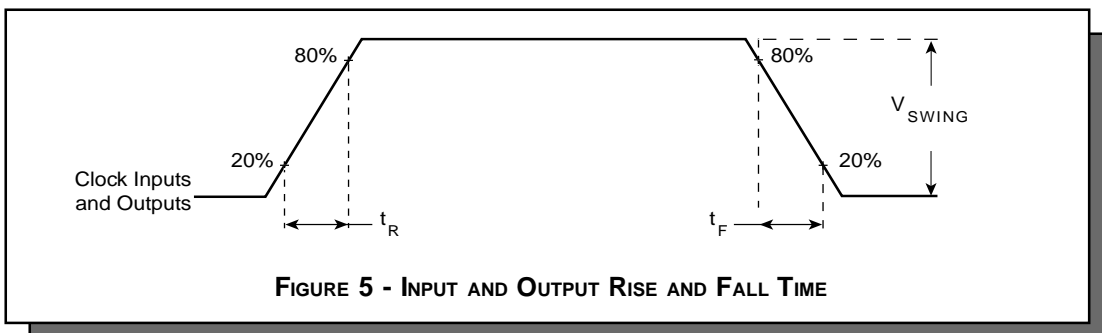


## PARAMETER MEASUREMENT INFORMATION

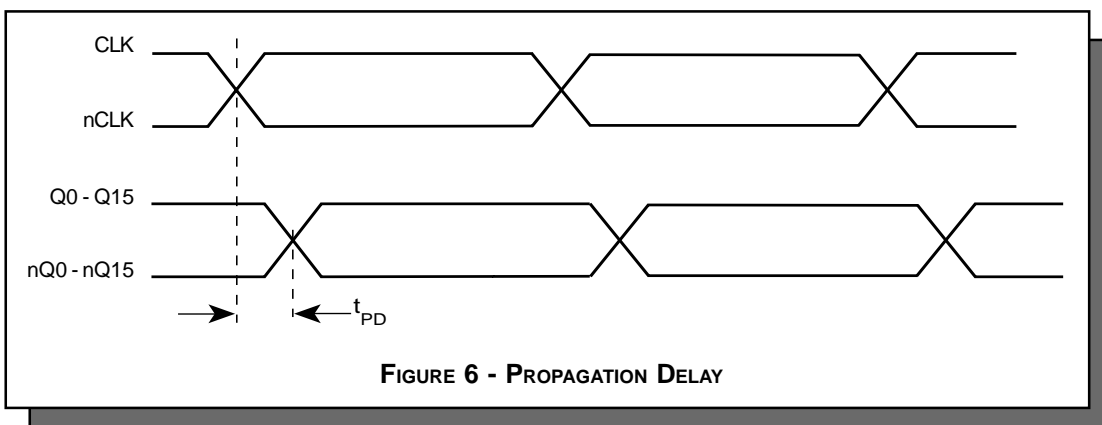




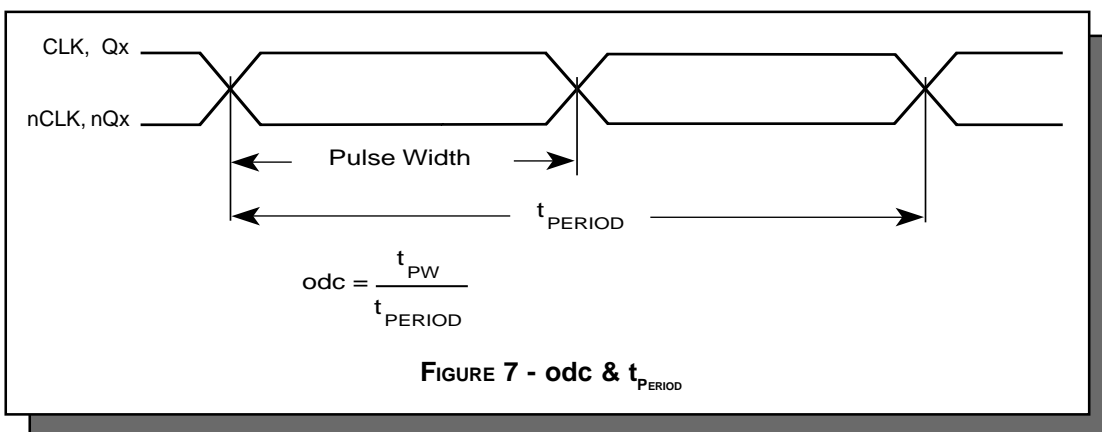
**FIGURE 4 - PART-TO-PART SKEW**



**FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME**



**FIGURE 6 - PROPAGATION DELAY**



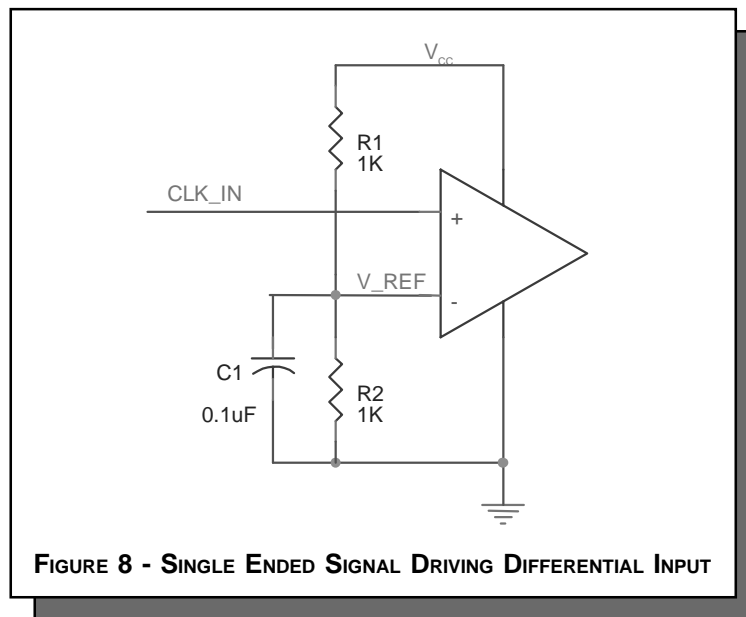
**FIGURE 7 - odc &  $t_{PERIOD}$**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .





## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8530-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8530-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 120mA = 415.8mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $16 * 30.2mW = 483.2mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $415.8mW + 483.2mW = 899mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 47.9°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.899W * 47.9^\circ C/W = 113.1^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 48-pin LQFP, Forced Convection**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

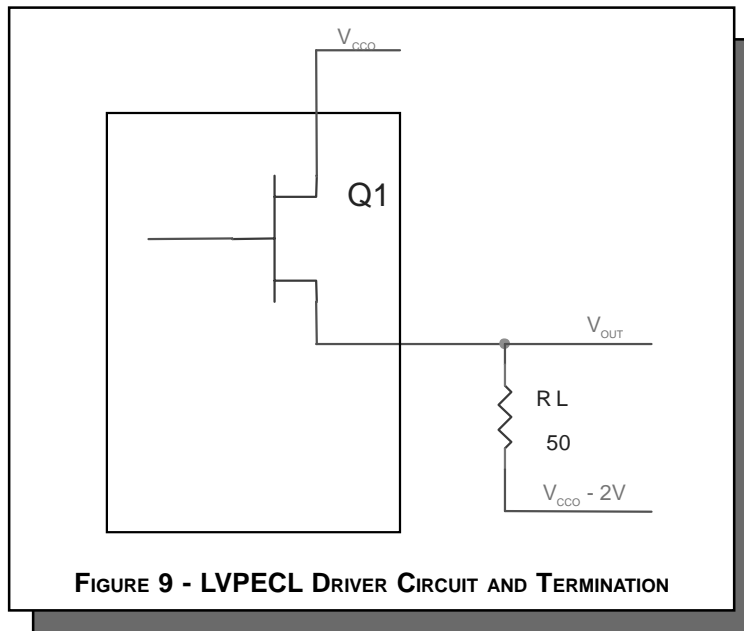




### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

$Pd_H$  is power dissipation when the output drives high.  
 $Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OH\_MAX})$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OL\_MAX})$$

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 1.0V$   
 Using  $V_{CC\_MAX} = 2.625$ , this results in  $V_{OH\_MAX} = 1.625V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
 Using  $V_{CC\_MAX} = 2.625$ , this results in  $V_{OL\_MAX} = 0.925V$

$$Pd_H = [(1.625V - (2.625V - 2V)) / 50 \Omega] * (1V) = 20mW$$

$$Pd_L = [(0.925V - (2.625V - 2V)) / 50 \Omega] * (1.7) = 10.2mW$$

Total Power Dissipation per output pair =  $Pd_H + Pd_L = 30.2mW$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8530-01 is: 930



PACKAGE OUTLINE - Y SUFFIX

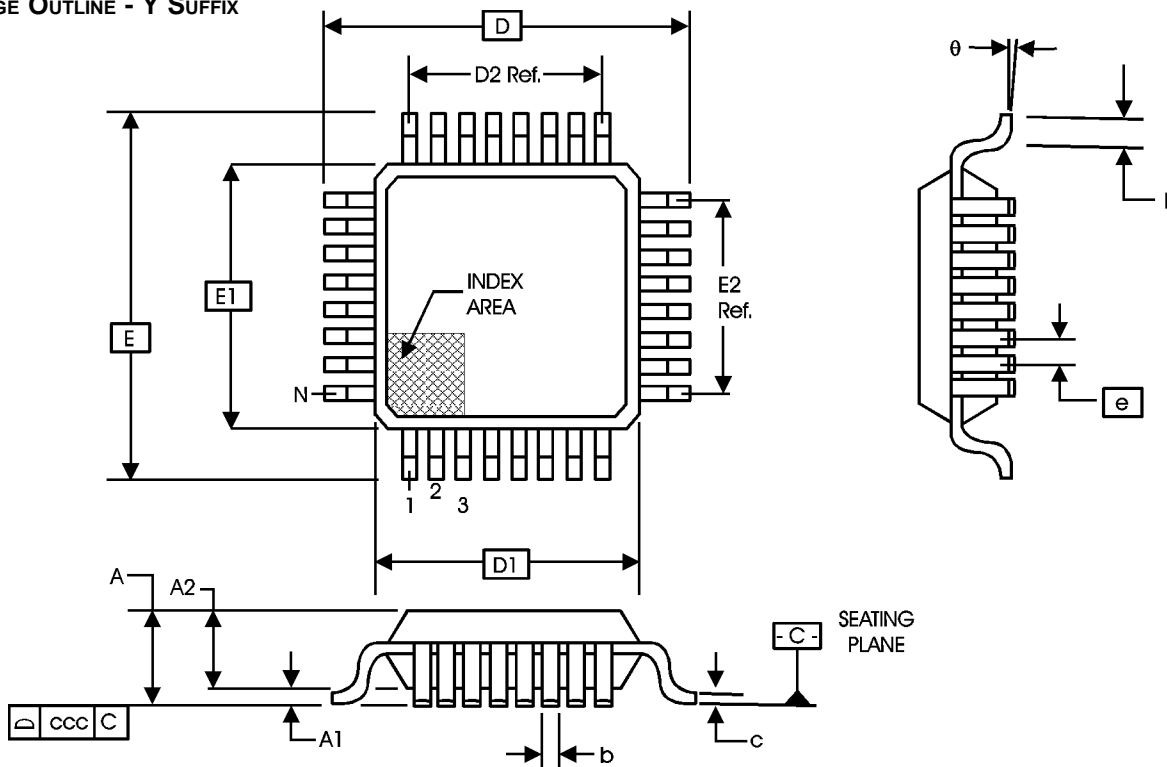


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
$\theta$	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

**ICS8530-01**  
LOW SKEW, 1-TO-16  
DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS8530DY-01	ICS8530DY-01	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8530DY-01T	ICS8530DY-01	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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