Integrated Circuit Systems, Inc.

ICS853013

LOW SKEW, DUAL, 1-TO-3, DIFFERENTIAL-TO-2.5V/3.3V/5V LVPECL/ECL FANOUT BUFFER

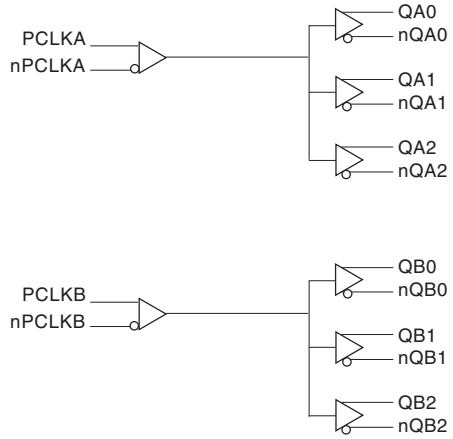
GENERAL DESCRIPTION

The ICS853013 is a low skew, high performance dual 1-to-3 Differential-to-2.5V/3.3V/5V LVPECL/ECL Fanout Buffer and a member of the Hiperclocks™ family of High Performance Clock Solutions from ICS. The ICS853013 operates with a positive or negative power supply at 2.5V, 3.3V, or 5V. Guaranteed output and part-to-part skew characteristics make the ICS853013 ideal for those clock distribution applications demanding well defined performance and repeatability.

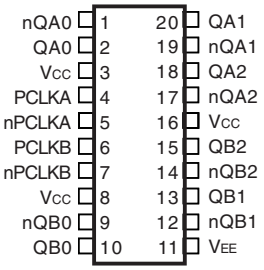
FEATURES

- Two differential LVPECL / ECL bank outputs
- Two differential LVPECL clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2GHz (typical)
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx input
- Output skew: 40ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 570ps (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 5.25V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -5.25V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS853013
20-Lead, 300-MIL SOIC
7.5mm x 12.8mm x 2.3mm body package
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
3, 8, 16	V_{CC}	Power		Power supply pins.
4	PCLKA	Input	Pulldown	Non-inverting differential LVPECL clock input.
5	nPCLKA	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
6	PCLKB	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
9, 10	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
14, 15	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
17, 18	nQA2, QA2	Output		Differential output pair. LVPECL interface levels.
19, 20	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLKA or PCLKB	nPCLKA or nPCLKB	QA0:QA2, QB0:QB2	nQA0:nQA2, nQB0:nQB2		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	5.5V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-5.5V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	46.2°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375 TO 5.25V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	3.3	5.25	V
I_{EE}	Power Supply Current				60	mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLKA, PCLKB nPCLKA, nPCLKB			150			150			150	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	-10			-10			-10			µA
		nPCLKA, nPCLKB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKA, nPCLKB and PCLKA, nPCLKB is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.495	1.53	1.565	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage(Single-Ended)		1.275		1.56	1.275		1.56	1.275		-0.83	V
V_{IL}	Input Low Voltage(Single-Ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLKA, PCLKB nPCLKA, nPCLKB			150			150			150	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	-10			-10			-10			µA
		nPCLKA, nPCLKB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKA, nPCLKB and PCLKA, nPCLKB is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLKA, PCLKB nPCLKA, nPCLKB			150			150			150	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	-10			-10			-10			µA
		nPCLKA, nPCLKB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKA, nPCLKB and PCLKA, nPCLKB is V_{CC} + 0.3V.

TABLE 4E. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLKA, PCLKB nPCLKA, nPCLKB			150			150			150	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	-10			-10			-10			µA
		nPCLKA, nPCLKB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKA, nPCLKA and PCLKB, nPCLKB is V_{CC} + 0.3V.

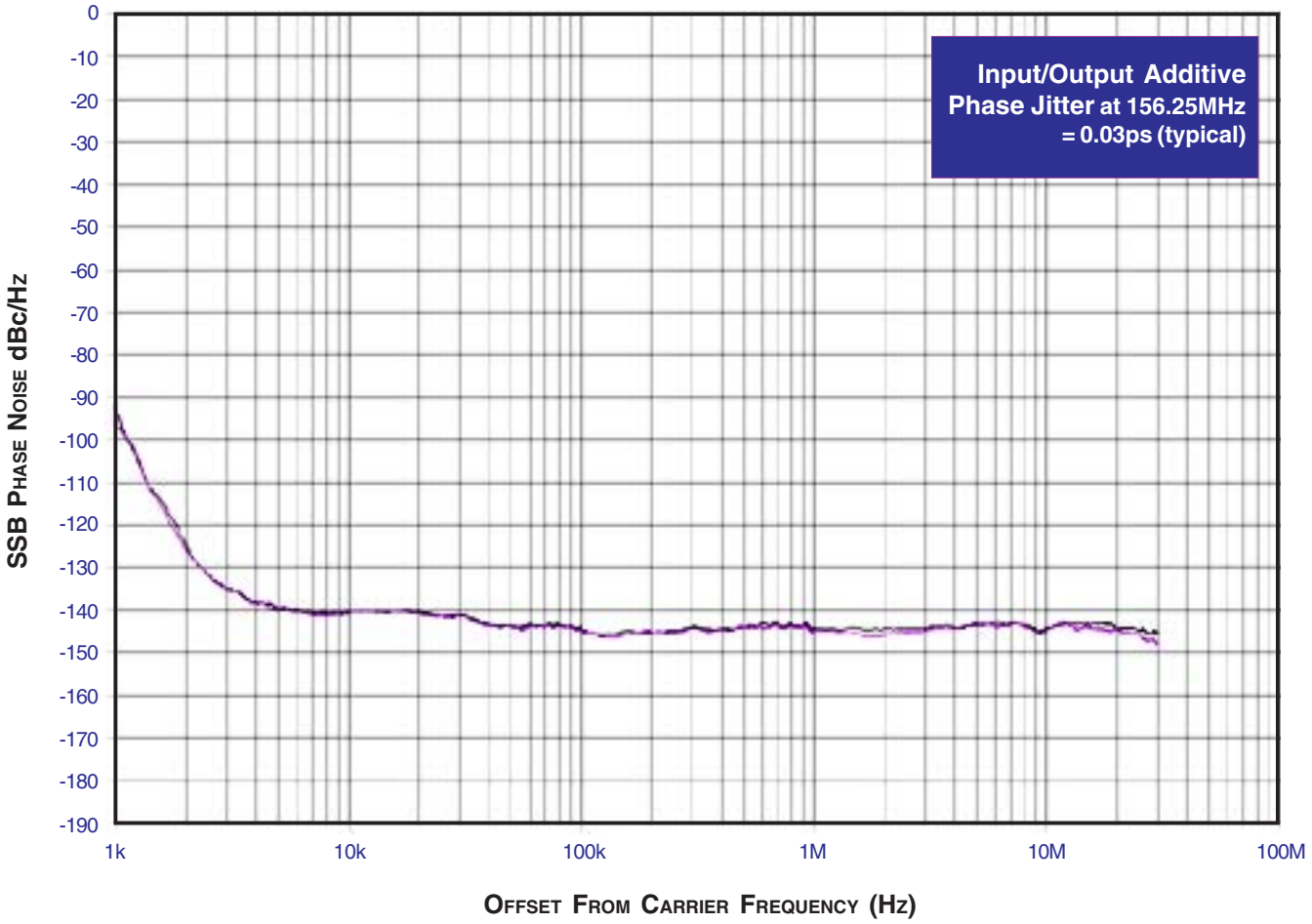
TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V OR V_{CC} = 2.375V TO 5.25V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>2			>2			>2		GHz
tP_{LH}	Propagation Delay, Low-to-High; NOTE 1		300	410	510	330	425	520	360	465	570	ps
tP_{HL}	Propagation Delay, High-to-Low; NOTE 1		300	410	510	330	425	520	360	465	570	ps
*t*sk(o)	Output Skew; NOTE 2, 4				40			40			40	ps
*t*sk(odc)	Output Duty Cycle Skew				40			40			40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250			250			250	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.03			0.03			0.03		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	120	180	250	140	180		150	190	230	ps

All parameters tested ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

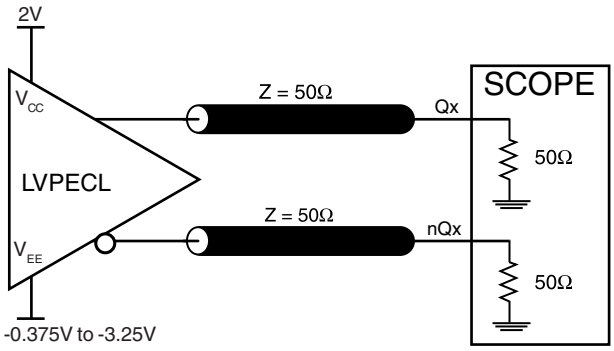
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

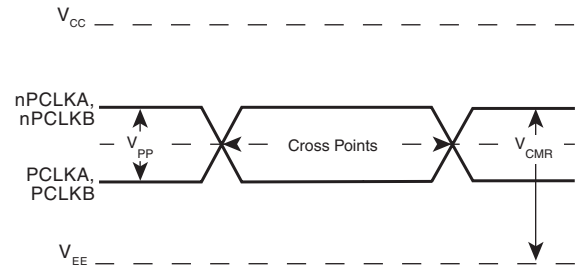


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

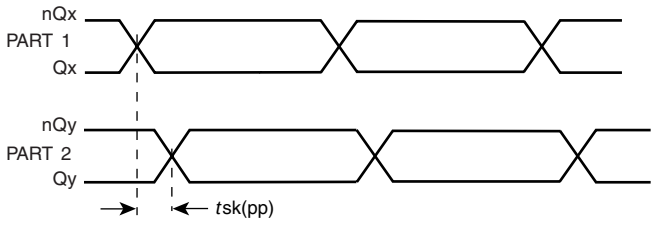
PARAMETER MEASUREMENT INFORMATION



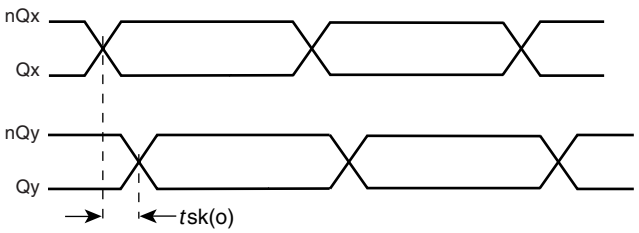
OUTPUT LOAD AC TEST CIRCUIT



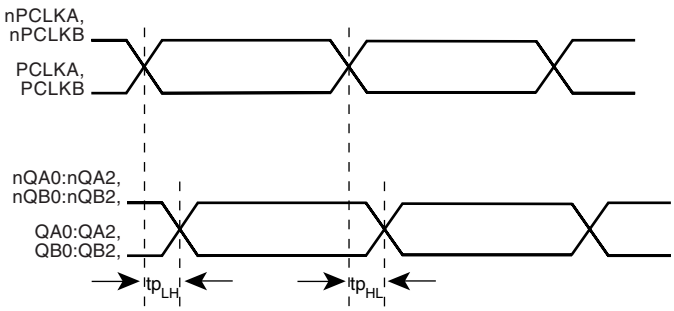
DIFFERENTIAL INPUT LEVEL



PART-TO-PART SKEW

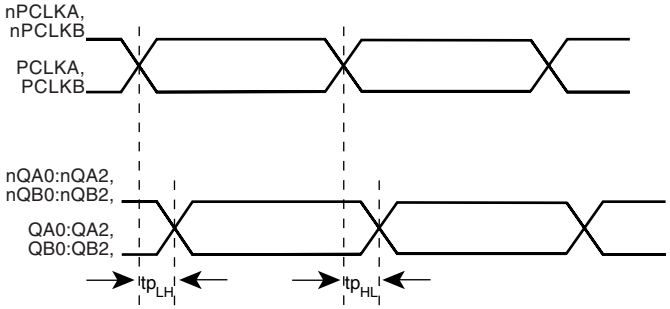


OUTPUT SKEW



$tsk(odc) = |tp_{LH} - tp_{HL}|$

OUTPUT DUTY CYCLE SKEW



PROPAGATION DELAY

OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF $\simeq V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

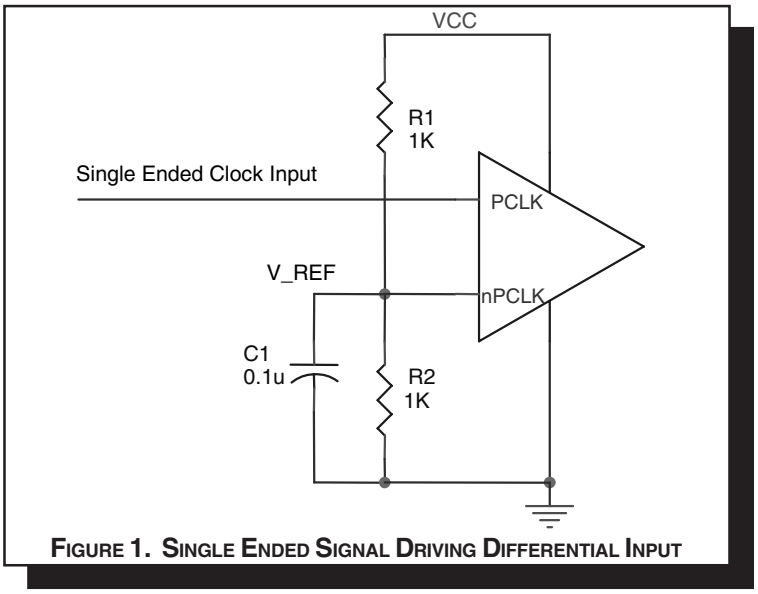


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL CLOCK INPUT INTERFACE

The PCLKx /nPCLKx accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLKx/nPCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

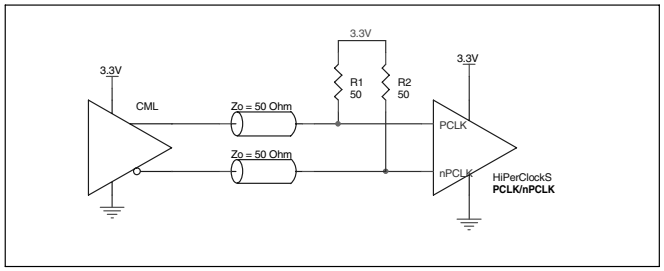


FIGURE 2A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

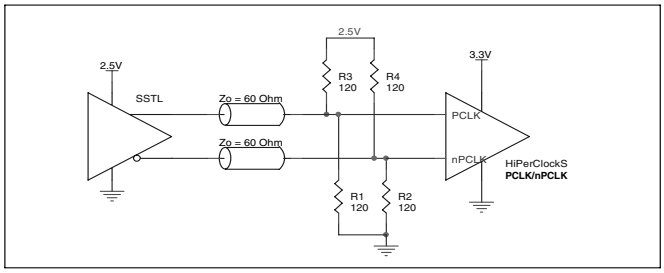


FIGURE 2B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

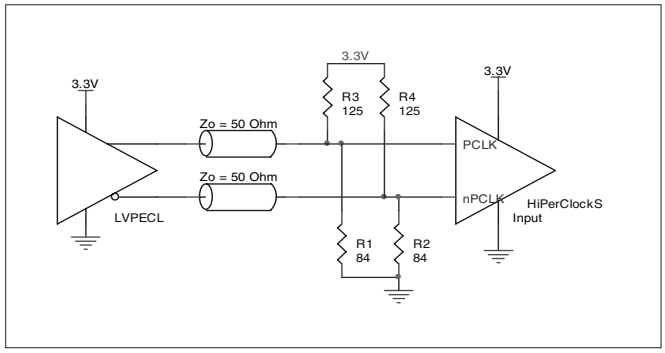


FIGURE 2C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

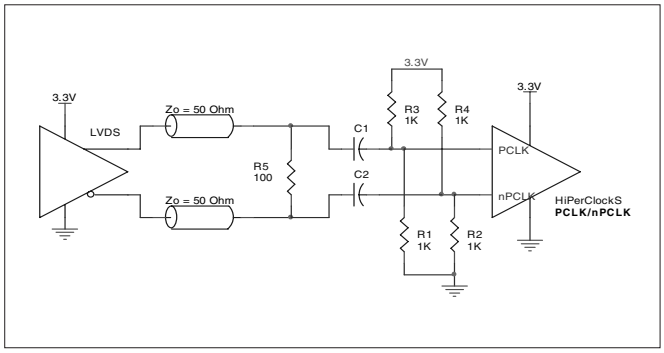


FIGURE 2D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

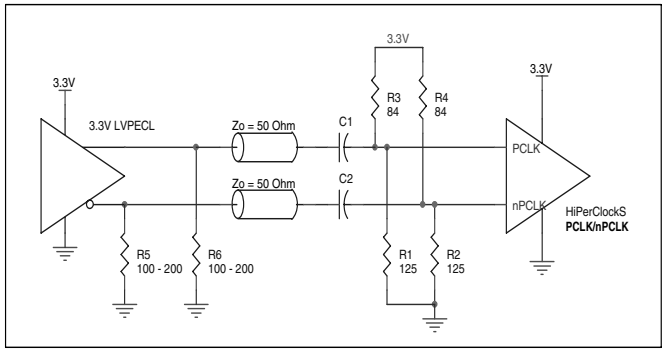


FIGURE 2E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

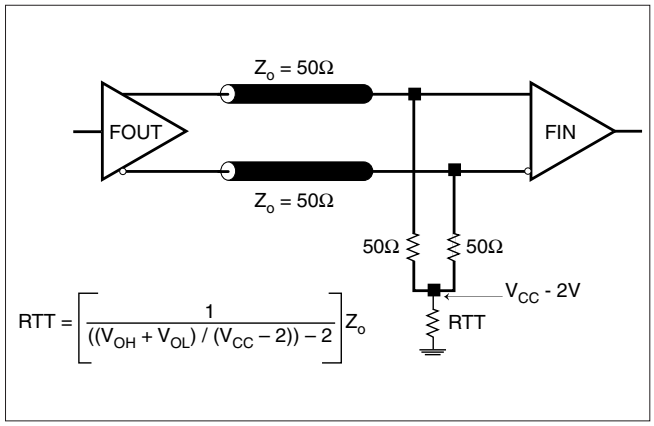


FIGURE 3A. LVPECL OUTPUT TERMINATION

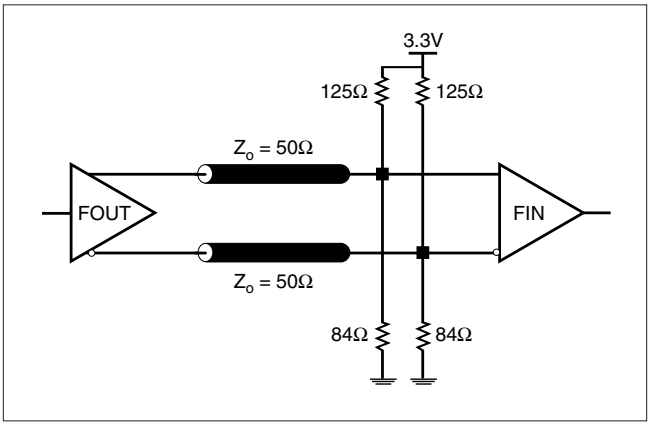


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

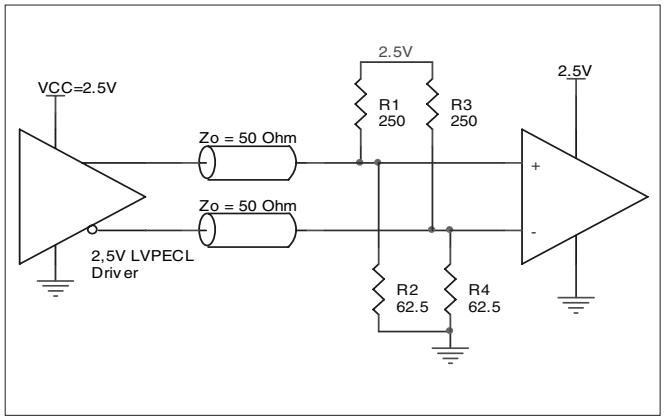


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

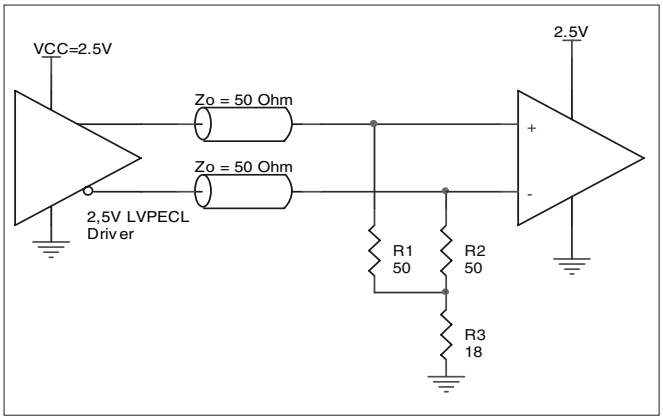


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

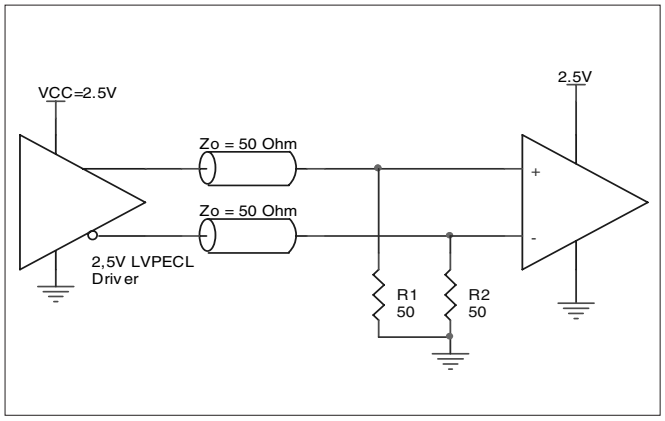


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853013.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853013 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 5.25V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 5.25V * 60mA = **315mW**
- Power (outputs)$_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30.94mW = **185.64mW**

Total Power$_{_MAX}$ (5.25V, with all outputs switching) = 315mW + 185.64mW = **500.64mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.500W * 39.7°C/W = 104.85°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN SOIC, FORCED CONVECTION

	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 5.

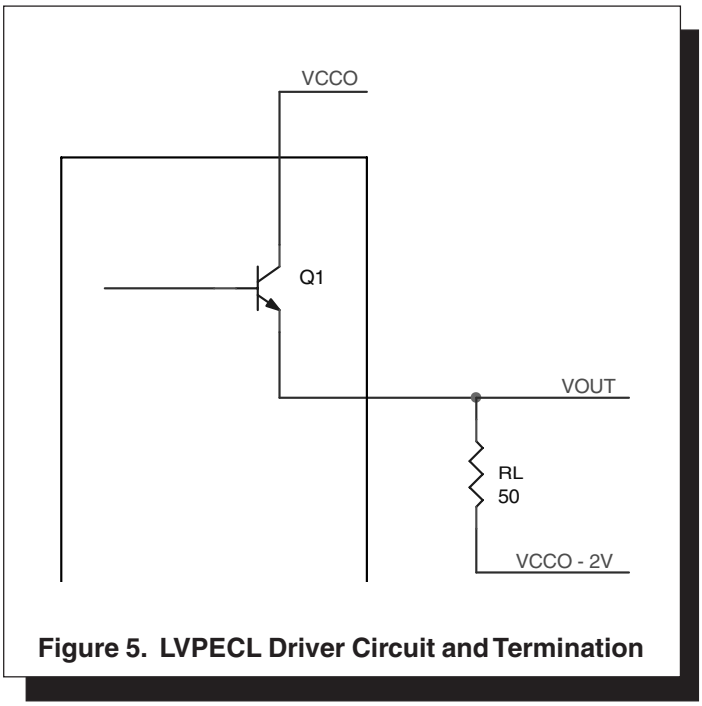


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.67V$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.67V$

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853013 is: 226

Pin compatible with MC100LVEL13, MC100EL13

PACKAGE OUTLINE - Y SUFFIX FOR 20 LEAD SOIC

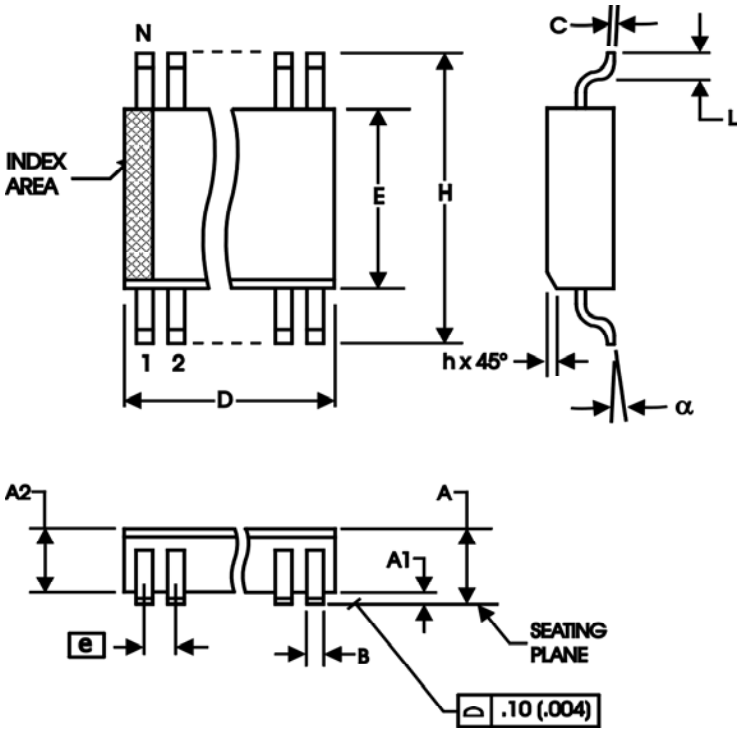


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853013AM	ICS853013AM	20 Lead SOIC	tube	-40°C to 85°C
ICS853013AMT	ICS853013AM	20 Lead SOIC	1000 tape & reel	-40°C to 85°C
ICS853013AMLF	ICS853013AMLF	20 Lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS853013AMLFT	ICS853013AMLF	20 Lead "Lead-Free" SOIC	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	8 16	Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free marking.	10/19/05