Integrated
Circuit
Systems, Inc.

ICS853017

QUAD, 1-TO-1
DIFFERENTIAL-TO-2.5V/3.3V/5V LVPECL/ECL RECEIVER

## GENERAL DESCRIPTION

ICS
HiPerClockS™

The ICS853017 is a quad 1-to-1, 2.5V/3.3V/5V differential LVPECL/ECL receiver and a member of the Hiperclocks™ family of High Performance Clock Solutions from ICS. The ICS853017 operates with a positive or negative power supply at 2.5V, 3.3V or 5V, and can accept both single-ended and differential inputs. For single-ended operation, an internally generated voltage, which is available on output pin V_{BB}, can be used as a switching bias voltage on the unused input of the differential pair. V_{BB} can also be used to rebias AC coupled inputs.

FEATURES

- 4 differential LVPECL / ECL 1:1 receivers

- 4 differential LVPECL clock input pairs

- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL

- Output frequency: >2GHz (typical)

- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx input

- Output skew: TBD

- Part-to-part skew: TBD

- Propagation delay: 320ps (typical)

- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 5.25V

- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -5.25V to -2.375V

- -40°C to 85°C ambient operating temperature

- Pin compatible with MC100LVEL17

BLOCK DIAGRAM
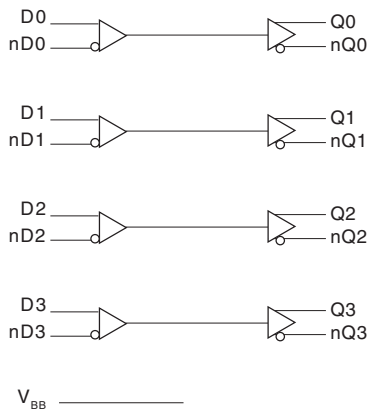
PIN ASSIGNMENT
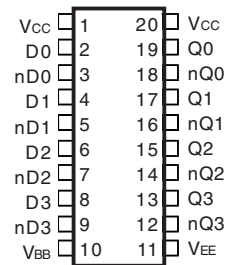
ICS853017
20-Lead, 300-MIL SOIC
7.5mm x 12.8mm x 2.3mm body package
M Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 20	V_{CC}	Power		Core supply pins.
2	D0	Input	Pulldown	Non-inverting differential clock input.
3	nD0	Input	Pullup/Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
4	D1	Input	Pulldown	Non-inverting differential clock input.
5	nD1	Input	Pullup/Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
6	D2	Input	Pulldown	Non-inverting differential clock input.
7	nD2	Input	Pullup/Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
8	D3	Input	Pulldown	Non-inverting differential clock input.
9	nD3	Input	Pullup/Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
10	V_{BB}	Power		Bias Voltage.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		KΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
D0:D3	nD0:nD3	Q0:Q3	nQ0:nQ3,		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 5.5V (LVPECL mode, V_{EE} = 0)

Negative Supply Voltage, V_{EE} -5.5V (ECL mode, V_{CC} = 0)

Inputs, V_I (LVPECL mode)   -0.5V to V_{CC} + 0.5V

Inputs, V_I (ECL mode)   0.5V to V_{EE} - 0.5V

Outputs, I_O
    Continuous Current   50mA
    Surge Current   100mA

  V_{BB} Sing/Source, I_{BB} ± 0.5mA

Operating Temperature Range, TA   -40°C to +85°C

Storage Temperature, T_{STG} -65°C to 150°C

Package Thermal Impedance, θ_{JA} 46.2°C/W (0 lfpm)
  (Junction-to-Ambient)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 5.25V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	3.3	5.25	V
I_{EE}	Power Supply Current			46		mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C		Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
V_{OH}	Output High Voltage; NOTE 1			2.275			2.295			2.33		V
V_{OL}	Output Low Voltage; NOTE 1			1.545			1.52			1.535		V
V_{IH}	Input High Voltage(Single-Ended)		2.075			2.075			2.075			V
V_{IL}	Input Low Voltage(Single-Ended)		1.43			1.43			1.43			V
V_{BB}	Output Voltage Reference; NOTE 2		1.86			1.86			1.86			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1,n D2, nD3			150			150			150	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1,n D2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. V_{CC} ≥ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			1.475			1.495			1.53		V
V_{OL}	Output Low Voltage; NOTE 1			0.745			0.72			0.735		V
V_{IH}	Input High Voltage(Single-Ended)		1.275			1.275			1.275			V
V_{IL}	Input Low Voltage(Single-Ended)		0.63			0.63			0.63			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1,n D2, nD3			150			150			150	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1,n D2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			3.975			3.995			4.03		V
V_{OL}	Output Low Voltage; NOTE 1			3.245			3.22			3.235		V
V_{IH}	Input High Voltage(Single-Ended)		3.775			3.775			3.775			V
V_{IL}	Input Low Voltage(Single-Ended)		3.13			3.13			3.13			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		5	1.2		5	1.2		5	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1,n D2, nD3			150			150			150	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1,n D2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 4C. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			-1.025			-1.005			-0.97		V
V_{OL}	Output Low Voltage; NOTE 1			-1.755			-1.78			-1.765		V
V_{IH}	Input High Voltage(Single-Ended)		-1.225			-1.225			-1.225			V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87			-1.87			-1.87			V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44			-1.44			-1.44			V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1,n D2, nD3			150			150			150	μA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			μA
		nD0, nD1,n D2, nD3	-150			-150			-150			μA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. V_{CC} ≥ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for Dx, nDx is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V OR V_{CC} = 2.375V TO 5.25V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>2			>2			>2		GHz
tP_{LH}	Propagation Delay, Low-to-High; NOTE 1			320			320			320		ps
tP_{HL}	Propagation Delay, High-to-Low; NOTE 1			320			320			320		ps
$tsk(o)$	Output Skew; NOTE 2, 4			TBD			TBD			TBD		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4			TBD			TBD			TBD		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		175			175			175		ps

All parameters tested ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
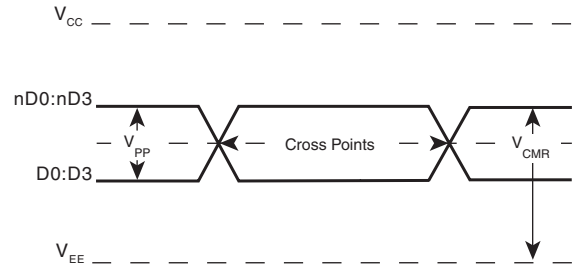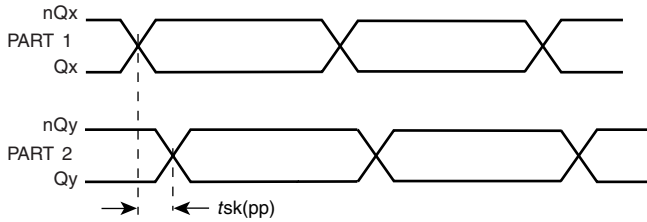NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
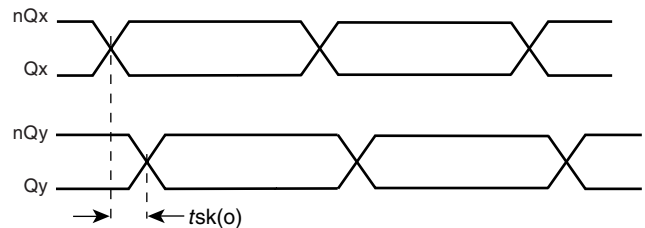
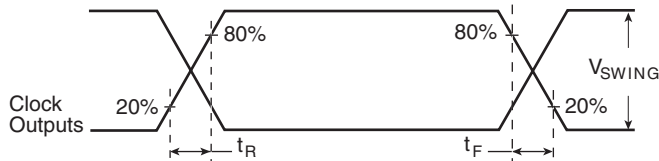## PARAMETER MEASUREMENT INFORMATION
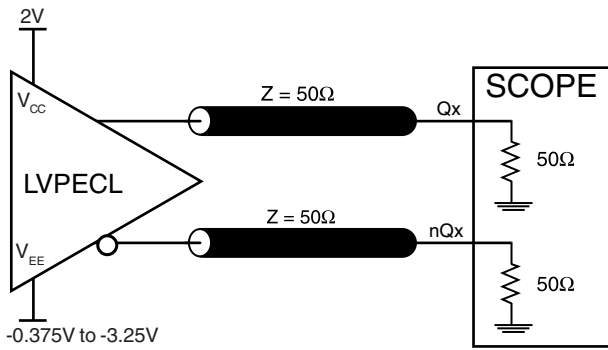
OUTPUT LOAD AC TEST CIRCUIT

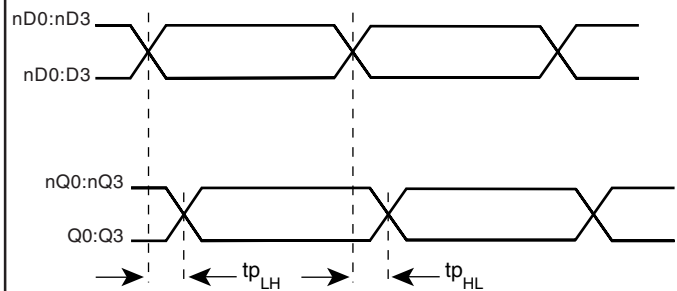**DIFFERENTIAL INPUT LEVEL**

PART-TO-PART SKEW

OUTPUT SKEW

OUTPUT RISE/FALL TIME


PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT
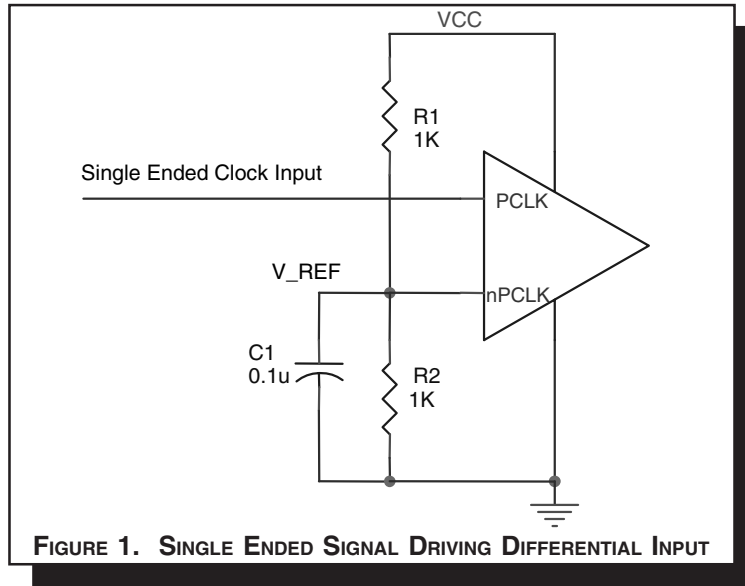
TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2} \right] Z_o$$
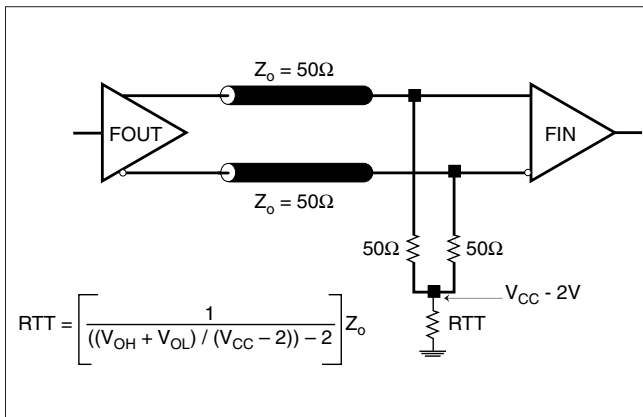
FIGURE 2A. LVPECL OUTPUT TERMINATION
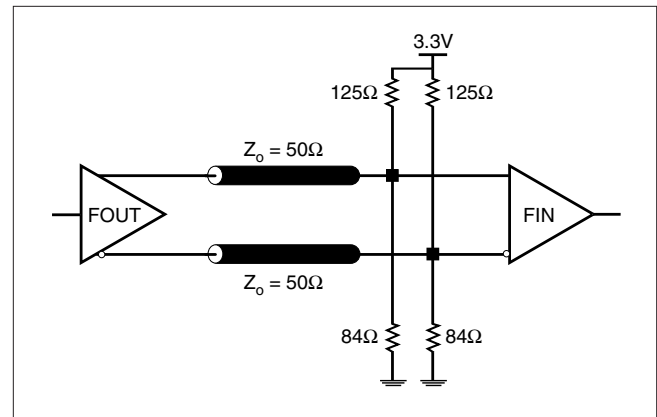
FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C*.
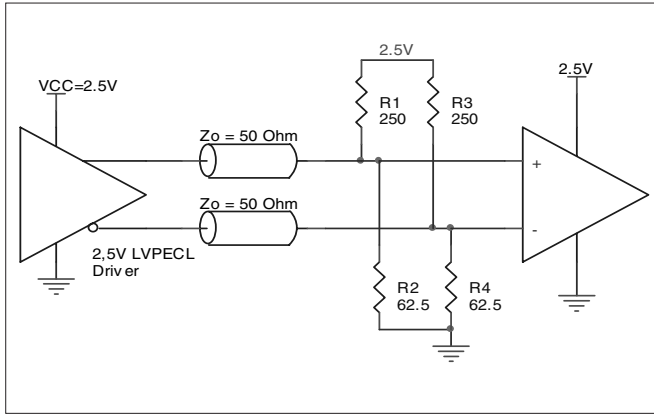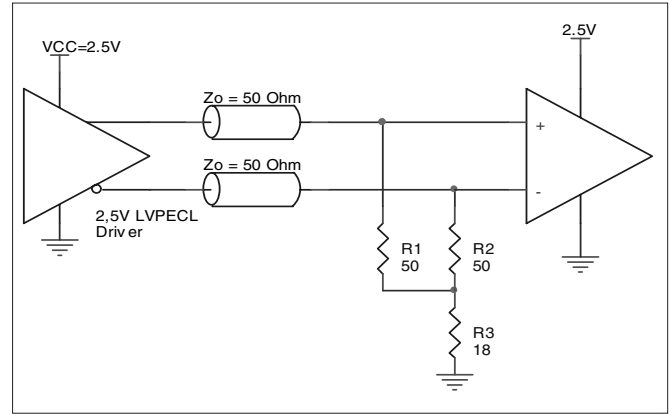

FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE
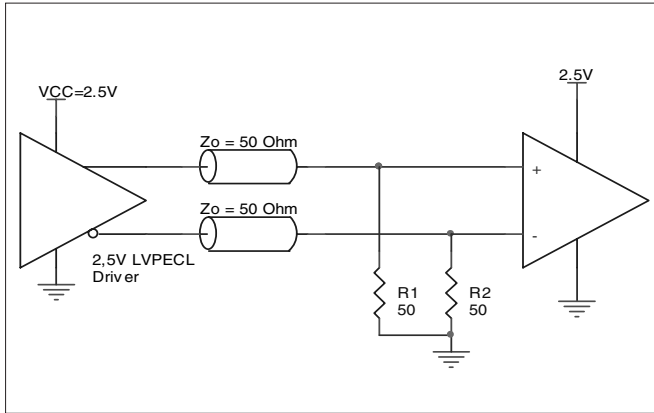

FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

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LVPECL CLOCK INPUT INTERFACE

The PCLKx /nPCLKx accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the HiPerClockS PCLKx/nPCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.
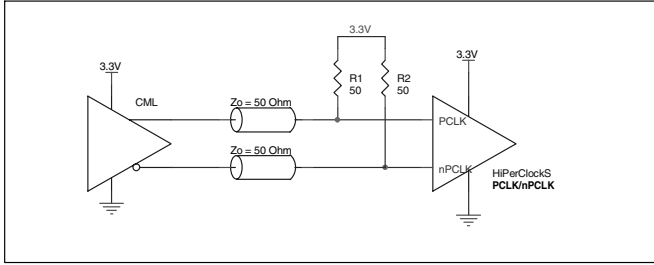
FIGURE 4A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER
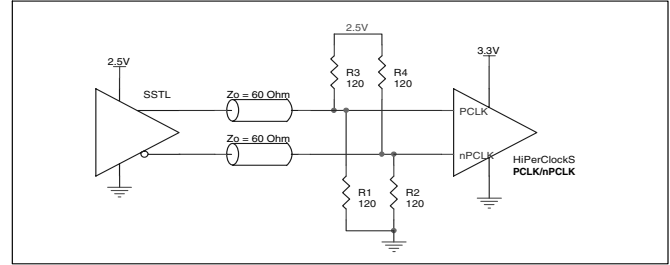
FIGURE 4B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER
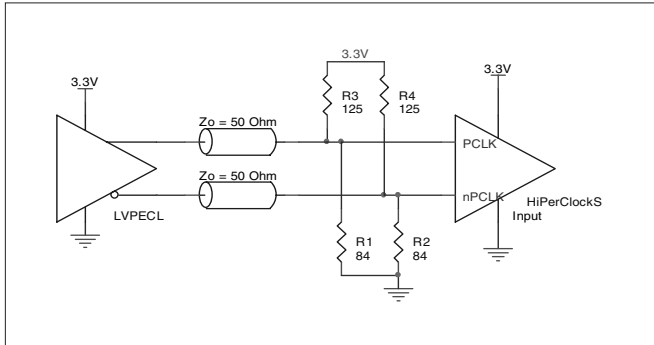
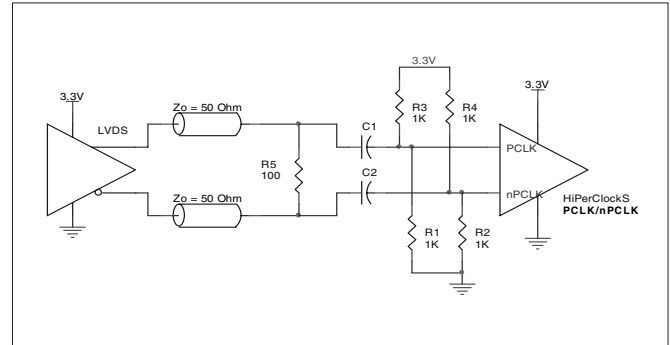FIGURE 4C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

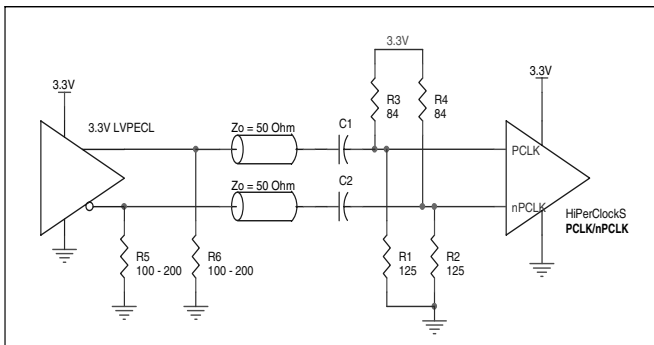FIGURE 4D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

FIGURE 4E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

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RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853017 is: 187

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PACKAGE OUTLINE - Y SUFFIX FOR 20 LEAD SOIC
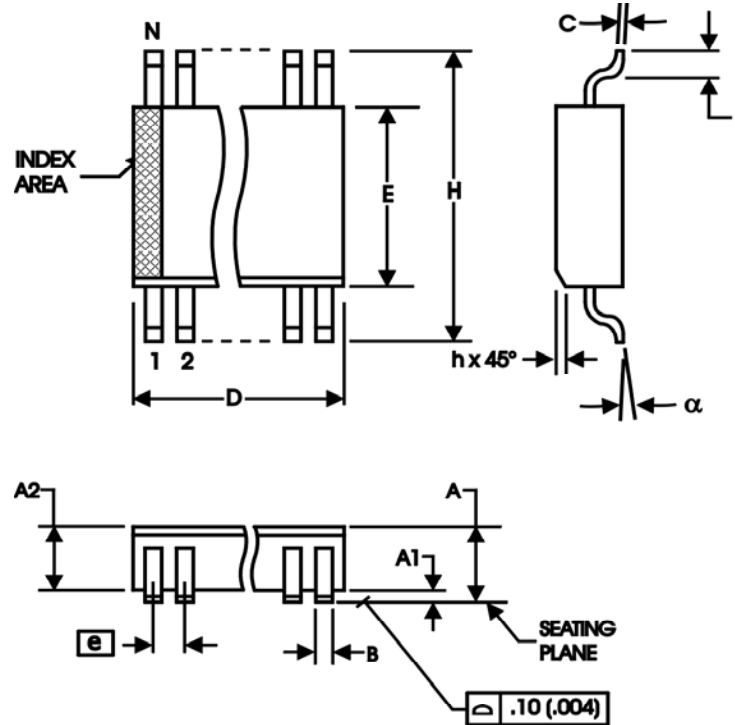
TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS853017AM	ICS853017AM	20 Lead SOIC	38 per tube	-40°C to 85°C
ICS853017AMT	ICS853017AM	20 Lead SOIC on Tape and Reel	1000	-40°C to 85°C