



## GENERAL DESCRIPTION

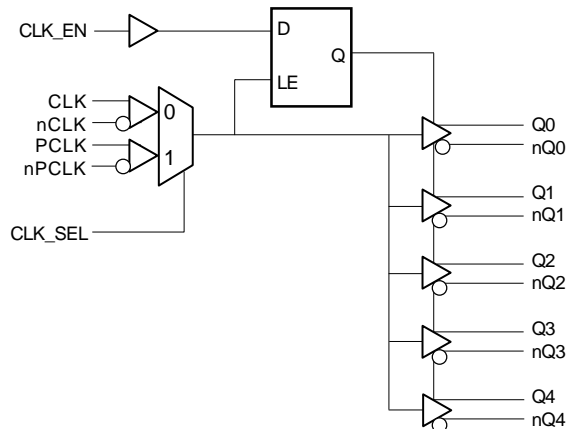
The ICS85304-01 is a low skew, high performance 1-to-5 Differential-to-3.3V LVPECL fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85304-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt clock pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS85304-01 ideal for those applications demanding well defined performance and repeatability.

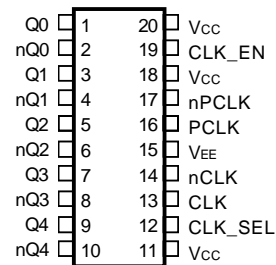
## FEATURES

- 5 differential 3.3V LVPECL outputs
- Selectable CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency up to 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 35ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2.1ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### ICS85304-01 20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm Package Body

**G Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVPECL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVPECL interface levels.
11, 18, 20	V <sub>CC</sub>	Power		Positive supply pins. Connect to 3.3V.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVTTTL / LVCMOS interface levels.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
15	V <sub>EE</sub>	Power		Negative supply pin. Connect to ground.
16	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
19	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVTTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	CLK, nCLK				4	pF
		PCLK, nPCLK				4	pF
		CLK_EN, CLK_SEL				4	pF
R <sub>PULLUP</sub>	Input Pullup Resistor				51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				51		KΩ

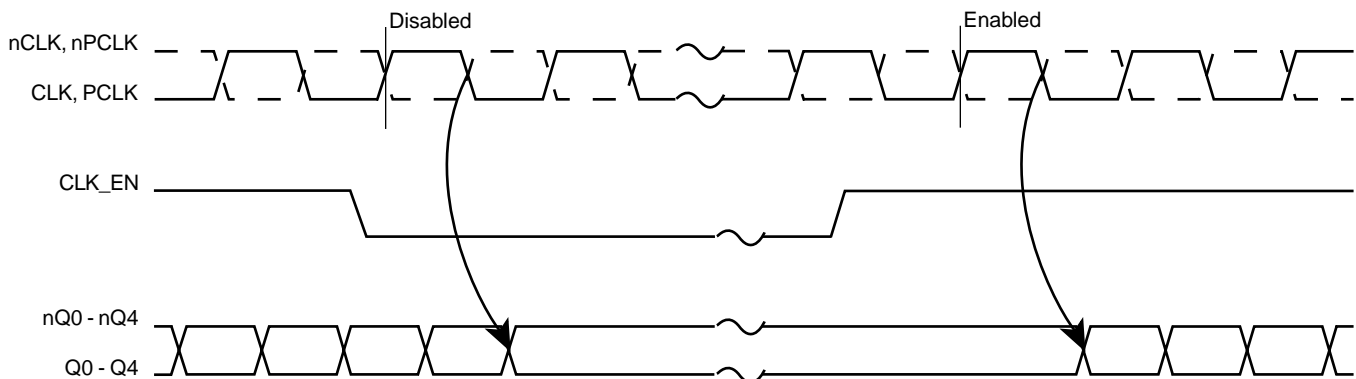


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0 thru Q4	nQ0 thru nQ4
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.



**FIGURE 1 - CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

Inputs		Outputs		Input to Output Mode	Polarity
CLK or CLK	nPCLK or nPCLK	Q0 thru Q4	nQ0 thru nQ4		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 8, Figure 8, which discusses wiring the differential input to accept single ended levels.



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CCx}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{CC} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0lfpn)
Storage Temperature, $T_{STG}$	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY CHARACTERISTICS,  $V_{CC}=3.3V\pm5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				55	mA

**TABLE 4B. LVCMOS / LVTTTL CHARACTERISTICS,  $V_{CC}=3.3V\pm5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	CLK_EN, CLK_SEL	2		3.765	V
$V_{IL}$	Input Low Voltage	CLK_EN, CLK_SEL	-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_EN	$V_{IN} = V_{CC} = 3.465V$		5	$\mu A$
		CLK_SEL	$V_{IN} = V_{CC} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	CLK_EN	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		CLK_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC}=3.3V\pm5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	nCLK	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
		CLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	nCLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		CLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC}=3.3V\pm5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nPCLK	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	PCLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nPCLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{CC} - 0.85$	V
$V_{OH}$	Output High Voltage; NOTE 3		$V_{CC} - 1.4$		$V_{CC} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 3		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications the maximum input voltage for PCLK, nPCLK is  $V_{CC} + 0.3V$ .

NOTE 3: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC}=3.3V\pm5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Maximum Output Frequency				650	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 650MHz$	1.0		2.1	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				35	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				150	ps
$t_R$	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
$t_F$	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	ps

All parameters measured at 500MHz unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

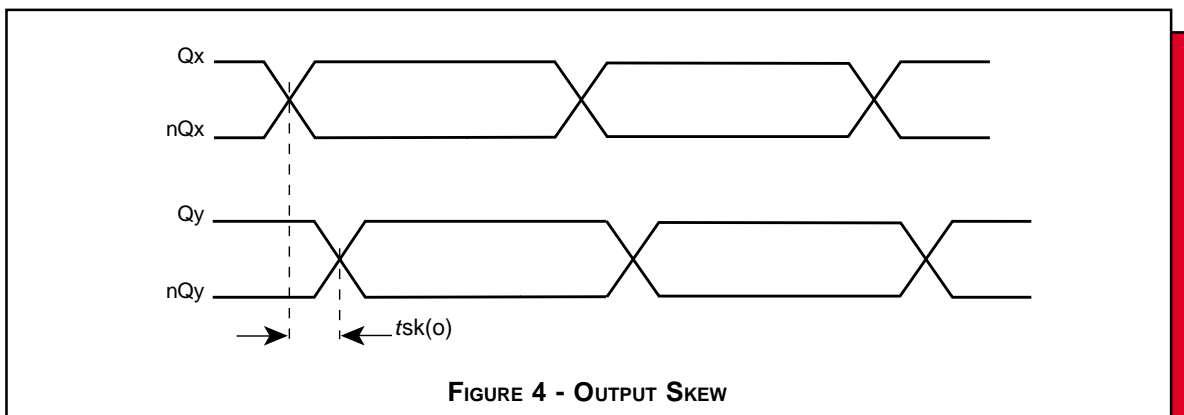
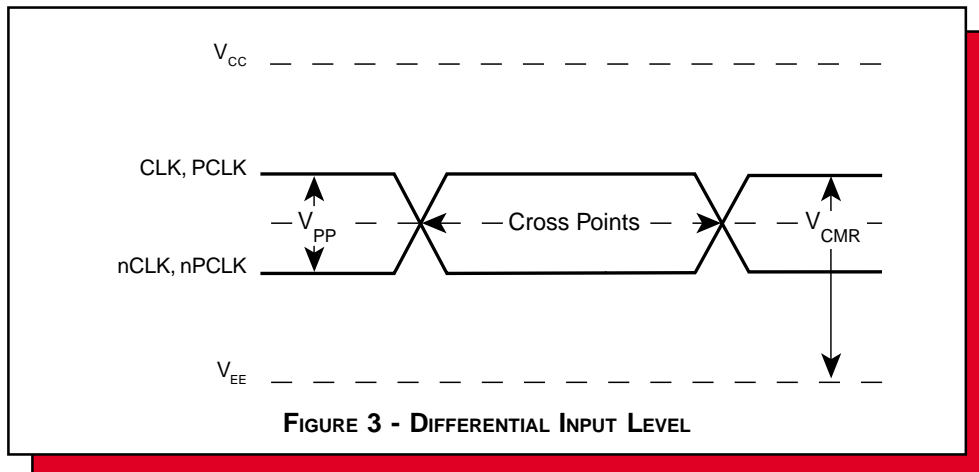
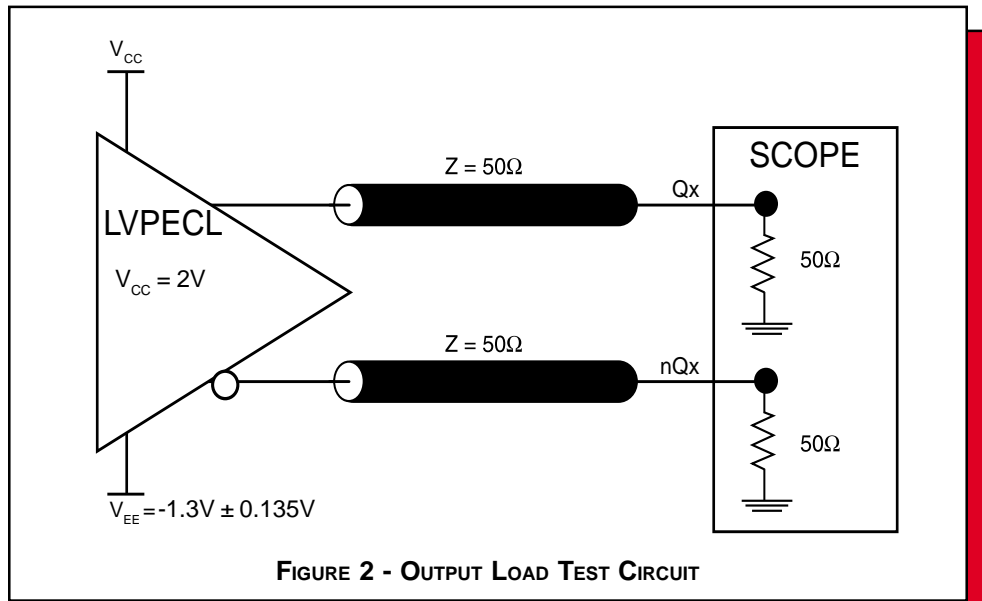
Measured at the output differential cross points.

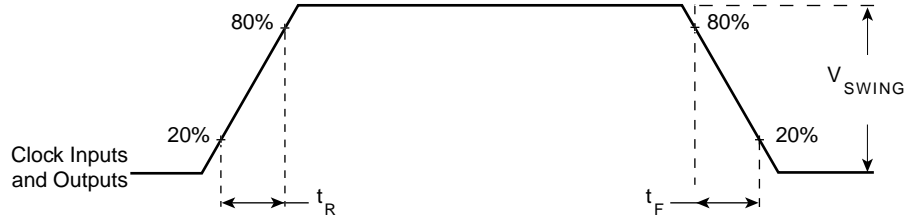
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

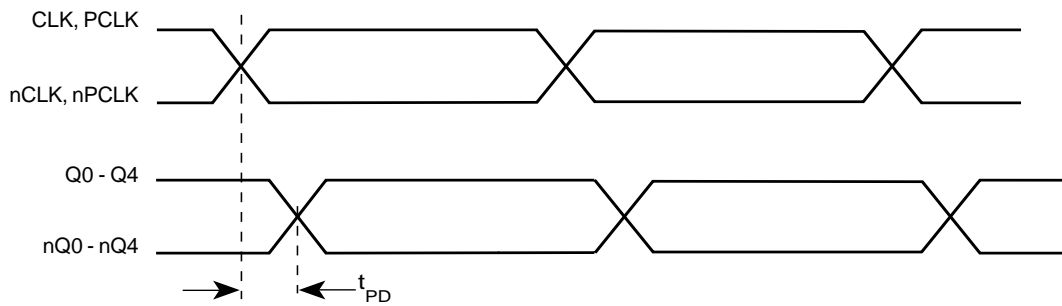


### PARAMETER MEASUREMENT INFORMATION

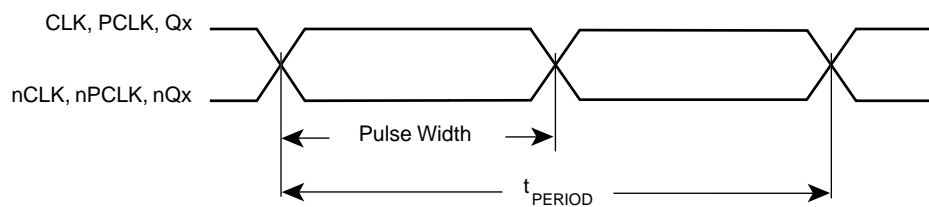




**FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME**



**FIGURE 6 - PROPAGATION DELAY**



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**FIGURE 7 - odc &  $t_{PERIOD}$**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

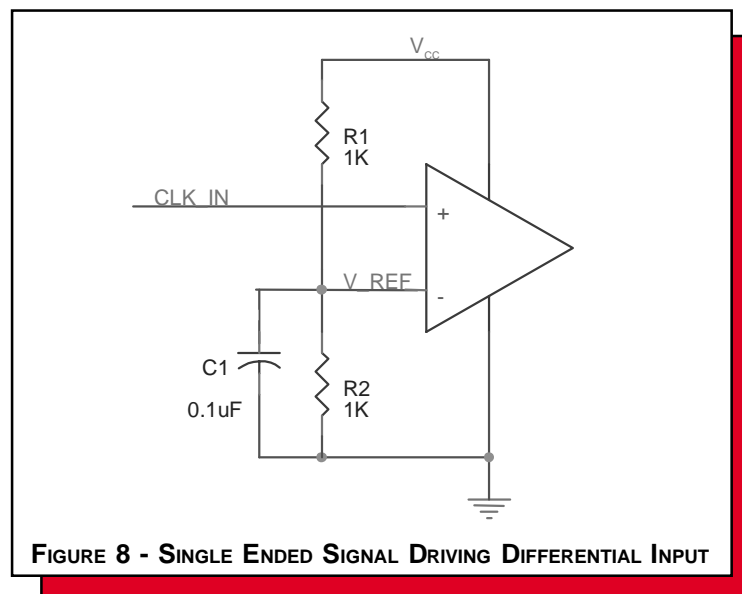


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT





## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85304-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85304-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 55mA = 190.57mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 30.2mW = 151mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.57mW + 151mW = 341.57mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.341W * 66.6^\circ C/W = 92.71^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 20-pin TSSOP, Forced Convection**

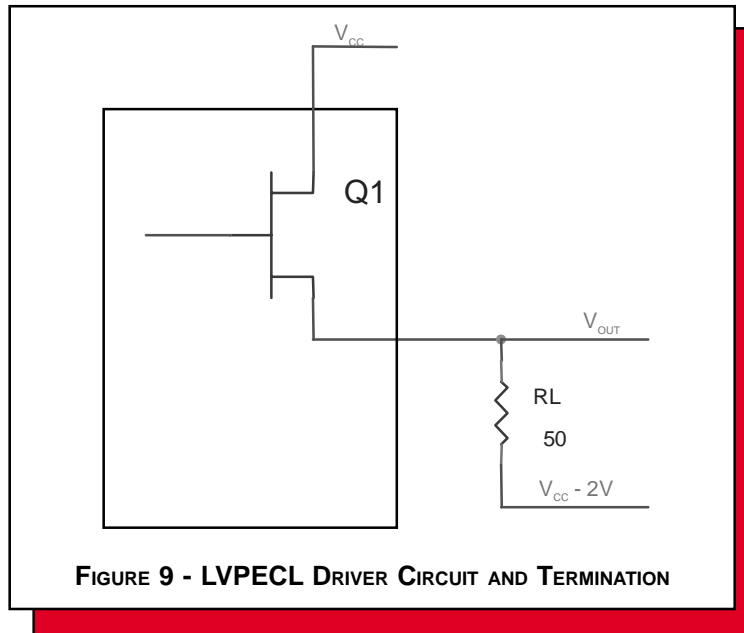
$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 9*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC} - 2V))/R_L] * (V_{CC} - V_{OH\_MAX})$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC} - 2V))/R_L] * (V_{CC} - V_{OL\_MAX})$$

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC} - 1.0V$   
Using  $V_{CC} = 3.465$ , this results in  $V_{OH\_MAX} = 2.465V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC} - 1.7V$   
Using  $V_{CC} = 3.465$ , this results in  $V_{OL\_MAX} = 1.765V$

$$Pd\_H = [(2.465V - (3.465V - 2V))/50 \Omega] * (3.465V - 2.465V) = 20.0mW$$

$$Pd\_L = [(1.765V - (3.465V - 2V))/50 \Omega] * (3.465V - 1.765V) = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30.2mW$$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS85304-01 is: 489



PACKAGE OUTLINE - G SUFFIX

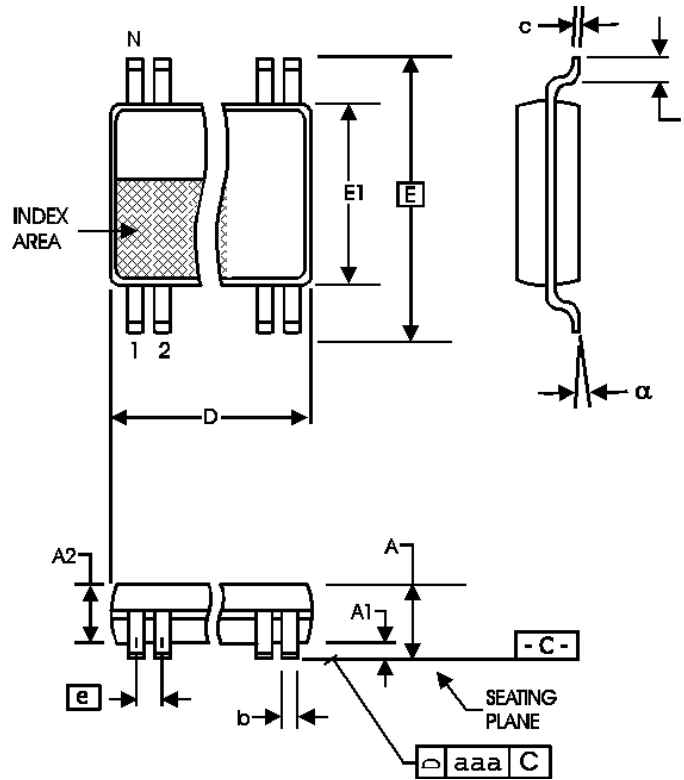


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated  
Circuit  
Systems, Inc.

**ICS85304-01**

LOW SKEW, 1-TO-5

DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Count</b>	<b>Temperature</b>
ICS85304AG-01	ICS85304AG-01	20 lead TSSOP	72 per tube	0°C to 70°C
ICS85304AG-01T	ICS85304AG-01	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C

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