PRELIMINARY

Integrated Circuit Systems, Inc.

ICS853052

DUAL LVCMOS / LVTTL-TO-DIFFERENTIAL 2.5V, 3.3V, 5V LVPECL MULTIPLEXER

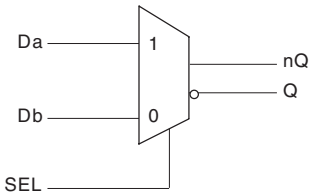
GENERAL DESCRIPTION

The ICS853052 is a Dual LVCMOS / LVTTL-to-Differential 2.5V, 3.3V, 5V LVPECL Multiplexer and a member of the HiPerClocks™family of High Performance Clocks Solutions from ICS. The ICS853052 has two selectable single ended clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to 2.5V, 3.3V or 5V LVPECL levels. The small outline 8-pin TSSOP or 8-pin SOIC packages make this device ideal for applications where space, high performance and low power are important.

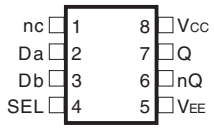
FEATURES

- 1 differential 2.5V, 3.3V or 5V LVPECL output
- 2 selectable LVCMOS/LVTTL clock inputs
- Output frequency: TBD
- Additive phase jitter, RMS: 0.06ps (typical)
- Propagation Delay: 370ps (typical)
- 2.5V, 3.3V or 5V operating supply voltage (operating range 2.375V to 5.5V)
- -40°C to 85°C ambient operating temperature
- Pin compatible with MC100EP58

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS853052
8-Lead TSSOP, 118 mil
3mm x 3mm x 0.95mm package body
G Package
Top View

8-Lead SOIC, 150 mil
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	nc	Unused		No connect.
2, 3	Da, Db	Input	Pulldown	LVCMOS / LVTTL clock inputs.
4	SEL	Input	Pulldown	Select input pin. When HIGH, selects Da input clock. When Low selects Db input clock. Single-ended 100H LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			1		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs	
SEL	**Selected Source**
0	Db
1	Da

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	101.7°C/W (0 m/s) TSSOP 112.7°C/W (0 lfpm) SOIC

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21			21			21		mA
V_{OH}	Output High Voltage; NOTE 1	1.375	1.475	1.58	1.425	1.495	1.57	1.495	1.53	1.565	V
V_{OL}	Output Low Voltage; NOTE 1	0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage, Single-Ended	1.275		1.56	1.275		1.56	1.275		-0.83	V
V_{IL}	Input Low Voltage, Single-Ended	0.63		0.965	0.63		0.965	0.63		0.965	V
I_{IH}	Input High Current			150			150			150	µA
I_{IL}	Input Low Current	150			150			150			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4B. DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21			21			21		mA
V_{OH}	Output High Voltage; NOTE 1	2175	2275	2380	2225	2295	2370	2295	2330	2365	mV
V_{OL}	Output Low Voltage; NOTE 1	1405	1545	1680	1425	1520	1615	1440	1535	1630	mV
V_{IH}	Input High Voltage), (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input Low Voltage, (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
I_{IH}	Input High Current			150			150			150	µA
I_{IL}	Input Low Current	150			150			150			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4C. DC CHARACTERISTICS, V_{CC} = 5V; V_{EE} = 0V

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21			21			21		mA
V_{OH}	Output High Voltage; NOTE 1	3875	3975	4105	4080	3925	3995	4070	3995	4065	mV
V_{OL}	Output Low Voltage; NOTE 1	3105	3245	3380	3125	3220	3315	3140	3235	3330	mV
V_{IH}	Input High Voltage, Single-Ended	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input Low Voltage, Single-Ended	3055		3375	3055		3375	3055		3375	mV
I_{IH}	Input High Current			150			150			150	µA
I_{IL}	Input Low Current	150			150			150			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -2.375V

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21			21			21		mA
V_{OH}	Output High Voltage; NOTE 1	-1125	-1025	-920	-1075	-1005	-930	-1005	-970	-935	mV
V_{OL}	Output Low Voltage; NOTE 1	-1895	-1755	-1620	-1875	-1780	-1685	-1860	-1765	-1670	mV
V_{IH}	Input High Voltage, Single-Ended	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input Low Voltage, Single-Ended	-1945		-1625	-1945		-1625	-1945		-1625	mV
I_{IH}	Input High Current			150			150			150	µA
I_{IL}	Input Low Current	150			150			150			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

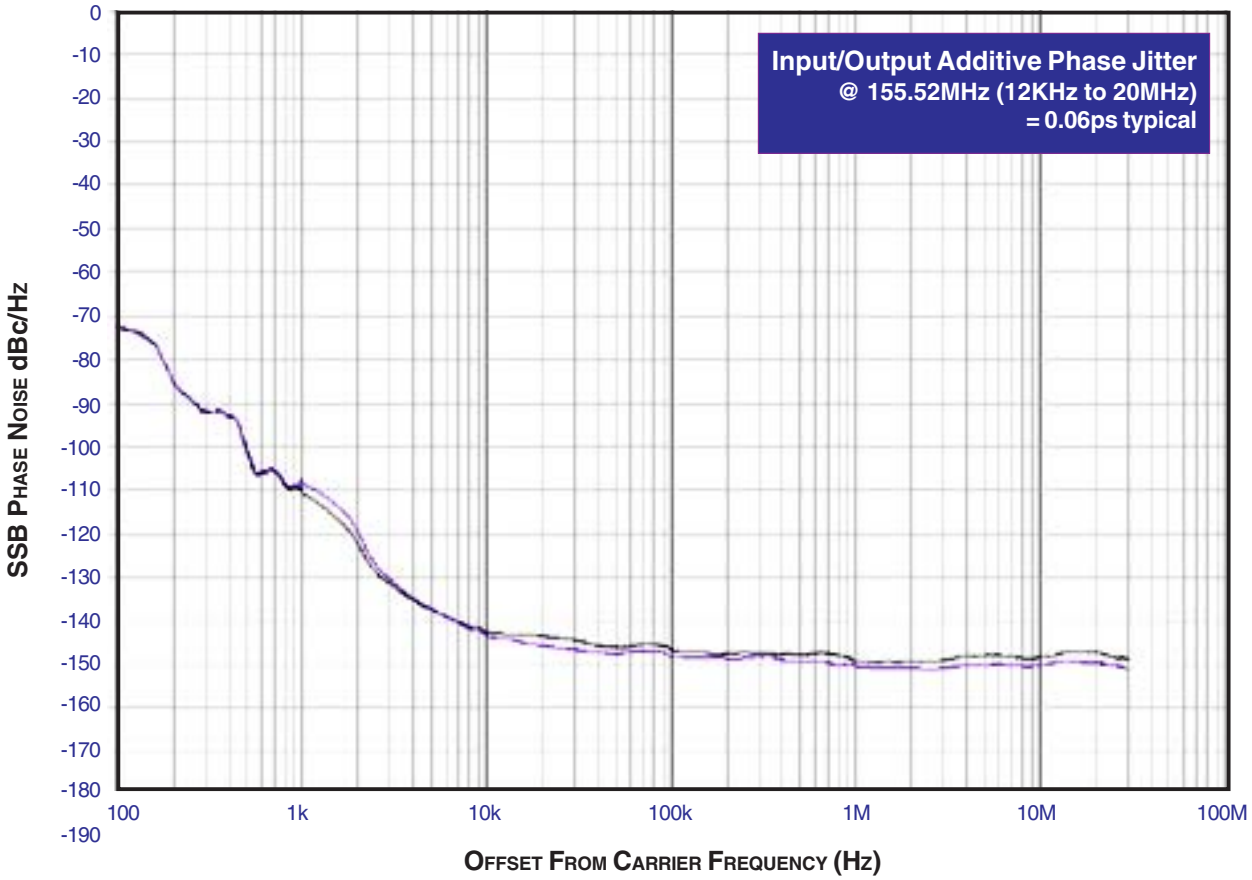
TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -2.375V OR V_{CC} = 2.375V TO 5.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay, Low to High; NOTE 1			TBD			370			TBD		ps
t_{PHL}	Propagation Delay, High to Low; NOTE 1			TBD			370			TBD		ps
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			TBD			0.06			TBD		ps
V_{PP}	Input Voltage Swing (Differential)			TBD			TBD			TBD		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		TBD			180			TBD		ps

All parameters are measured ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from V_{CC}/2 of the input crossing point to the differential output crossing point.

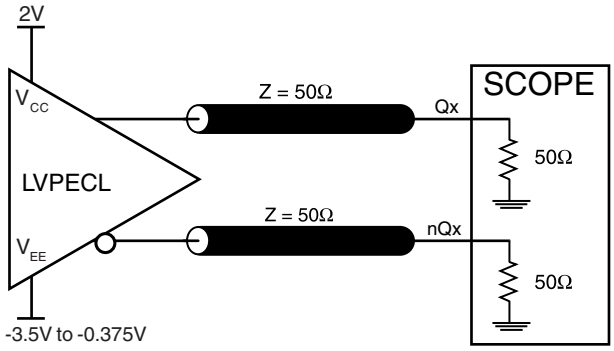
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

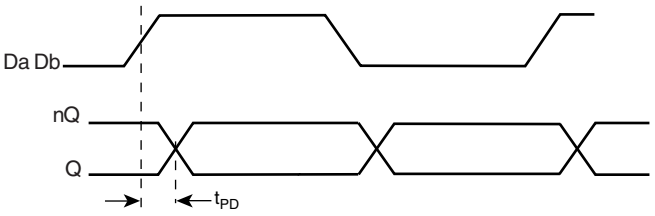


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

PARAMETER MEASUREMENT INFORMATION



OUTPUT LOAD AC TEST CIRCUIT



PROPAGATION DELAY

OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 1A and *Figure 1B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 1B can be eliminated and the termination is shown in *Figure 1C*.

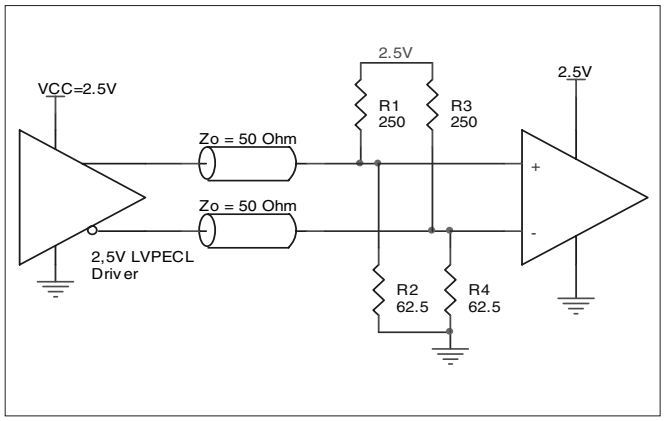


FIGURE 1A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

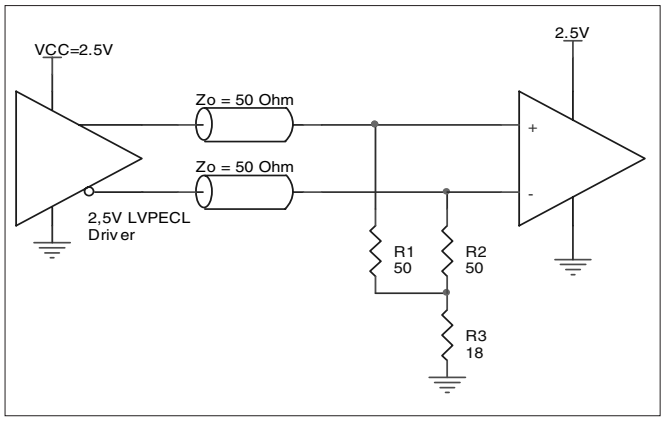


FIGURE 1B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

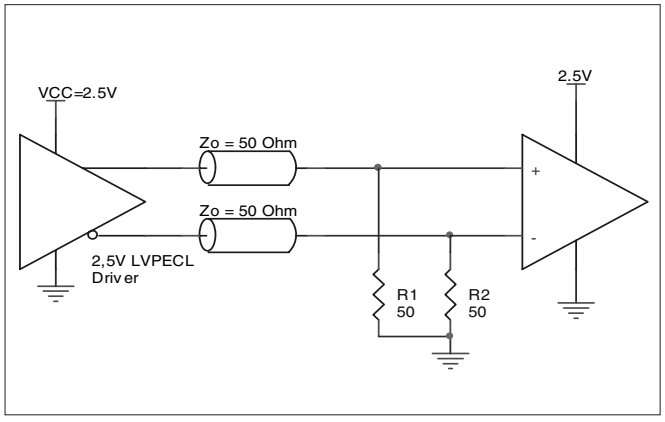


FIGURE 1C. 2.5V LVPECL TERMINATION EXAMPLE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

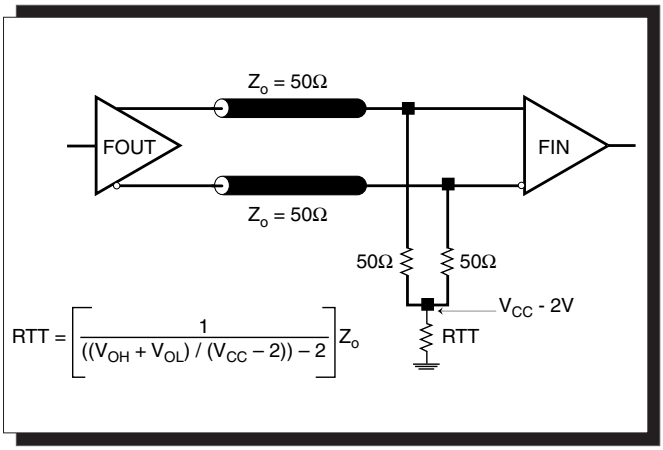


FIGURE 2A. LVPECL OUTPUT TERMINATION

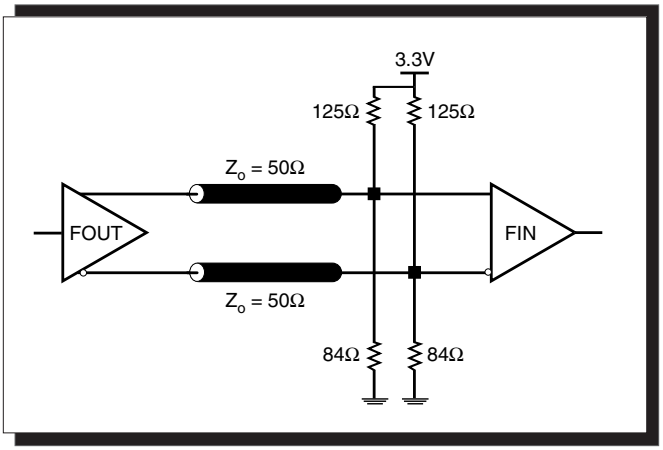


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 5V LVPECL OUTPUT

This section shows examples of 5V LVPECL output termination. *Figure 3A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to V_{CC} - 2V = 3V at the receiver. *Figure 3B* shows Thevenin equivalence of Figure 3A. In actual application where the 3V DC power supply is not available, this approached is normally used.

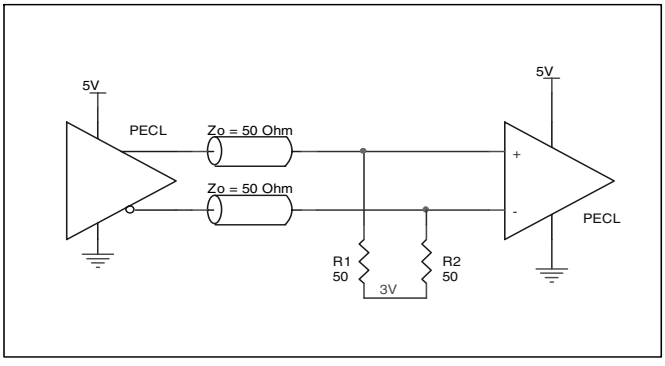


FIGURE 3A. STANDARD 5V PECL OUTPUT TERMINATION

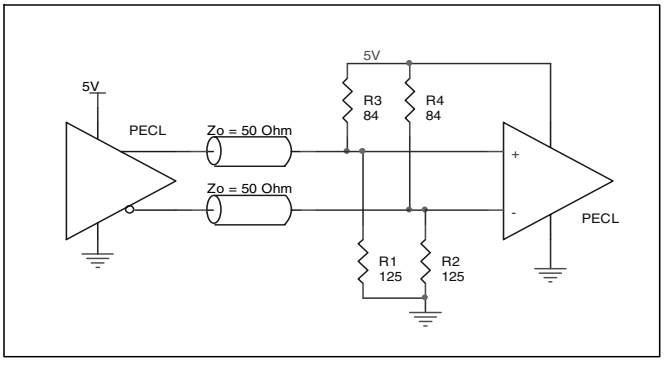


FIGURE 3B. 5V PECL OUTPUT TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853052. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853052 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 5.5V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 5.5V * 21mA = **115.5mW**
- Power (outputs)$_{MAX}$ = **30.94mW/Loaded Output pair**

Total Power$_{_MAX}$ (5.5V, with all outputs switching) = 115.5mW + 30.94mW = **146.4mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.146W * 90.5°C/W = 98.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 4.

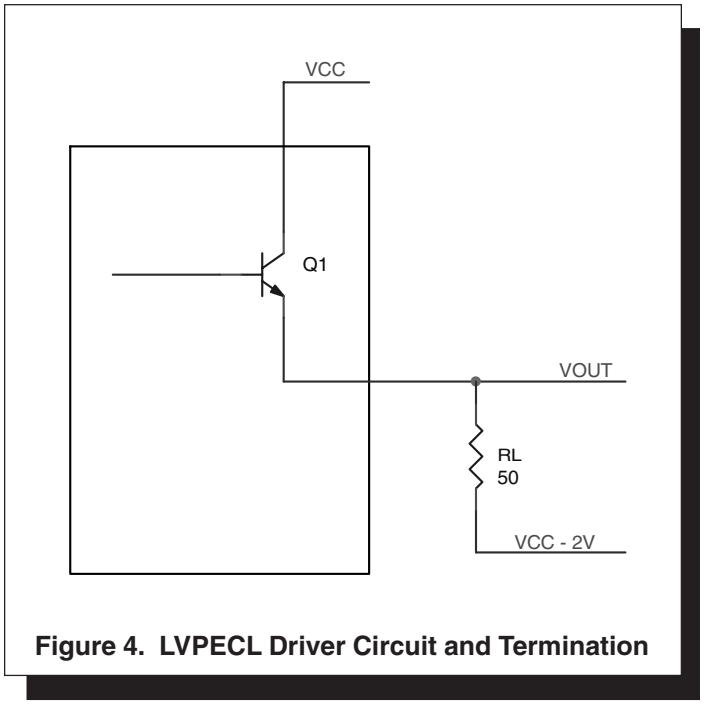


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} – 1.67V$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50Ω] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50Ω] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

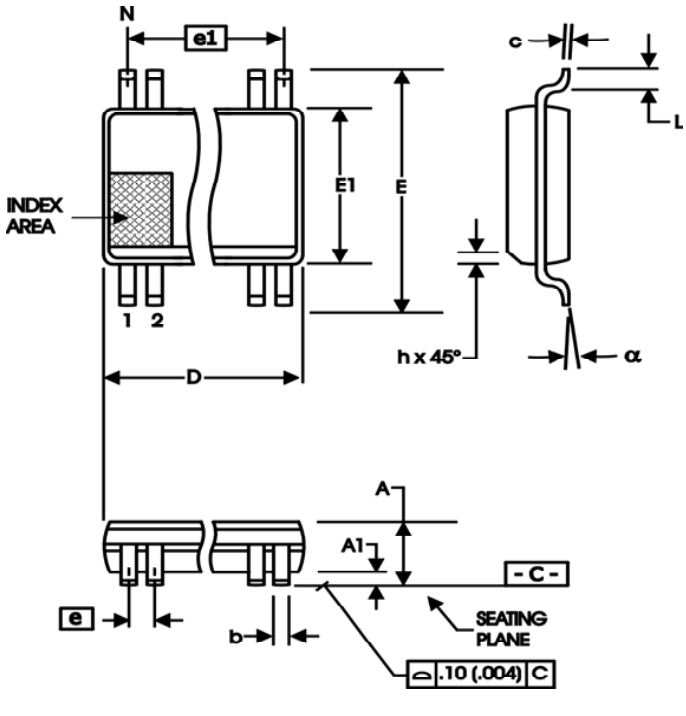
θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853052 is: 110

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

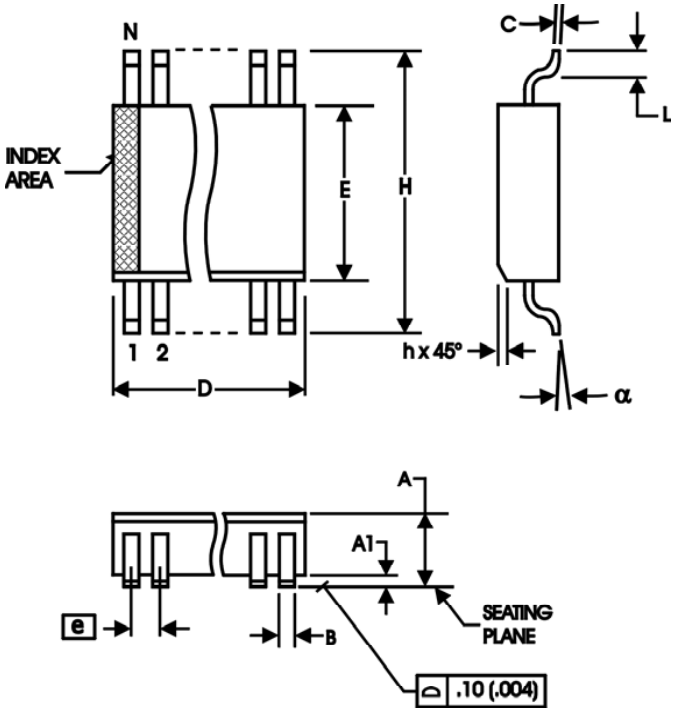


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS853052AG	052A	8 lead TSSOP	96 per tube	-40°C to 85°C
ICS853052AGT	052A	8 lead TSSOP on Tape and Reel	2500	-40°C to 85°C
ICS853052AM	853052A	8 lead SOIC	96 per tube	-40°C to 85°C
ICS853052AMT	853052A	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C