Integrated Circuit Systems, Inc.

ICS85311
Low Skew, 1-to-2 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer

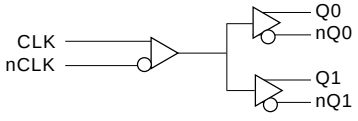
General Description

The ICS85311 is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels.The ICS85311 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85311 ideal for those clock distribution applications demanding well defined performance and repeatability.

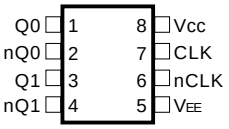
Features

- 2 differential 2.5V/3.3V LVPECL / ECL outputs
- 1 CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 1GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 15ps (maximum)
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 1.4ns (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -2.375V to -3.465V
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

Block Diagram



Pin Assignment



ICS85311

8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin. Connect to ground.
6	nCLK	Input	Pullup	Inverting differential clock input.
7	CLK	Input	Pulldown	Non-inverting differential clock input.
8	V_{CC}	Power		Positive supply pin. Connect to 2.5v or 3.3V.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK, nCLK				4	pF
R_{PULLUP}	Input Pullup Resistor				51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		KΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	112°C/W
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				25	mA

Table 3B. Differential DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltag for CLK, nCLK is V_{CC} + 0.3V.

Table 3C. Power Supply DC Characteristics, V_{CC} = 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				25	mA

TABLE 3D. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 2.625V			150	µA
		nCLK	$V_{CC} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 2.625V, V_{IN} = 0V	-5			µA
		nCLK	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltag for CLK, nCLK is V_{CC} + 0.3V.

TABLE 3E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.65		0.9	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4F. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				1	GHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 1GHz	0.9		1.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				15	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				100	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48		52	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

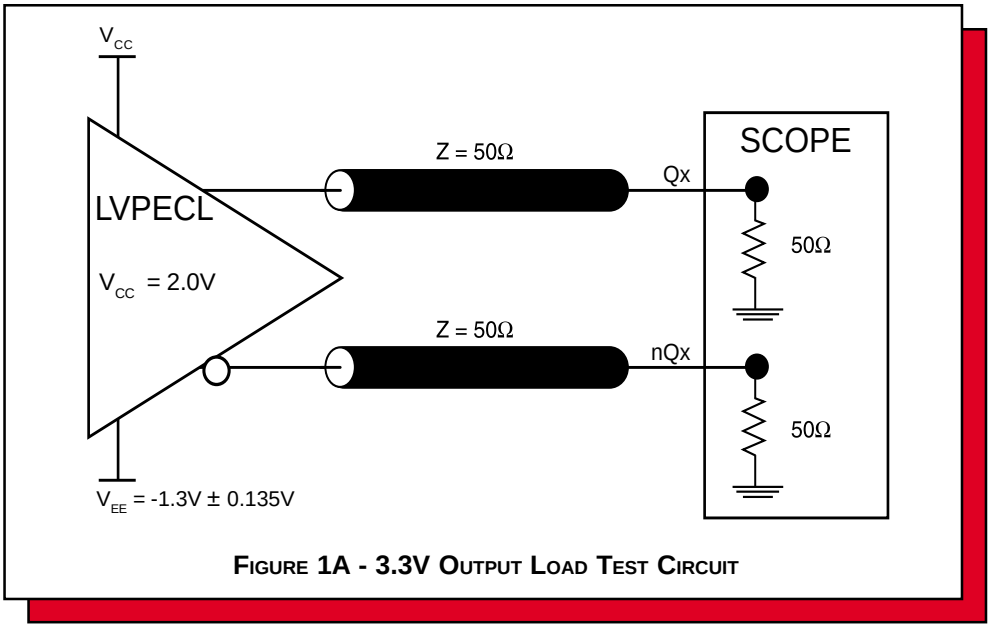


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

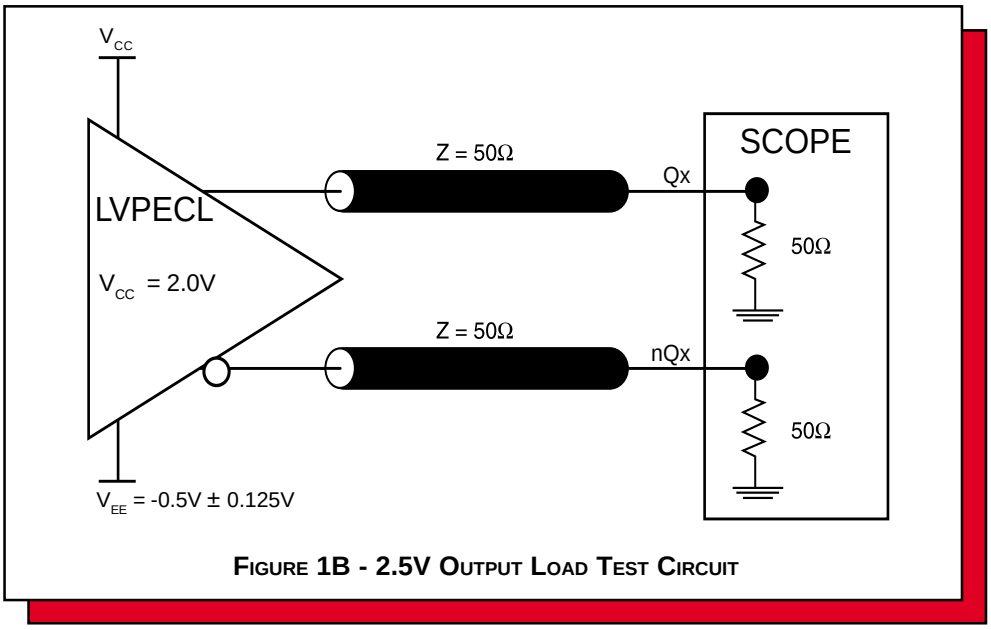


FIGURE 1B - 2.5V OUTPUT LOAD TEST CIRCUIT

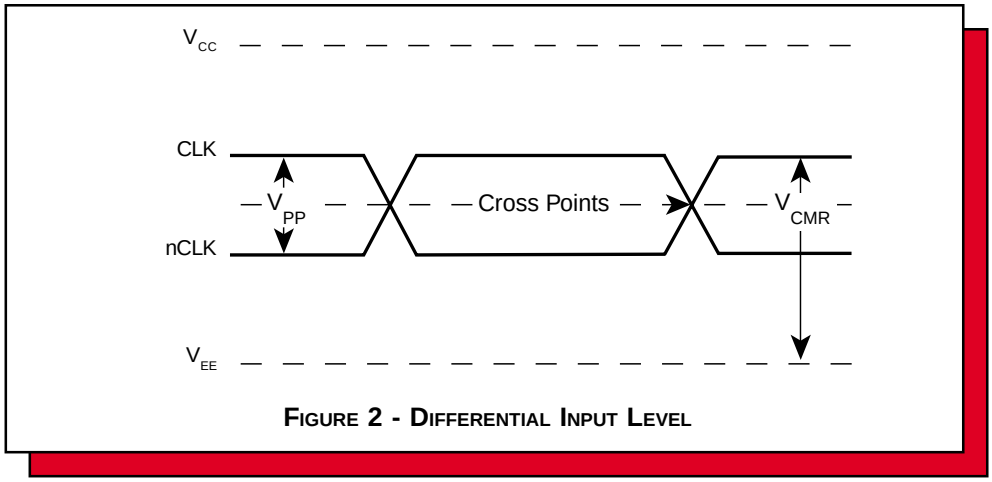


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

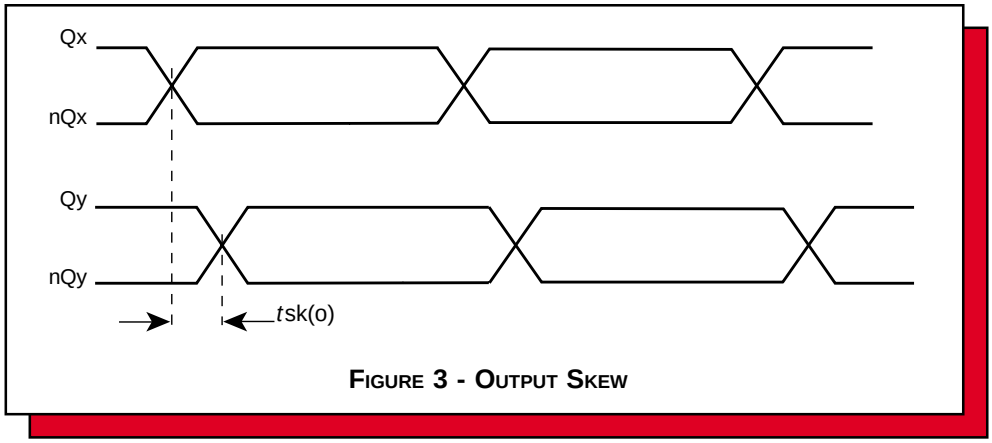


FIGURE 3 - OUTPUT SKEW

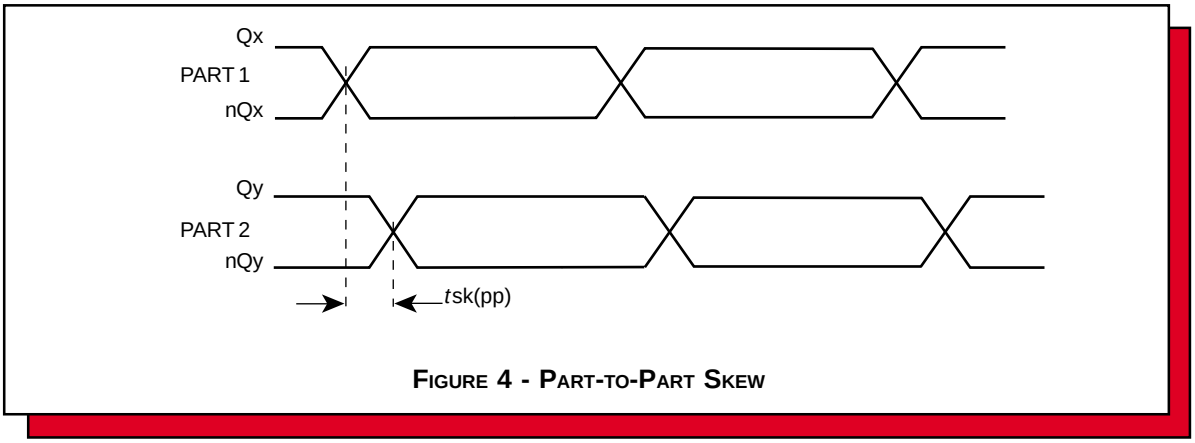


FIGURE 4 - PART-TO-PART SKEW

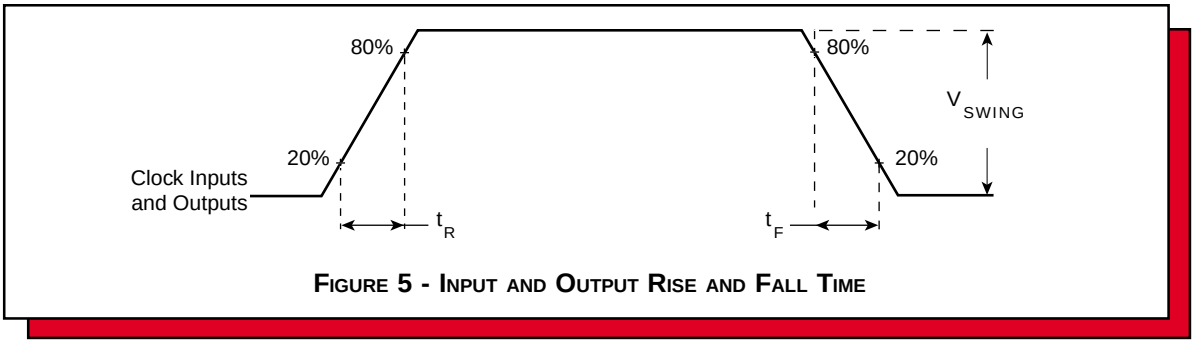


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

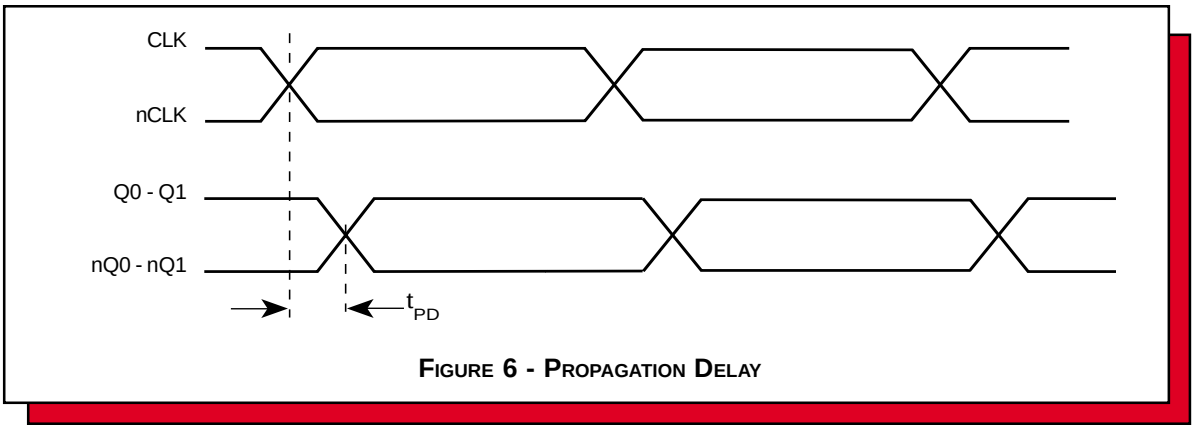


FIGURE 6 - PROPAGATION DELAY

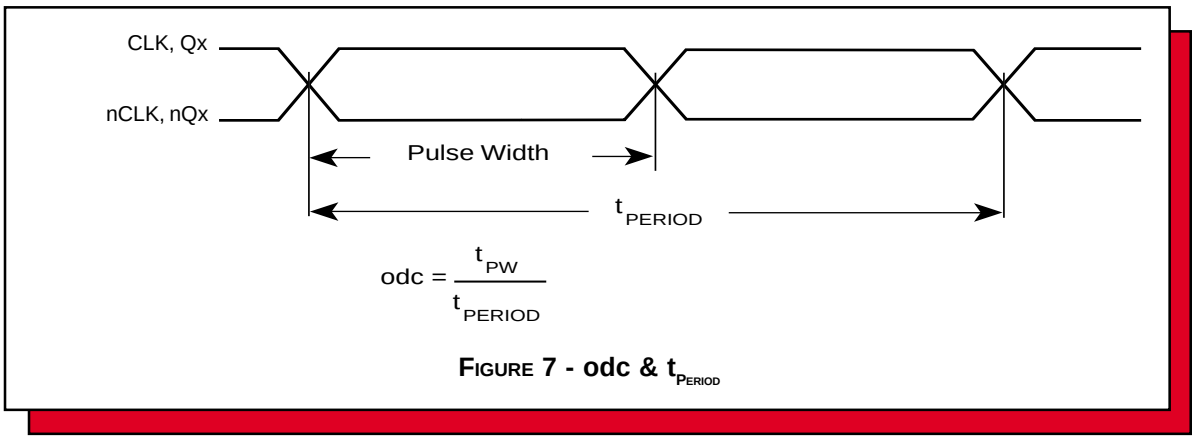


FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

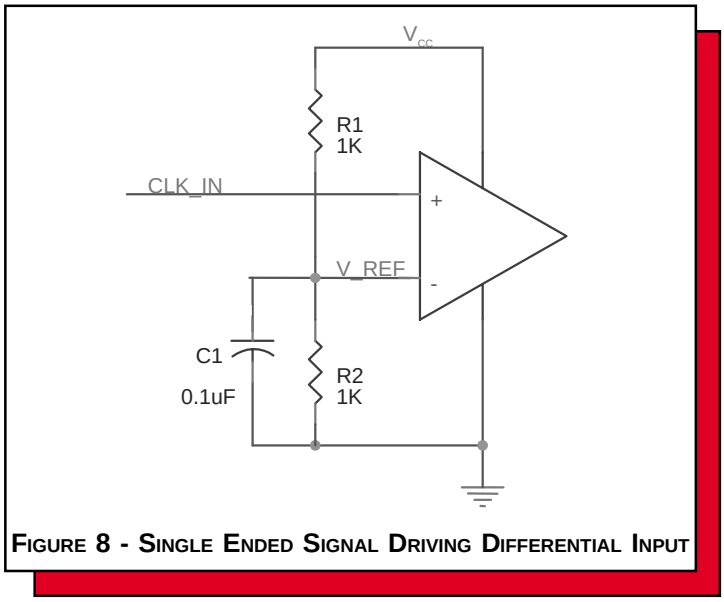


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85311. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation of the ICS85311 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core) = V_{CC} * I_{EE} = 3.465V * 25mA = **86.6mW**
- Power (outputs) = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 x 30.2mW = **60.4mW**

Total Power (3.465V, with all outputs switching) = 86.6mW + 60.4mW = **147mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

In order to determine if the junction temperature is below 125°C, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used in conjunction with the total power dissipation. Assuming a moderate air low of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per the table below:

$Tj = \theta_{JA}$ * Pd_total + T_A where Pd_total is the total power dissipation of the device and T_A is the ambient temperature. Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.147W * 103.3°C/W = 85.2°C. This is well below the limit of 125°C.

This calculation is only an example, and the Tj will obviously vary depending on the number of outputs that are loaded, supply voltage, air flow, and the type of board (single layer or multi-layer).

Thermal Resistance θ_{JA} for 8-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 9.

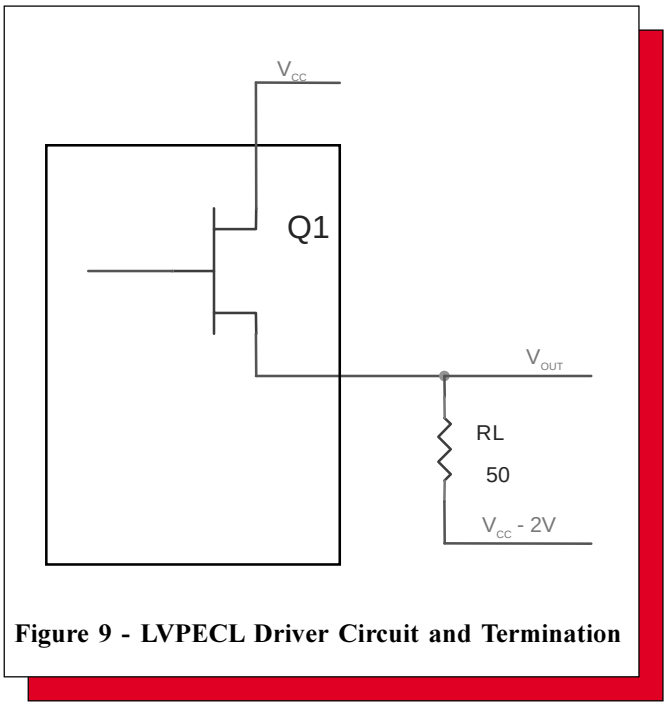


Figure 9 - LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC} - 2V))/R_L]*(V_{CC} - V_{OH\_MAX})$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC} - 2V))/R_L]*(V_{CC} - V_{OL\_MAX})$

- For logic high , $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC} – 1.0V}$
  Using V_{CC} = 3.465, this results in V_{OH_MAX} = **2.465V**
- For logic low , $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC} – 1.7V}$
  Using V_{CC} = 3.465, this results in V_{OL_MAX} = **1.765V**

Pd_H = [(2.465V - (3.465V - 2V))/50 Ω]*(3.465V - 2.465V) = **20.0mW**
Pd_L = [(1.765V - (3.465V - 2V))/50 Ω]*(3.465V - 1.765V) = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85311 is: 225

PACKAGE OUTLINE - M SUFFIX

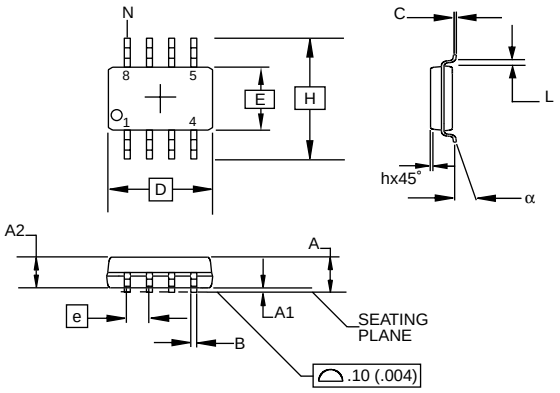


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MINIMUN	MAXIMUM	MINIMUN	MAXIMUM
N	8			
A	1.35	1.75	0.532	0.0688
A1	0.10	0.25	0.0040	0.0098
A2	1.25	1.50	0.0492	0.0590
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	0.1890	0.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85311AM	ICS85311AM	8 lead SOIC	96 per tube	0°C to 70°C
ICS85311AMT	ICS85311AM	8 lead SOIC on Tape and Reel	2500	0°C to 70°C