Low Skew, 1-to-6, Crystal/ LVCMOS/ Differential-to-3.3V, 2.5V LVPECL Fanout Buffer

ICS8536-01

DATA SHEET

GENERAL DESCRIPTION

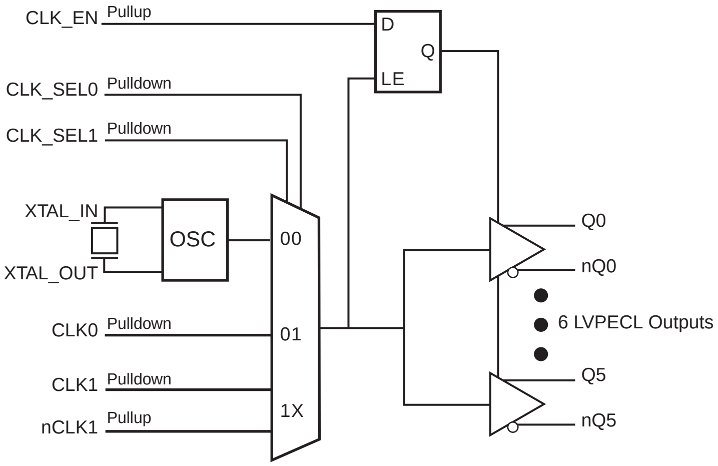
The ICS8536-01 is a low skew, high performance 1-to-6 Selectable Crystal, Single-Ended, or Differential Input-to-3.3V, 2.5V LVPECL Fanout Buffer. The ICS8536-01 has selectable crystal, single ended or differential clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to LVPECL levels. The CLK1, nCLK1 pair can accept most standard differential input levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8536-01 ideal for those applications demanding well defined performance and repeatability.

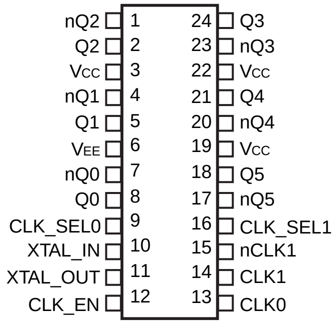
FEATURES

- Six 3.3V, 2.5V LVPECL outputs
- Selectable crystal oscillator, differential CLK1, nCLK1 pair or LVCMOS/LVTTL clock input
- CLK1, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Crystal frequency range: 12MHz - 40MHz
- Output skew: 55ps (maximum) CLK1, nCLK1 @ 3.3V
- Part-to-part skew: 450ps (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- Full 3.3V or 2.5V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8536-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVPECL interface levels
3, 19, 22	V_{CC}	Power		Power supply pins
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels
6	V_{EE}	Power		Negative supply pin
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3A.
13	CLK	Input	Pulldown	LVCMOS/LVTTL clock input
14	CLK	Input	Pulldown	Non-inverting differential clock input
15	nCLK	Input	Pullup	Inverting differential clock input
17, 18	nQ5, Q5	Output		Differential output pair. LVPECL interface levels
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface levels
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pulup Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q0:Q5**	**nQ0:nQ5**
0	0	0	XTAL	Disabled	Disabled
0	0	1	CLK0	Disabled	Disabled
0	1	X	CLK1, nCLK1	Disabled	Disabled
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1, nCLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in *Figure 1.*

In the active mode, the state of the outputs are a function of the selected clock input as described in Table 3B.

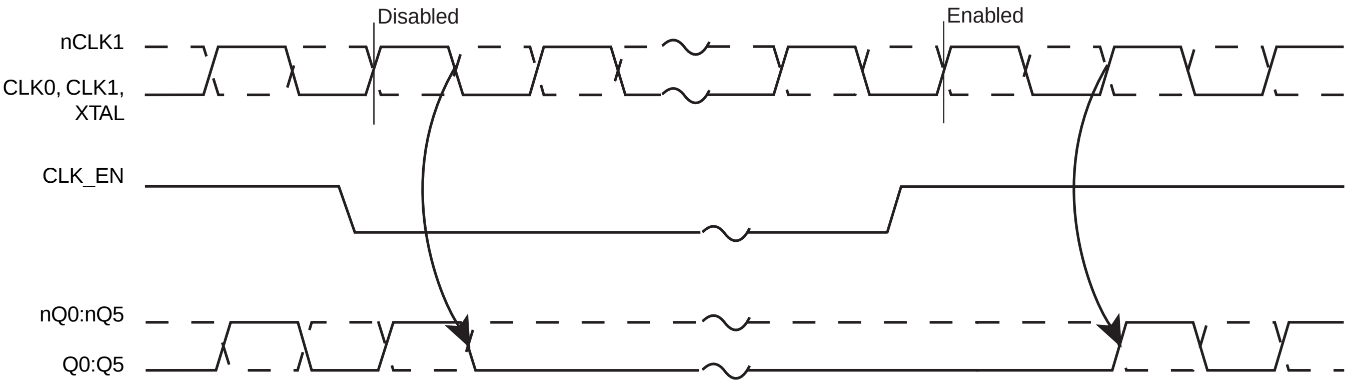


FIGURE 1. CLK_EN TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	84.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Paramete	Test Condition	MInimu	Typica	Maximu	Unit
V_{CC}	Power Supply Voltage		33135	35	3V46	
I_{EE}	Power Supply Current				85A	m

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximu	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				85	mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} =23.3V			V_{CC} + 0.3	V
			V_{CC} =72.5V	1.V		$_{CC}$ +V0.3	
V_{IL}	Input Low Voltage		V_{CC} =33.3V	-0.		0.V	
			V_{CC} =32.5V	-0.		0.V	
I_{IH}	Input High Current	CLK0, CLK_SEL0:1	V_{CC} = V_{IN} =03.465V or 2.625V			15A	µ
		CLVK_EN	$_{CC}$ = V_{IN} =53.465V or 2.625V				µA
I_{IL}	Input Low Current	CLK0, CLK_SEL0:1	V_{CC} = 3.465V or 2.625V, V_{IN} =50V	-A			µ
		CLVK_EN	$_{CC}$ = 3.465V or 2.625V, V_{IN} =00V	-A15			µ

TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
		CLK1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nVCLK1	$_{CC}$ = 3.465V or 2.625V, V_{IN} = 00V	-1A5			µ
		CLVK1	$_{CC}$ = 3.465V or 2.625V, V_{IN} = 50V	-A			µ
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0315		1.V	
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} +V0.5		$_{CC}$ -V0.85	

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		4z	MH
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7F	p
Drive Level				1W	m

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	CLK1/nCLK1				700	MHz
		CLK0				300	MHz
t_{PD}	Propagation Delay, NOTE1A, 1B	CLK1/nCLK1		1.7		2.5	ns
		CLK0		1.35		2.0	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2		CLK1/nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
*t*sk(o)	Output Skew; NOTE 3, 5					55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5					450	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1/nCLK1		48		52	%
		CLK0		44		56	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 6A	*f* = 150MHz		-76		dB
		NOTE 6B	*f* = 250MHz		-75		dB

All parameters measured at $f_{OUT} \leq 300$MHz unless noted otherwise.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter

NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.

NOTE 1B: Measured from $V_{CC}/2$ input crossing point to the differential output crossing point.

NOTE 2: Driving only one input clock.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6A: CLK0 (150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.

NOTE 6B: CLK0 (250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

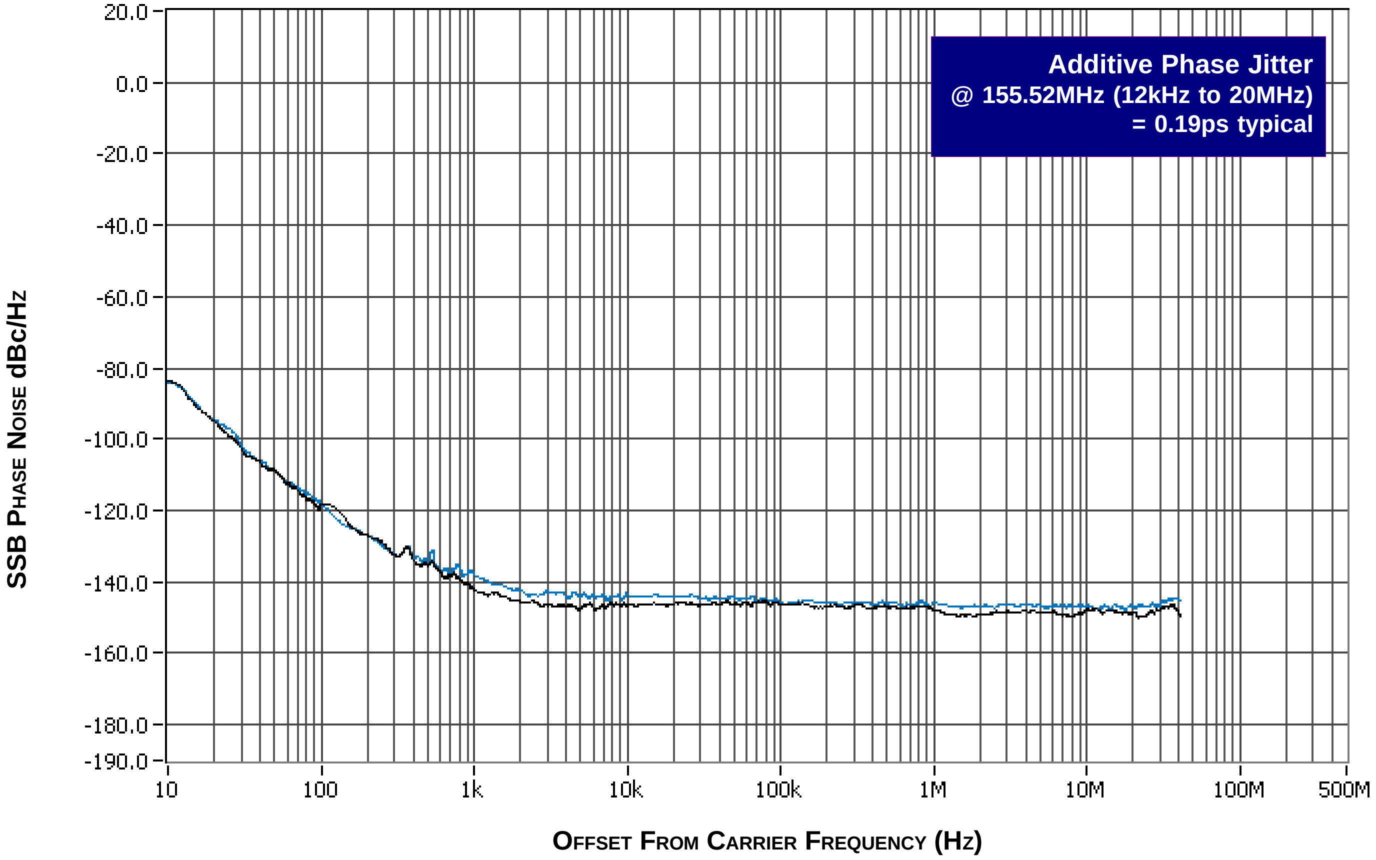
TABLE 6B. AC CHARACTERISTICS, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	CLK1, nCLK1				700	MHz
		CLK0				300	MHz
t_{PD}	Propagation Delay, NOTE1A, 1B	CLK1, nCLK1		1.7		2.65	ns
		CLK0		1.4		2.05	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2		CLK1, nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
*t*sk(o)	Output Skew; NOTE 3, 5					55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5					450	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1, nCLK1		48		52	%
		CLK0		46		54	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 6A	*f* = 150MHz		-76		dB
		NOTE 6B	*f* = 250MHz		-75		dB

For notes, see Table 6A above.

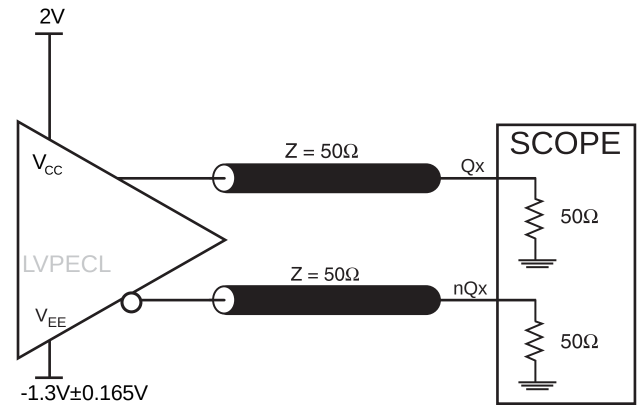
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

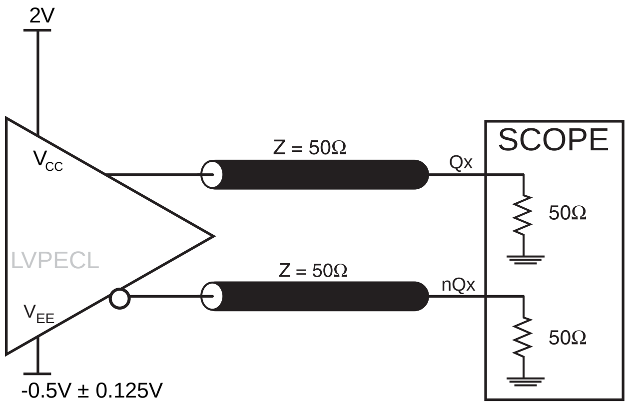


As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

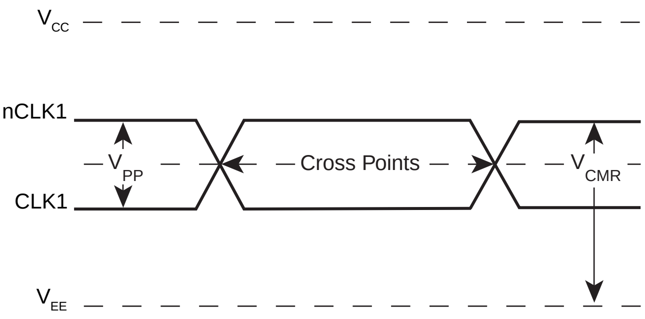
PARAMETER MEASUREMENT INFORMATION



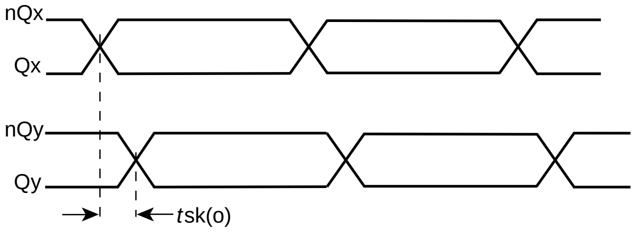
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



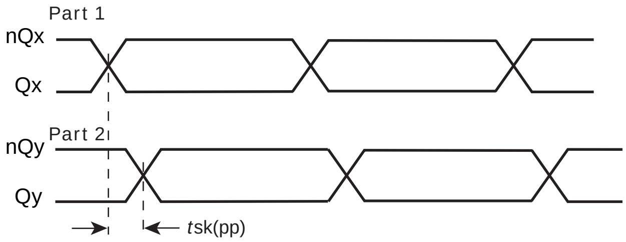
2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



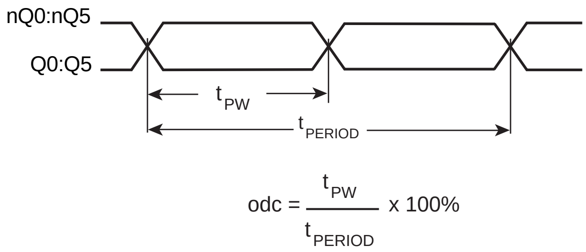
DIFFERENTIAL INPUT LEVELS



OUTPUT SKEW

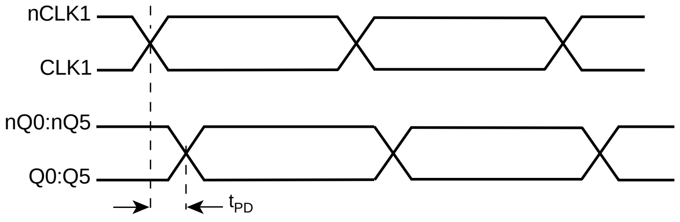


PART-TO-PART SKEW

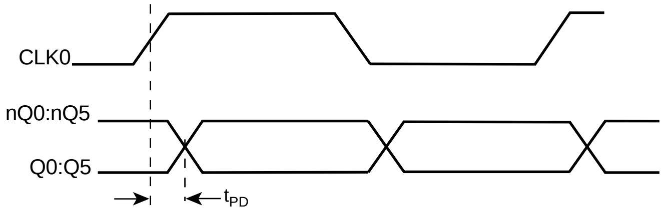


$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

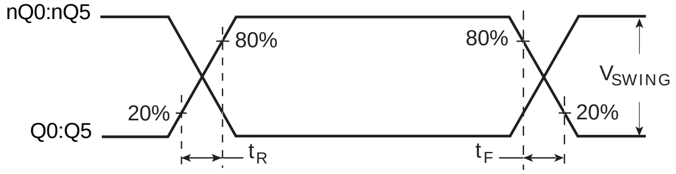
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY (DIFFERENTIAL INPUT)



PROPAGATION DELAY (LVCMOS INPUT)



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{cc}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{cc} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single-ended swing and V_{cc} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50 applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{cc} + 0.3V . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

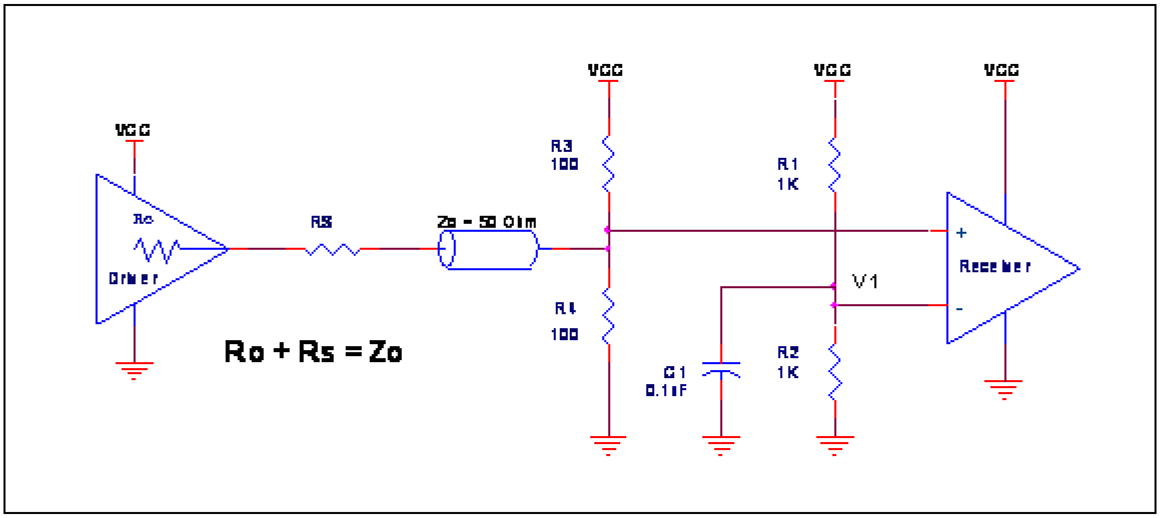


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

CRYSTAL INPUT INTERFACE

The ICS8536-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

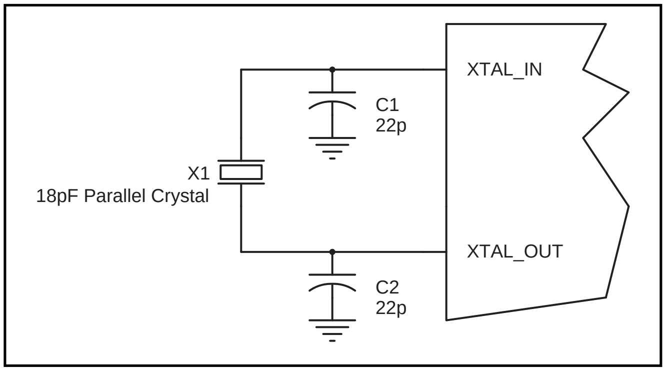


FIGURE 2. CRYSTAL INPUT INTERFACE

OVERDRIVING THE CRYSTAL INTERFACE

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. Figure 3 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

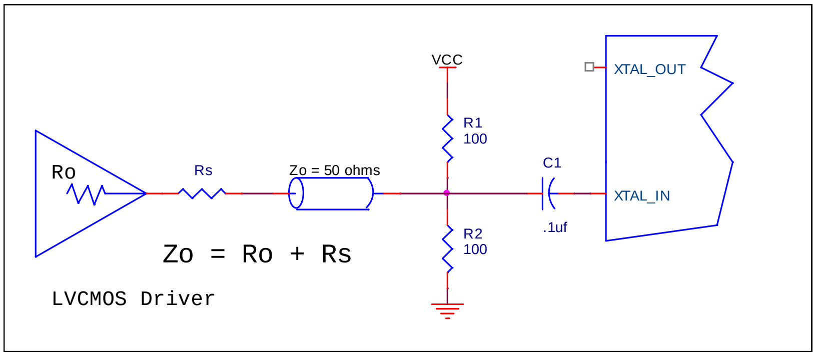


FIGURE 3A. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

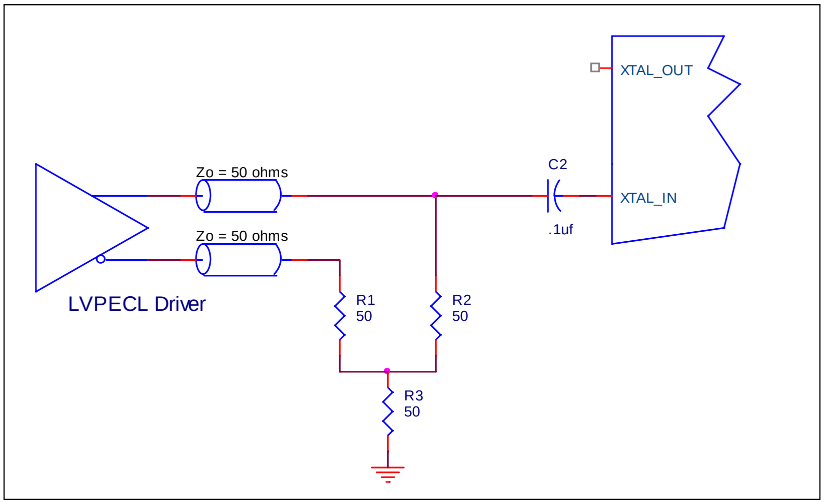


FIGURE 3B. GENERAL DIAGRAM FOR LVPECL DRIVER TO XTAL INPUT INTERFACE

Differential Clock Input Interface

The CLK, nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the CLK, nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

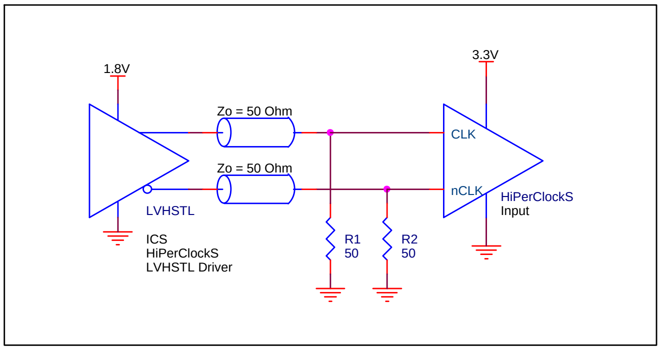


Figure 4A. CLK, nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

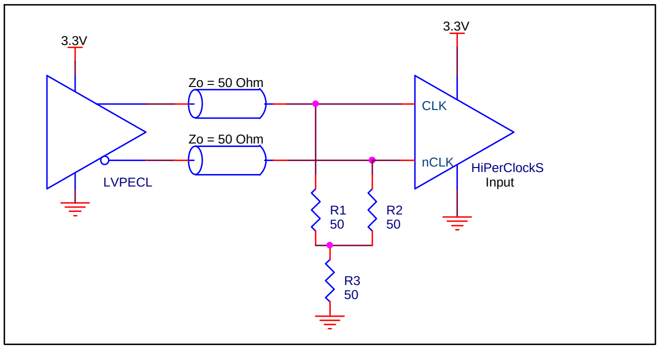


Figure 4B. CLK, nCLK Input Driven by a 3.3V LVPECL Driver

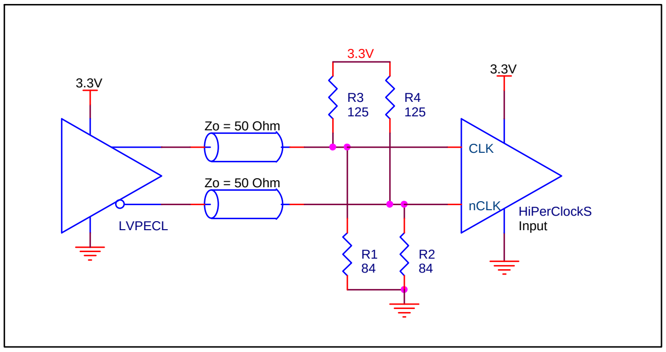


Figure 4C. CLK, nCLK Input Driven by a 3.3V LVPECL Driver

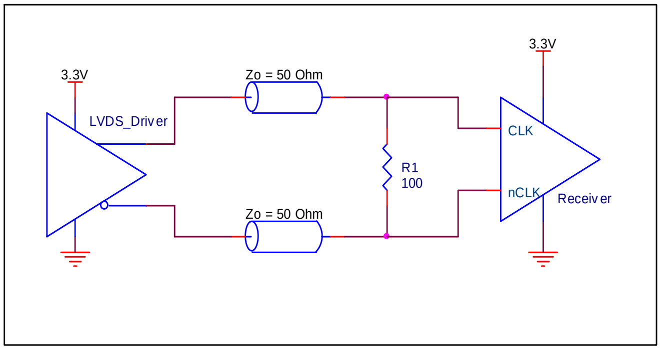


Figure 4D. CLK, nCLK Input Driven by a 3.3V LVDS Driver

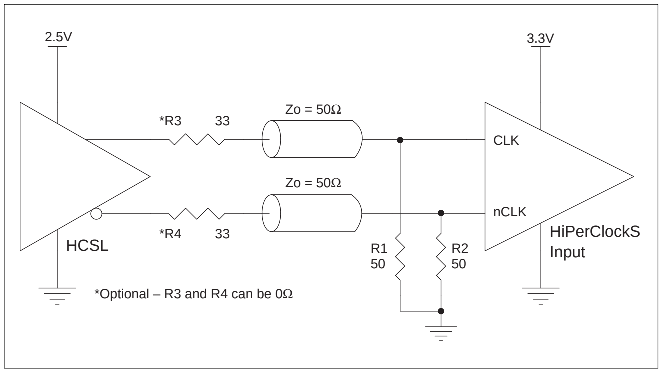


Figure 4E. CLK, nCLK Input Driven by a 3.3V HCSL Driver

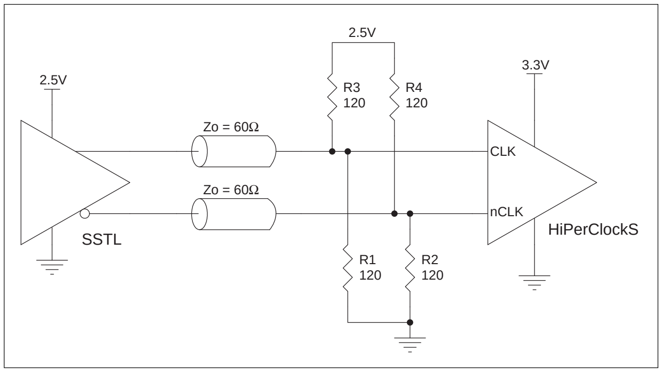


Figure 4F. CLK, nCLK Input Driven by a 2.5V SSTL Driver

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

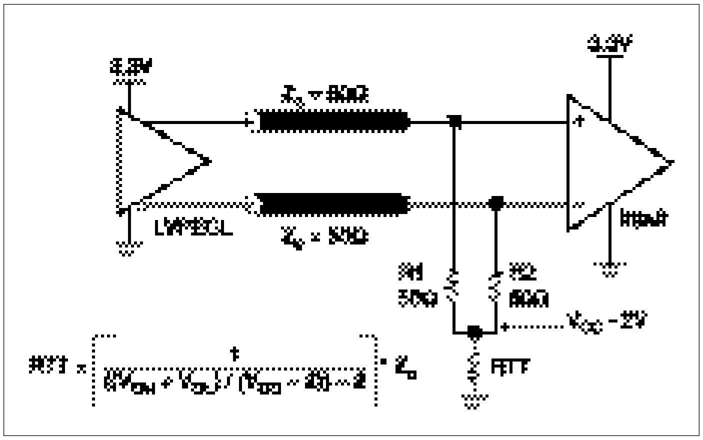


FIGURE 5A. LVPECL OUTPUT TERMINATION

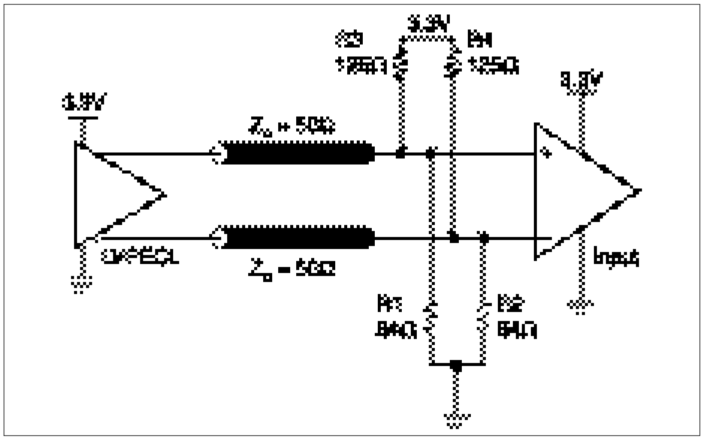


FIGURE 5B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

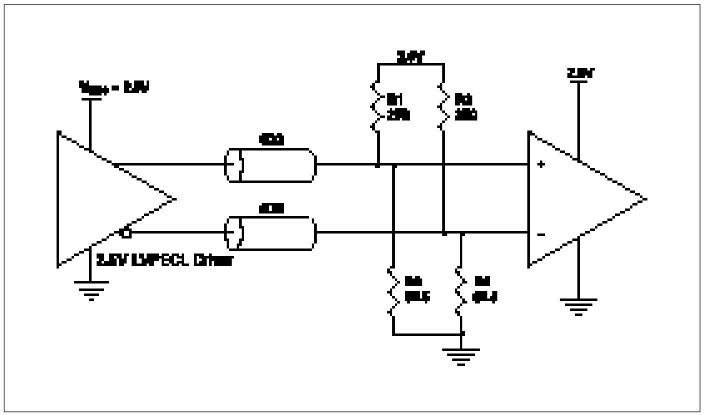


FIGURE 6A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

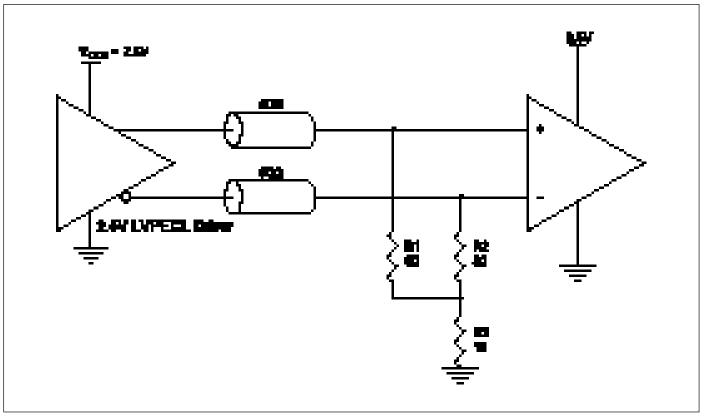


FIGURE 6B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

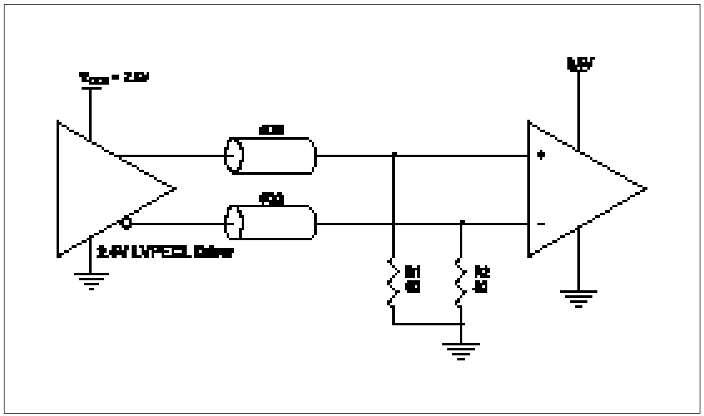


FIGURE 6C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8536-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8536-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 85mA = 294.525 **mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 294.525mW + 180mW **= 474.525mW**

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 84.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.475W * 84.6°C/W = 110.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	84.6°C/W	80.3°C/W	78.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

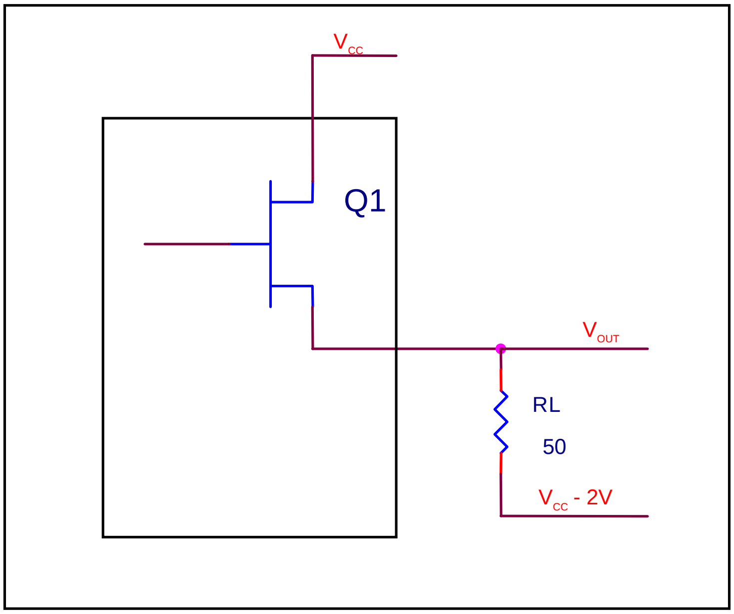


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate power dissipation due to the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX})$ = **0.9V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX})$ = **1.7V**

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX})$ =
[(2V - 0.9V)/50 Ω] * 0.9V = **19.8mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX})$ =
[(2V - 1.7V)/50 Ω] * 1.7V = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	84.6°C/W	80.3°C/W	78.1°C/W

TRANSISTOR COUNT

The transistor count for ICS8536-01 is: 513

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

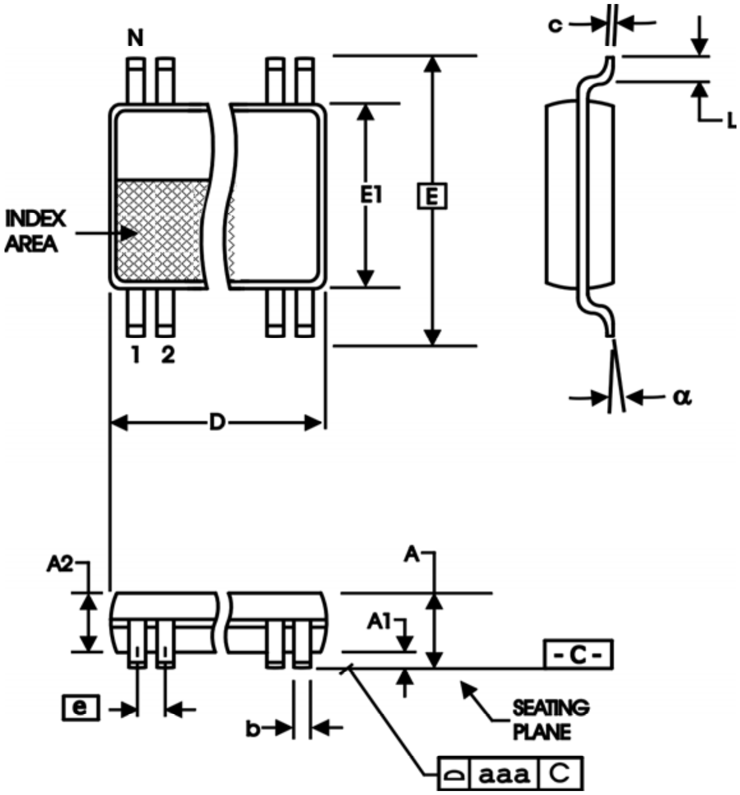


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximu
N4	2	
A-	-0	1.2
A15	050	0.1
A20	058	1.0
b9	001	0.3
c9	000	0.2
D0	707	7.9
EC	6.40 BASI	
E01	403	4.5
eC	0.65 BASI	
L5	054	0.7
α	0°	8
aaa	-0	0.1

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8536AG-01LF	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS8536AG-01LFT	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Changes	Date
B	 4A, 4B 6A 6B 10 	 1 4 6 6 15, 16 19 20	Removed HiPerClock references throughout. Updated diagrams to current standard throughout. Features List: Removed non lead-free package. Vcc: changed Core Supply Voltage to Power Supply Voltage. Per PCN #Table Note: changed f_{MAX} to $f_{OUT} \leq$ 300MHz. t_{PD} : 2.0ns (Max) to 2.6ns (Max). Updated text in Power Considerations section. Removed non lead-free ordering options and note. Removed quantity from T&R. Deleted disclaimer at bottom of page 19. Updated disclaimer on last page.	8/17/12

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