

### General Description

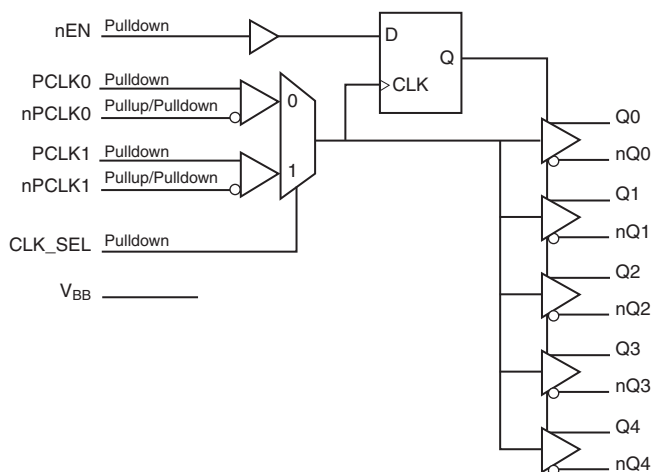
The ICS853S014I is a low skew, high performance 1-to-5, 2.5V/3.3V Differential-to-LVPECL/ECL Fanout Buffer. The ICS853S014I has two selectable clock inputs.

Guaranteed output and part-to-part skew characteristics make the ICS853S014I ideal for those applications demanding well defined performance and repeatability.

### Features

- Five differential LVPECL/ECL outputs
- Two selectable differential LVPECL clock inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2GHz
- Output skew: 55ps (maximum)
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 500ps (maximum)
- Additive phase jitter, RMS: 0.10ps (maximum)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $3.8V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -3.8V$  to  $-2.375V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Lead-free (RoHS 6) packaging

### Block Diagram



### Pin Assignment

Q0	1	20	V <sub>CC</sub>
nQ0	2	19	nEN
Q1	3	18	V <sub>CC</sub>
nQ1	4	17	nPCLK1
Q2	5	16	PCLK1
nQ2	6	15	V <sub>BB</sub>
Q3	7	14	nPCLK0
nQ3	8	13	PCLK0
Q4	9	12	CLK_SEL
nQ4	10	11	V <sub>EE</sub>

**ICS853S014I**

**20-Lead TSSOP**

**6.5mm x 4.4mm x 0.925mm package body**

**G Package**

**Top View**

## Pin Description and Pin Characteristic Table

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL/ECL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVPECL/ECL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVPECL/ECL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVPECL/ECL interface levels.
11	V <sub>EE</sub>	Power		Negative supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. Single-ended LVPECL interface levels.
13	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
14	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V <sub>CC</sub> /2 default when left floating.
15	V <sub>BB</sub>	Output		Bias voltage.
16	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V <sub>CC</sub> /2 default when left floating.
18, 20	V <sub>CC</sub>	Power		Positive supply pins.
19	nEN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Qx outputs are forced low, nQx outputs are forced high. Single-ended LVPECL interface levels.

NOTE: *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			37		kΩ
R <sub>VCC/2</sub>	Pullup/Pulldown Resistors			37		kΩ

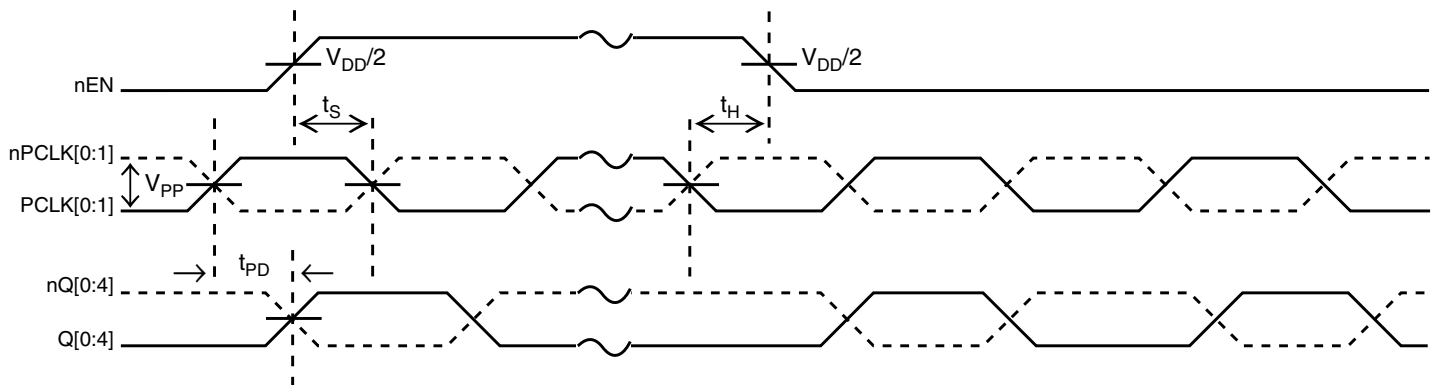
## Function Tables

**Table 3A. Control Input Function Table**

Inputs			Outputs	
nEN	CLK_SEL	Selected Source	Q0:Q4	nQ0:nQ4
1	0	PCLK0, nPCLK0	Disabled; Low	Disabled; High
1	1	PCLK1, nPCLK1	Disabled; Low	Disabled; High
0	0	PCLK0, nPCLK0	Enabled	Enabled
0	1	PCLK1, nPCLK1	Enabled	Enabled

After nEN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1*.

In the active mode, the state of the outputs are a function of the PCLK0, nPCLK0 and PCLK1, nPCLK1 inputs as described in Table 3B.


**Figure 1. nEN Timing Diagram**
**Table 3B. Clock Input Function Table**

Inputs		Outputs		Input to Output Mode	Polarity
PCLK0 or PCLK1	nPCLK0 or nPCLK1	Q0:Q4	nQ0:nQ4		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section. *Wiring the Differential Input to Accept Single-ended Levels.*

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V (LVPECL mode, $V_{EE} = 0V$ )
Negative Supply Voltage, $V_{EE}$	-4.6V (ECL mode, $V_{CC} = 0V$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
$V_{BB}$ Sink//Source, $I_{BB}$	$\pm 0.5mA$
Operating Temperature Range, $T_A$	-40°C to +85°C
Package Thermal Impedance, $\theta_{JA}$	92.1°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 2.375V$  to  $3.8V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	3.3	3.8	V
$I_{EE}$	Power Supply Current				68	mA

**Table 4B. DC Characteristics,  $V_{CC} = 3.3V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1		2.175	2.275	2.50	2.225	2.295	2.495	2.22	2.295	2.485	V
$V_{OL}$	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
$V_{IH}$	Input High Voltage (CLK_SEL, nEN)		2.075		2.36	2.075		2.36	2.075		2.36	V
$V_{IL}$	Input Low Voltage (CLK_SEL, nEN)		1.43		1.765	1.43		1.765	1.43		1.765	V
$V_{BB}$	Output Voltage Reference; NOTE 2		1.72		1.98	1.72		1.98	1.72		1.98	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 3		1.2		3.3	1.2		3.3	1.2		3.3	V
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 4		150	800	1200	150	800	1200	150	800	1200	mV
$I_{IH}$	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK0, PCLK1	-10			-10			-10			$\mu A$
		nPCLK0, nPCLK1	-150			-150			-150			$\mu A$

NOTE: Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$  for the differential inputs.

NOTE 4: The  $V_{CMR}$  and  $V_{PP}$  levels should be such that input low voltage never goes below  $V_{EE}$ .

**Table 4C. LVPECL DC Characteristics,  $V_{CC} = 2.5V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1		1.375	1.475	1.70	1.425	1.495	1.69	1.42	1.495	1.685	V
$V_{OL}$	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.86	0.64	0.735	0.85	V
$V_{IH}$	Input High Voltage (CLK_SEL, nEN)		1.275		1.56	1.275		1.56	1.275		1.56	V
$V_{IL}$	Input Low Voltage (CLK_SEL, nEN)		0.63		0.965	0.63		0.965	0.63		0.965	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 2		1.2		2.5	1.2		2.5	1.2		2.5	V
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 3		150	800	1200	150	800	1200	150	800	1200	mV
$I_{IH}$	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK0, PCLK1	-10			-10			-10			$\mu A$
		nPCLK0, nPCLK1	-150			-150			-150			$\mu A$

NOTE: Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$  for the differential inputs.

NOTE 3: The  $V_{CMR}$  and  $V_{PP}$  levels should be such that input low voltage never goes below  $V_{EE}$ .

**Table 4D. ECL DC Characteristics,  $V_{CC} = 0V$ ;  $V_{EE} = -3.8V$  to  $-2.375V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1		-1.125	-1.025	-0.80	-1.075	-1.005	-0.805	-1.08	-1.005	-0.815	V
$V_{OL}$	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
$V_{IH}$	Input High Voltage (CLK_SEL, nEN)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
$V_{IL}$	Input Low Voltage (CLK_SEL, nEN)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
$V_{BB}$	Output Voltage Reference; NOTE 2		-1.58		-1.32	-1.58		-1.32	-1.58		-1.32	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 3		$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	V
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 4		150	800	1200	150	800	1200	150	800	1200	mV
$I_{IH}$	Input High Current	PCLK0, PCLK1			150			150			150	$\mu A$
		nPCLK0, nPCLK1										
$I_{IL}$	Input Low Current	PCLK0, PCLK1	-10			-10			-10			$\mu A$
		nPCLK0, nPCLK1	-150			-150			-150			$\mu A$

NOTE: Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$  for the differential inputs.

NOTE 4: The  $V_{CMR}$  and  $V_{PP}$  levels should be such that input low voltage never goes below  $V_{EE}$ .

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{CC} = -3.8V$  to  $-2.375V$  or ,  $V_{CC} = 2.375V$  to  $3.8V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Output Frequency			2			2			2	GHz
$t_{PD}$	Propagation Delay; NOTE 1	250		425	300		450	350		500	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section ( $f = 156.25MHz$ , 12kHz - 20MHz)		0.06	0.10		0.07	0.10		0.08	0.10	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 4			55			55			55	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			100			100			100	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	70	220	80		220	90		220	ps
$t_S$	Clock Enable Setup Time	100	50		100	50		100	50		ps
$t_H$	Clock Enable Hold Time	200	140		200	140		200	140		ps

NOTE: All parameters are measured at  $f \leq 1GHz$ , unless otherwise noted.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

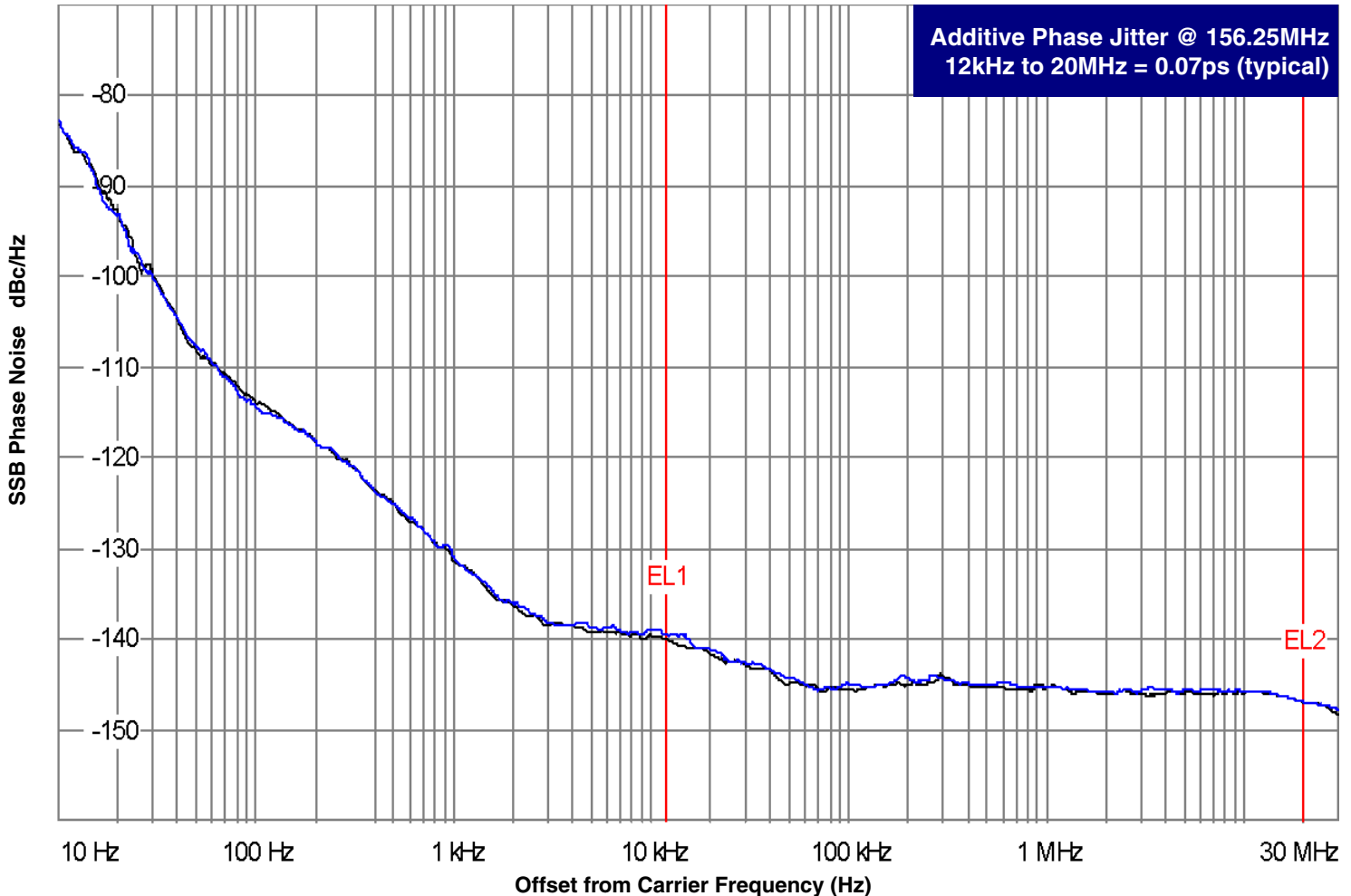
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

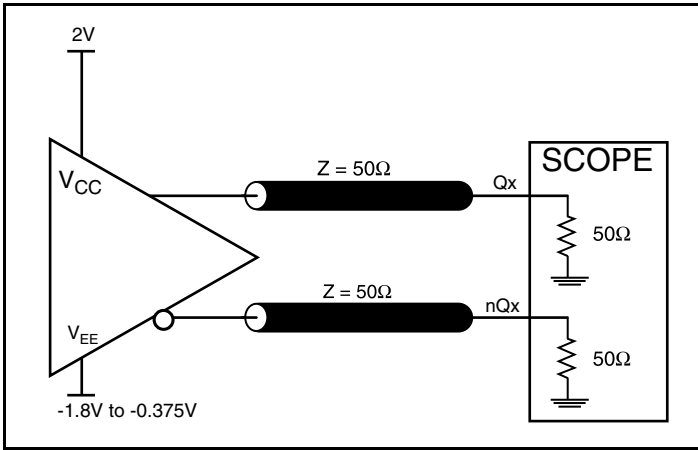


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

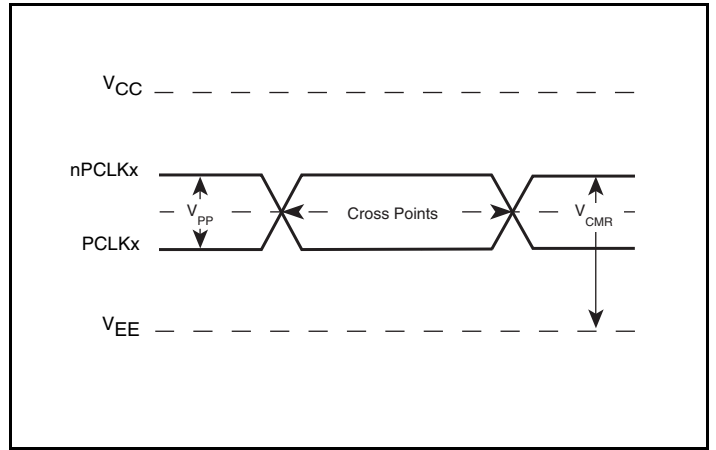
The source generator "IFR2042 10kHz – 5.4GHz Low Noise Signal Generator used as external input to an Agilent 8133A 3GHz Pulse Generator".



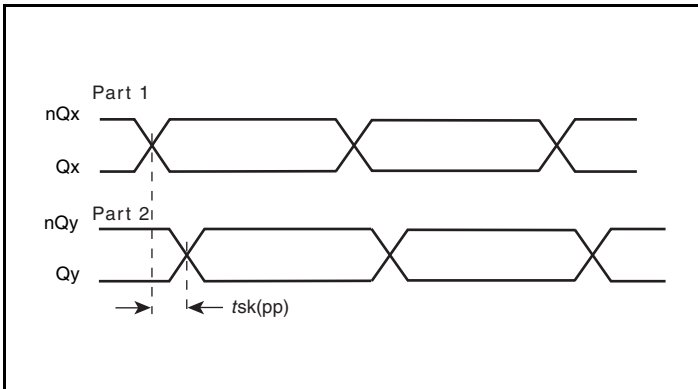
### Parameter Measurement Information



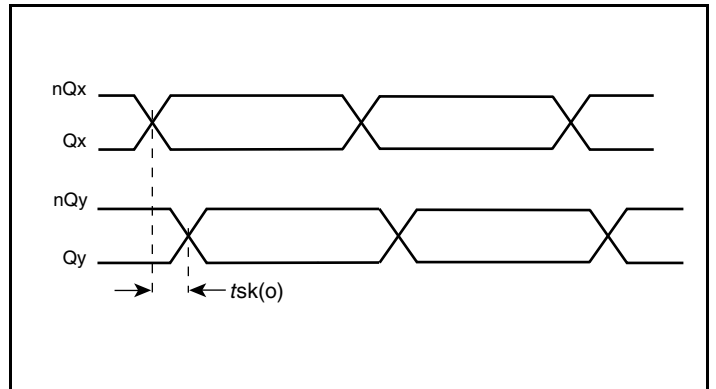
LVPECL Output Load Test Circuit



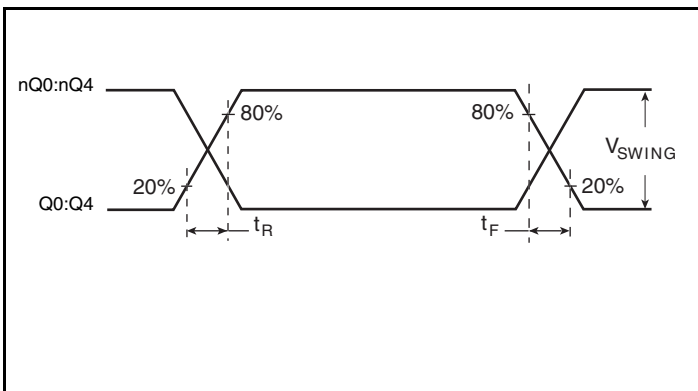
Differential Input Level



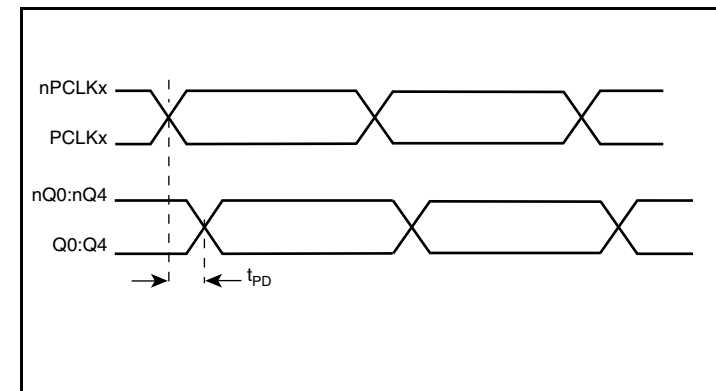
Part-to-Part Skew



Output Skew



Output Rise/Fall Time



Propagation Delay

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line

impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

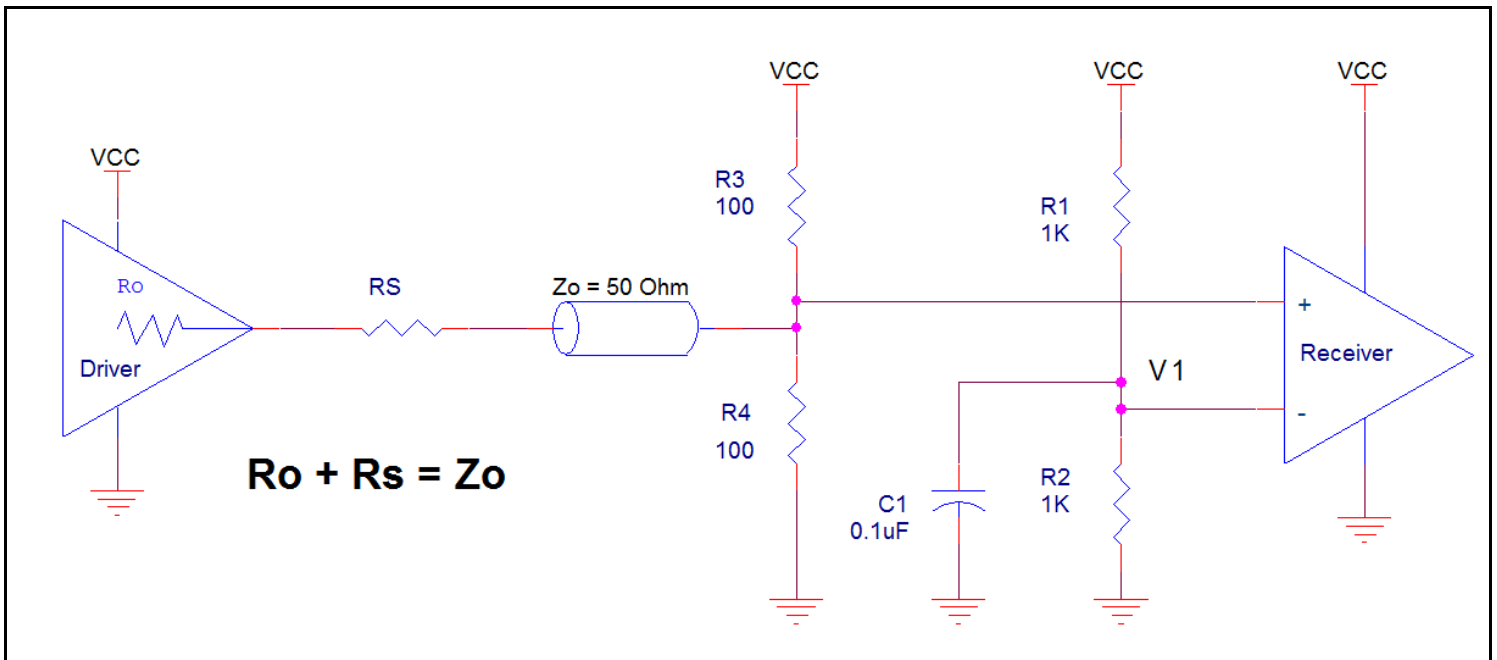
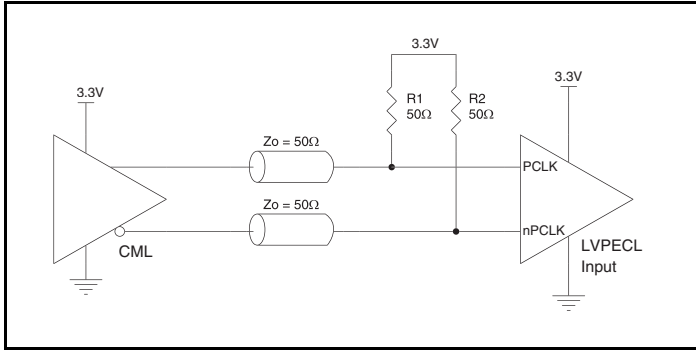


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

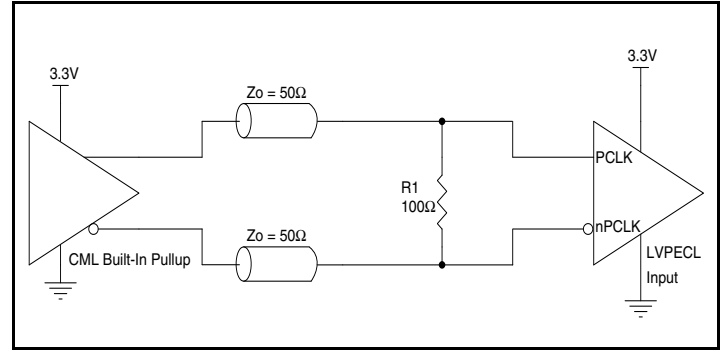
## LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the PCLK/nPCLK input driven by the most common driver types.

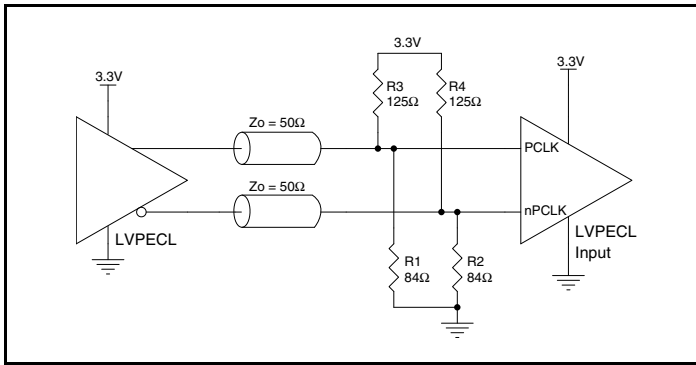
The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



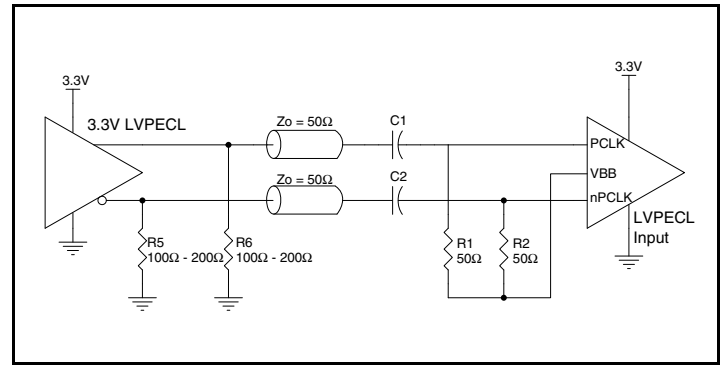
**Figure 3A. PCLK/nPCLK Input Driven by an Open Collector CML Driver**



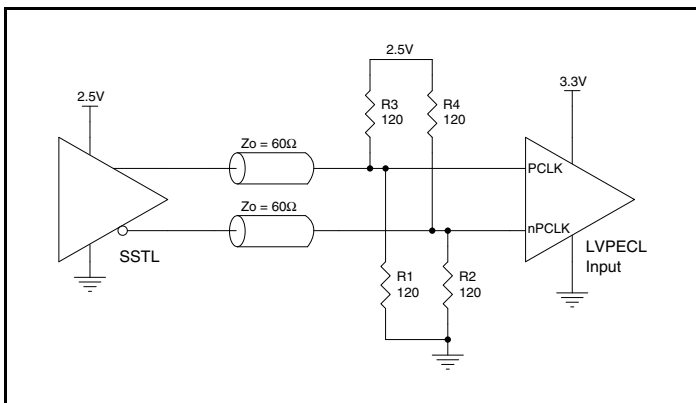
**Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**



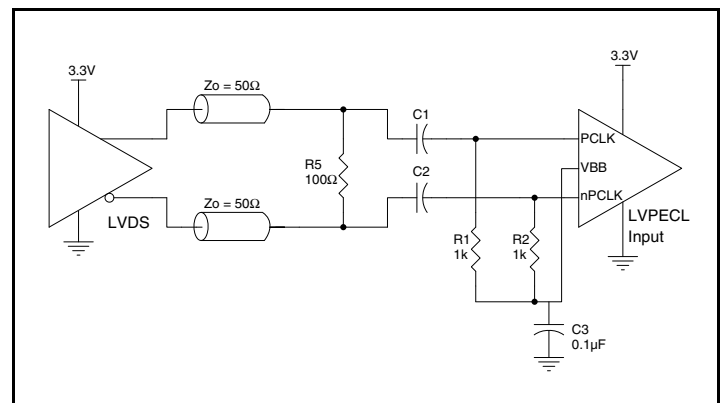
**Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**



**Figure 3E. PCLK/nPCLK Input Driven by an SSTL Driver**



**Figure 3F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

## Recommendations for Unused Output Pins

### Inputs:

#### PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from PCLK to ground.

#### LVC MOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 $\Omega$

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

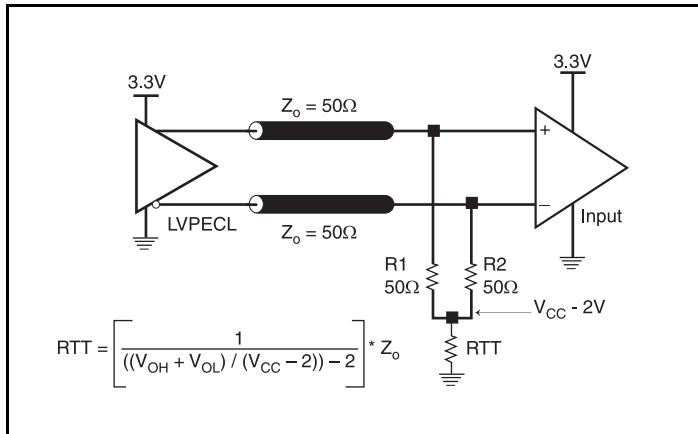


Figure 4A. 3.3V LVPECL Output Termination

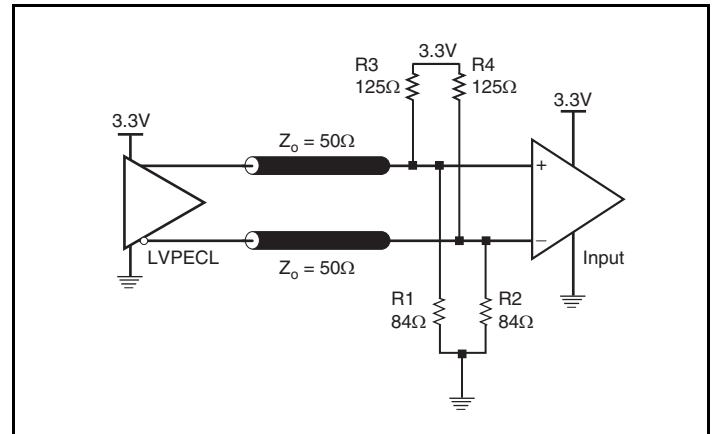


Figure 4B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

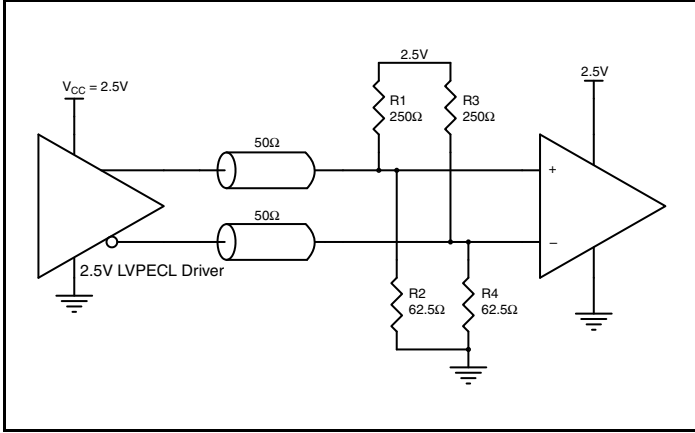


Figure 5A. 2.5V LVPECL Driver Termination Example

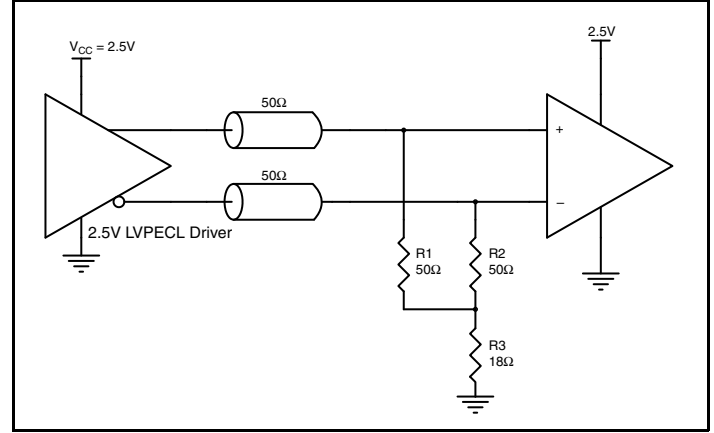


Figure 5B. 2.5V LVPECL Driver Termination Example

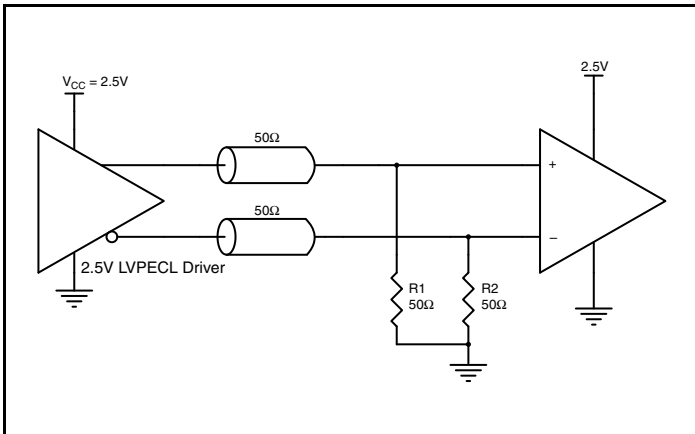
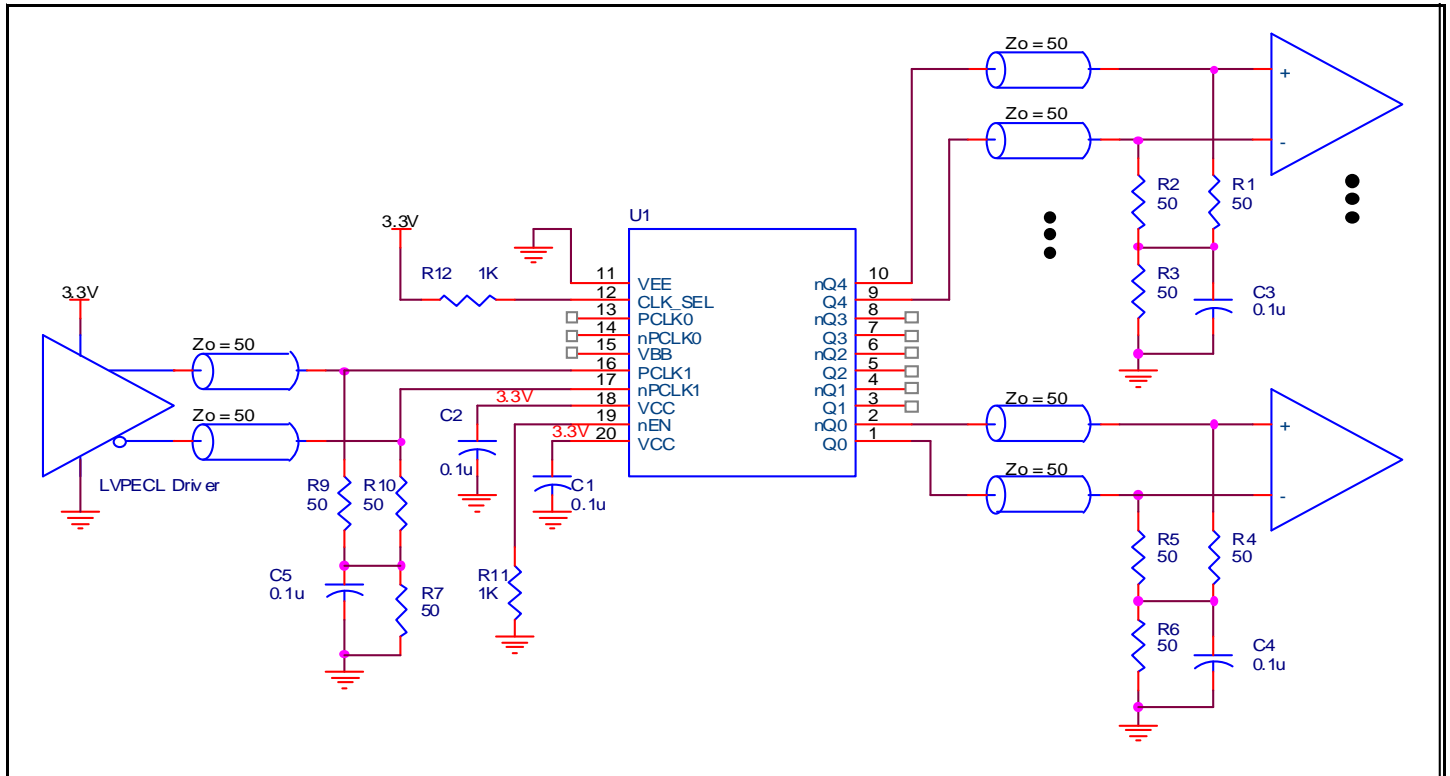


Figure 5C. 2.5V LVPECL Driver Termination Example

## Schematic Example

This application note provides general design guide using ICS853S014I LVPECL buffer. *Figure 6* shows a schematic example of the ICS853S014I LVPECL clock buffer. In this example, the input

is driven by an LVPECL driver. CLK\_SEL is set at logic high to select PCLK1, nPCLK1 input.



**Figure 6. ICS853S014I Example LVPECL Clock Output Buffer Schematic**

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S014I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853S014I is the sum of the core power plus the power dissipated due to the load. The following is the power dissipation for  $V_{CC} = 3.8V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.8V * 68mA = \mathbf{258.4mW}$
- Power (outputs)<sub>MAX</sub> = **30.94mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 30.94mW = \mathbf{154.7mW}$

**Total Power**<sub>MAX</sub> (3.8V, with all outputs switching) =  $258.4mW + 154.7mW = \mathbf{413.1mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.1°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.413\text{W} * 92.1^\circ\text{C/W} = 123^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

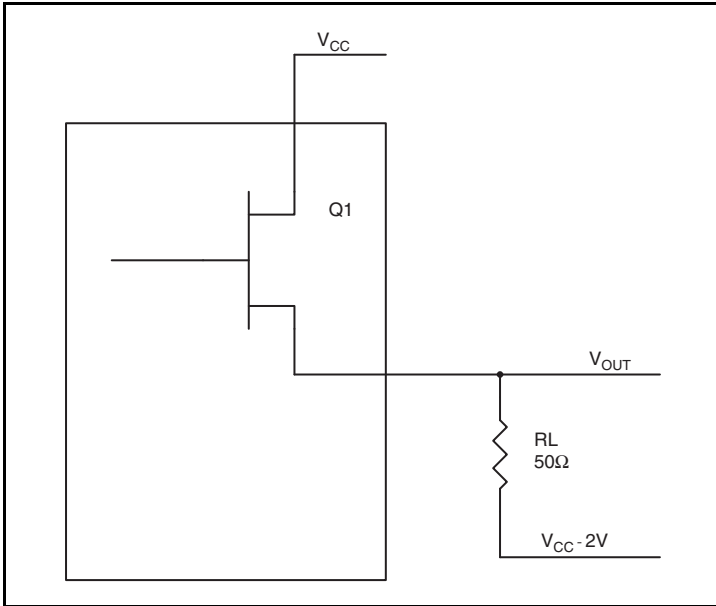
**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W

### T3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate power dissipation due to the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.935V$   
( $V_{CC\_MAX} - V_{OH\_MAX}$ ) = **0.935V**
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.67V$   
( $V_{CC\_MAX} - V_{OL\_MAX}$ ) = **1.67V**

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = \mathbf{19.92mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = \mathbf{11.02mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{30.94mW}$$



## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W

## Transistor Count

The transistor count for ICS853S014I is: 407

Pin compatible with ICS853014

## Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

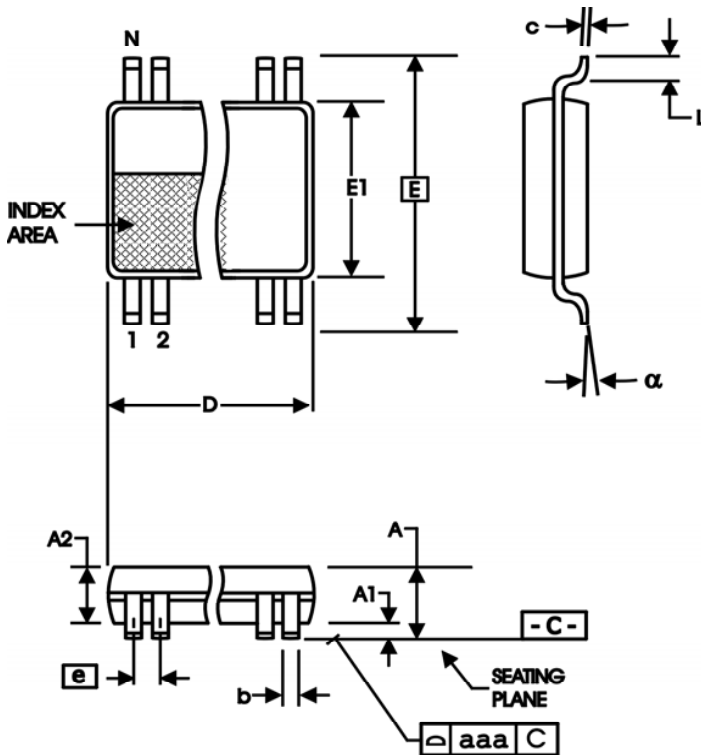


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 9. Ordering Information**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
853S014AGILF	ICS53S014AIL	"Lead-Free" 20 Lead TSSOP	Tube	-40°C to 85°C
853S014AGILFT	ICS53S014AIL	"Lead-Free" 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5	7	AC Characteristics Table - added Additive Phase Jitter max. spec.	9/1/10
C	T6B T7B T8B T9	1 4 15 16 18 19 20	Added 20 Lead VFQFN proposed pin assignment. Absolute Maximum Ratings - added 32 Lead VFQFN Package Thermal Impedance. Added <i>VFQFN EPad Thermal Release</i> section. Added proposed <i>20 Lead VFQFN Thermal Resistance</i> table. Added proposed <i>20 Lead VFQFN theta ja</i> table. Added proposed <i>20 Lead VFQFN Package Outline and Dimensions</i> . Ordering Information Table added proposed <i>20 Lead VFQFN ordering information</i> .	10/29/10
D	T9	10 15 18	Deleted all "Proposed" VFQFN Package References throughout the datasheet. Updated Application Note, Wiring the Differential Input Levels to Accept Single-ended Levels. Deleted Application Note, <i>VFQFN EPAD Thermal Release Path</i> . Ordering Information Table - deleted tape & reel count; deleted VFQFN package information.	5/23/13

## We've Got Your Timing Solution



6024 Silver Creek Valley Road  
San Jose, California 95138

**Sales**  
800-345-7015 (inside USA)  
+408-284-8200 (outside USA)  
Fax: 408-284-2775  
[www.IDT.com/go/contactIDT](http://www.IDT.com/go/contactIDT)

**Technical Support**  
[netcom@idt.com](mailto:netcom@idt.com)  
+480-763-2056

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2013. All rights reserved.