PRELIMINARY

Integrated Circuit Systems, Inc.

ICS854058
8:1
DIFFERENTIAL-TO-LVDS CLOCK MULTIPLEXER

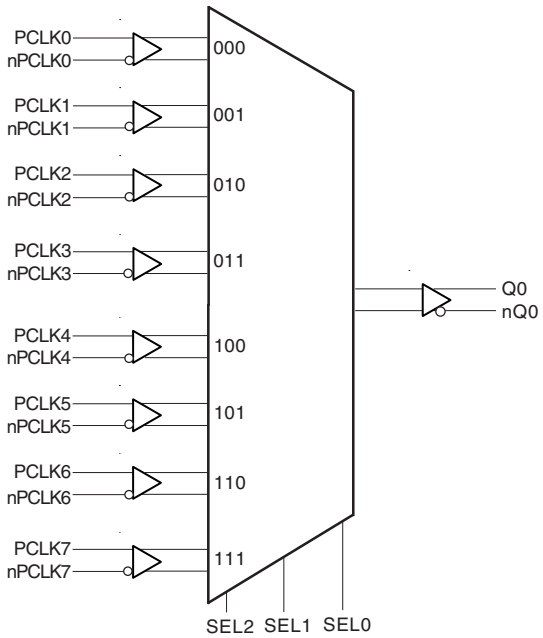
GENERAL DESCRIPTION

The ICS854058 is an 8:1 Differential-to-LVDS Clock Multiplexer which can operate up to 2.5GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS854058 has 8 selectable differential clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL2 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 000 selects PCLK0, nPCLK0).

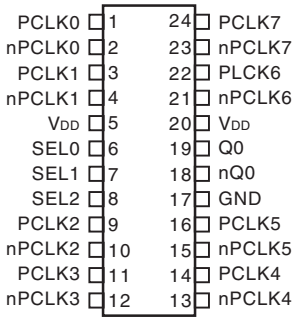
FEATURES

- High speed 8:1 differential multiplexer
- 1 differential LVDS output
- 8 selectable differential PCLK, nPCLK inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2.5GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Part-to-part skew: TBD
- Propagation delay: 595ps (typical)
- Supply voltage range: 3.135V to 3.465V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS854058
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.92mm body package
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK0	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK1	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
5, 20	V_{DD}	Power		Positive supply pins.
6, 7, 8	SEL0, SEL1, SEL2	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
9	PCLK2	Input	Pulldown	Non-inverting differential LVPECL clock input.
10	nPCLK2	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential LVPECL clock input.
12	nPCLK3	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
13	nPCLK4	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
14	PCLK4	Input	Pulldown	Non-inverting differential LVPECL clock input.
15	nPCLK5	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
16	PCLK5	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	GND	Power		Power supply ground.
18, 19	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
21	nPCLK6	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
22	PCLK6	Input	Pulldown	Non-inverting differential LVPECL clock input.
23	nPCLK7	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
24	PCLK7	Input	Pulldown	Non-inverting differential LVPECL clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{VDD/2}$	Pullup/Pulldown Resistors			50		KΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs	
SEL2	SEL1	SEL0	Q0	nQ0
0	0	0	PCLK0	nPCLK0
0	0	1	PCLK1	nPCLK1
0	1	0	PCLK2	nPCLK2
0	1	1	PCLK3	nPCLK3
1	0	0	PCLK4	nPCLK4
1	0	1	PCLK5	nPCLK5
1	1	0	PCLK6	nPCLK6
1	1	1	PCLK7	nPCLK7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			68		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0:SEL2		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	SEL0:SEL2		-0.3		0.8	V
I_{IH}	Input High Current	SEL0:SEL2	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL0:SEL2	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0:PCLK7	V_{DD} = V_{IN} = 3.465V			150	µA
		nPCLK0:nPCLK7	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0:PCLK7	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0:nPCLK7	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15			V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.2			V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%

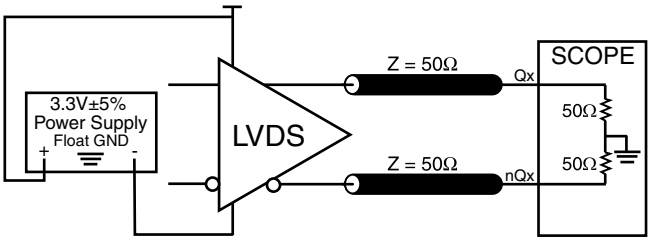
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.135V TO 3.465V

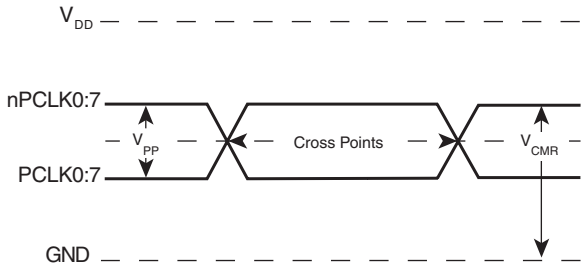
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1			595		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		180		ps

All parameters measured up to 1.3GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

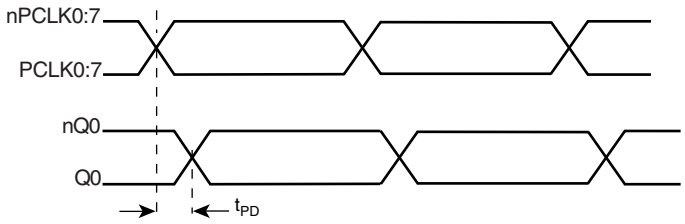
PARAMETER MEASUREMENT INFORMATION



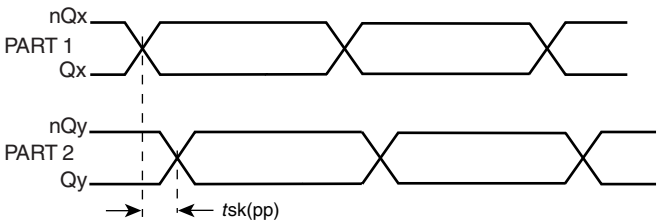
3.3V OUTPUT LOAD AC TEST CIRCUIT



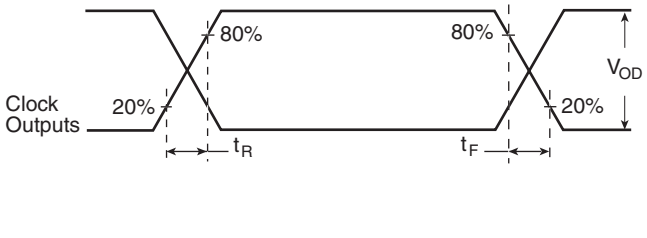
DIFFERENTIAL INPUT LEVEL



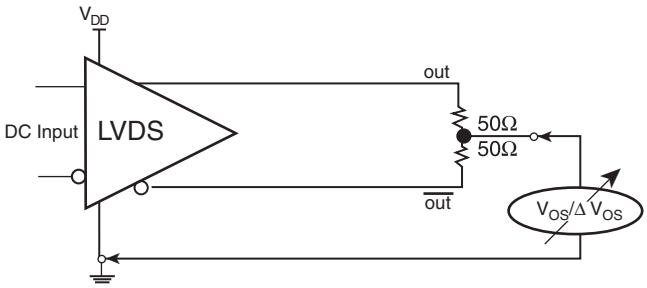
PROPAGATION DELAY



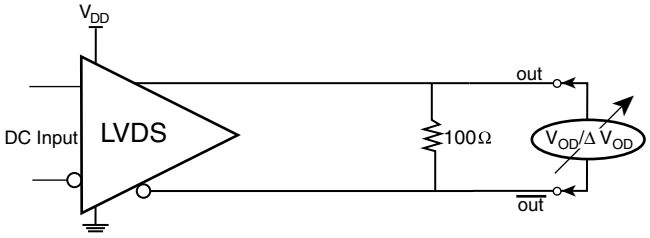
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE



DIFFERENTIAL OUTPUT VOLTAGE

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

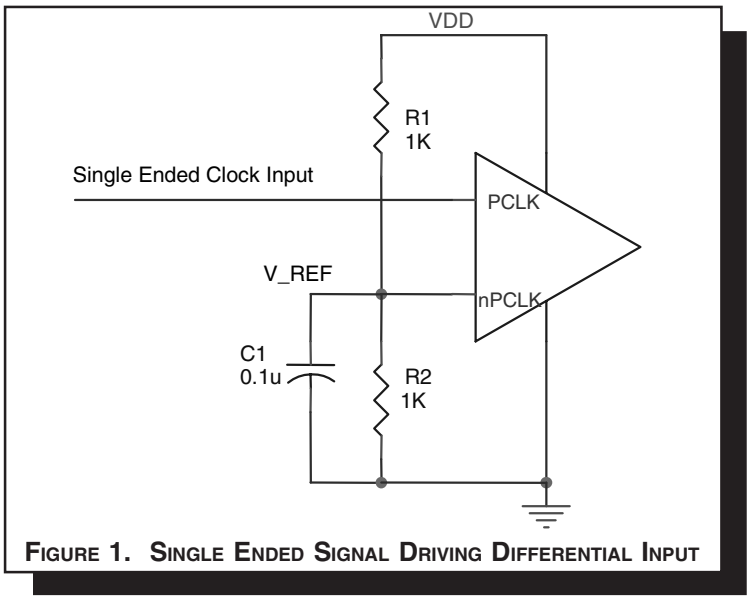


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 2.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

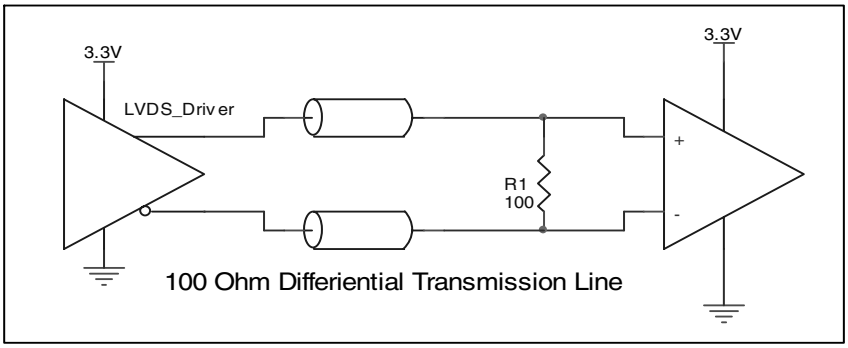


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

LVPE CL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

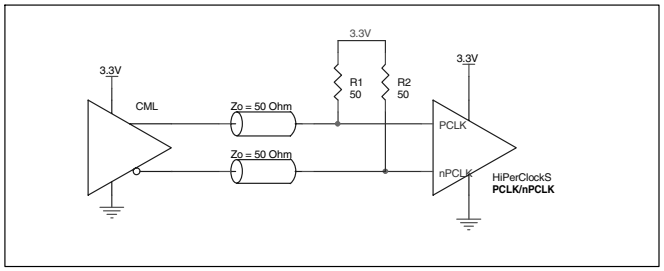


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

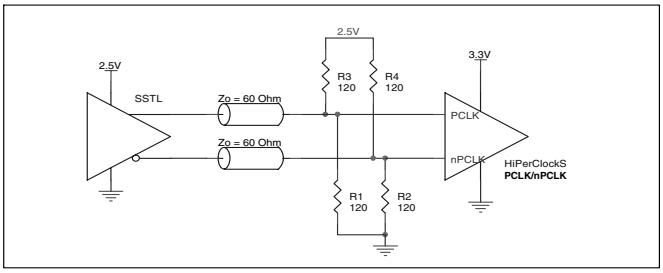


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL IN DRIVER

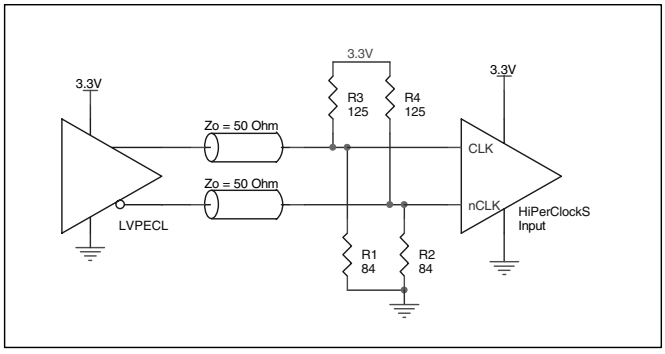


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

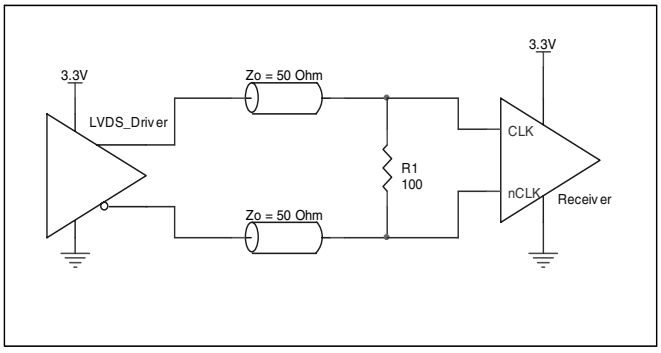


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

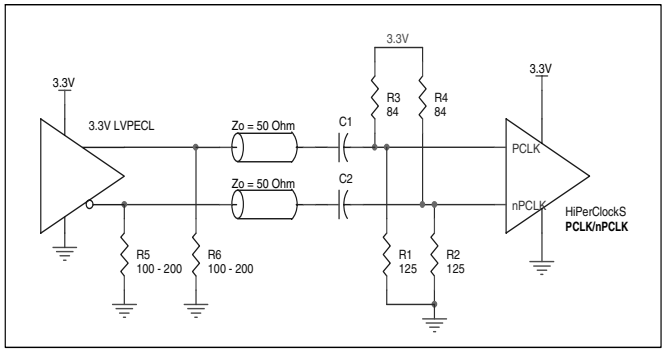


FIGURE 3E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

An application schematic example of ICS854058 is shown in *Figure 4.* The inputs can accept various types of differential signals. In this example, the inputs are driven by LVDS drivers. The transmission lines are assumed to be 100Ω differential. The 100Ω matched loads termination should be located near the receivers. It is recommended at least one decoupling capacitor per power pin. The decoupling capacitor should be low ESR and located as close as possible to the power pin.

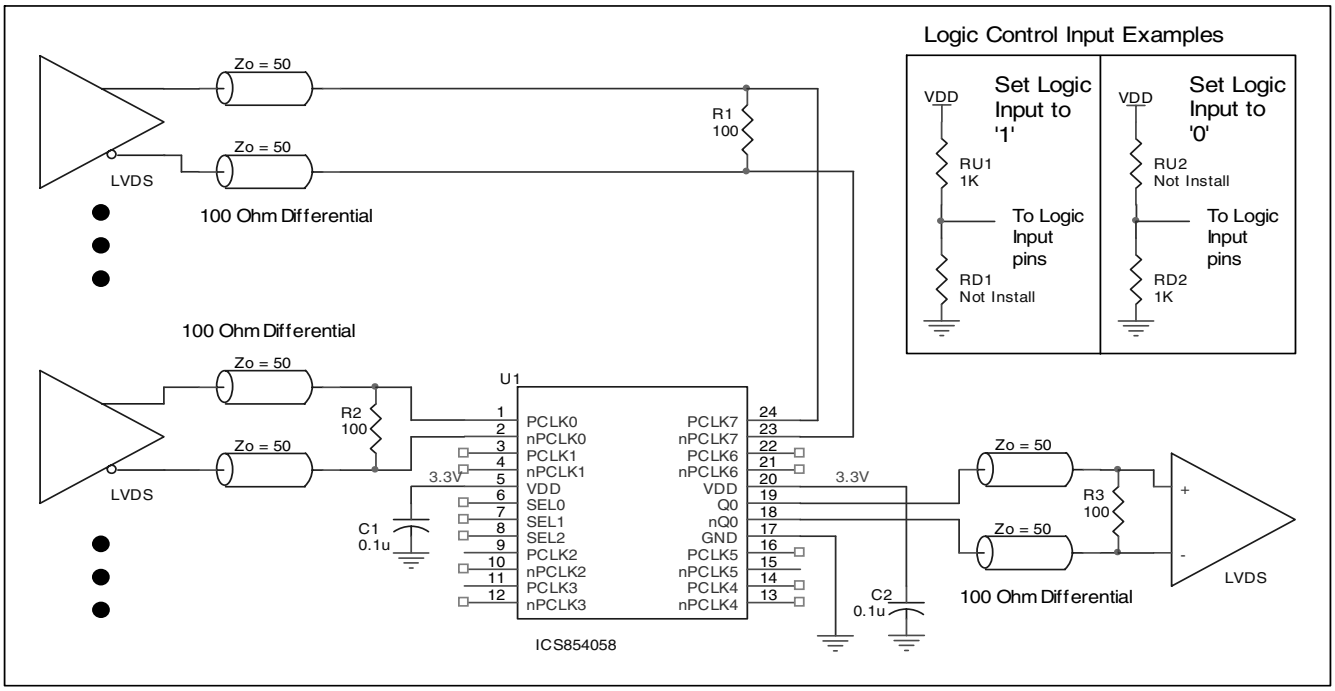


FIGURE 4. ICS854058 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

TRANSISTOR COUNT

The transistor count for ICS854058 is: 361

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

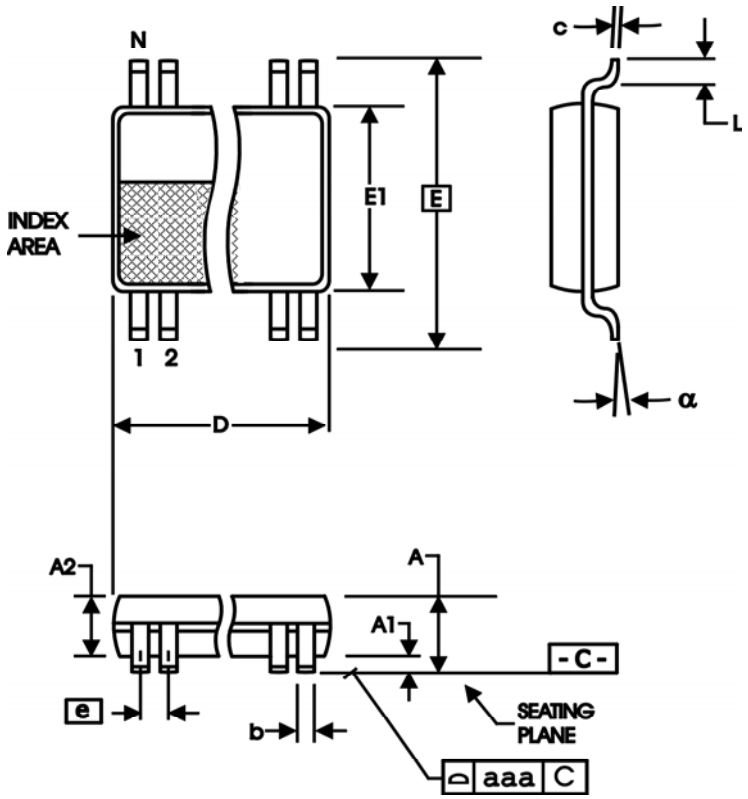


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS854058AG	ICS854058AG	24 Lead TSSOP	60 per tube	-40°C to 85°C
ICS854058AG	ICS854058AG	24 Lead TSSOP on Tape and Reel	2500	-40°C to 85°C