Integrated Circuit Systems, Inc.

ICS85408

LOW SKEW, 1-TO-8 DIFFERENTIAL-TO-LVDS CLOCK DISTRIBUTION CHIP

GENERAL DESCRIPTION

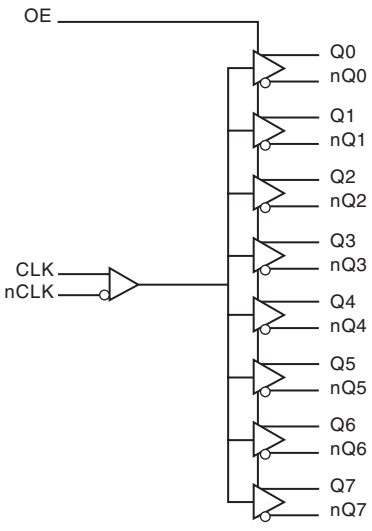
The ICS85408 is a low skew, high performance 1-to-8 Differential-to-LVDS Clock Distribution Chip and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85408 CLK, nCLK pair can accept most differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the ICS85408 provides a low power, low noise, low skew, point-to-point solution for distributing LVDS clock signals.

Guaranteed output and part-to-part skew specifications make the ICS85408 ideal for those applications demanding well defined performance and repeatability.

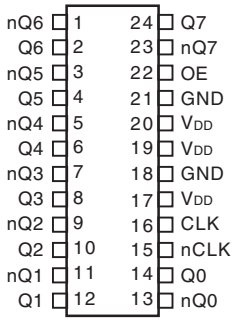
FEATURES

- 8 Differential LVDS outputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, HCSL) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Multiple output enable inputs for disabling unused outputs in reduced fanout applications
- Output skew: 50ps (maximum)
- Part-to-part skew: 550ps (maximum)
- Propagation delay: 2.4ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85408
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ6, Q6	Output		Differential output pair. LVDS interface levels.
3, 4	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
5, 6	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 8	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
9, 10	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
11, 12	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
13, 14	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
15	nCLK	Input	Pullup	Inverting differential clock input.
16	CLK	Input	Pulldown	Non-inverting differential clock input.
17, 19, 20	V_{DD}	Power		Positive supply pins.
18, 21	GND	Power		Power supply ground.
22	OE	Input	Pullup	Output enable. Controls the enabling and disabling of outputs Qx, nQx. When HIGH, the outputs are enabled. When LOW, the outputs are in HiZ. LVCMOS / LVTTL interface levels.
23, 24	nQ7, Q7	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			4		pF

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs	Outputs	
OE	Q0:Q7	nQ0:nQ7
0	HiZ	HiZ
1	ACTIVE	ACTIVE

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q7	nQ0:nQ7		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				90	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE		-0.3		0.8	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{IN} = V_{DD} = 3.465V			150	µA
		nCLK	V_{IN} = V_{DD} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined ast V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

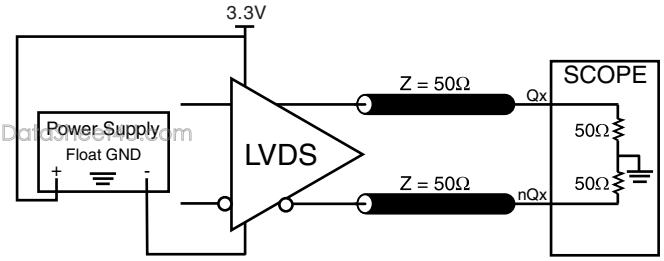
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	400	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.125	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	µA
I_{OFF}	Power Off Leakage		-1		+1	µA
I_{OSD}	Differential Output Short Circuit Current				-5.5	mA
I_{OS}/I_{OSB}	Output Short Circuit Current				-12	mA

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

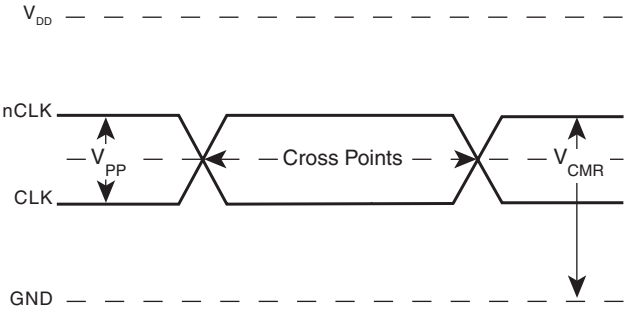
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.6		2.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				550	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		600	ps
odc	Output Duty Cycle		45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5				5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5				5	ns

All parameters measured at f ≤ 622MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This paragraph is defined according with JEDEC Standard 65.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production 5.

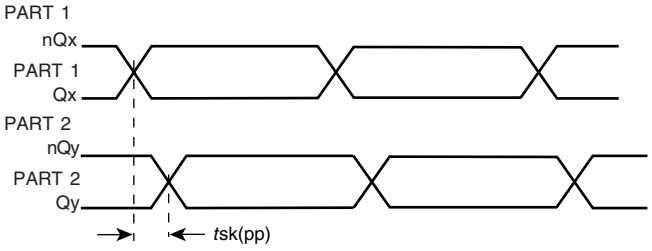
PARAMETER MEASUREMENT INFORMATION



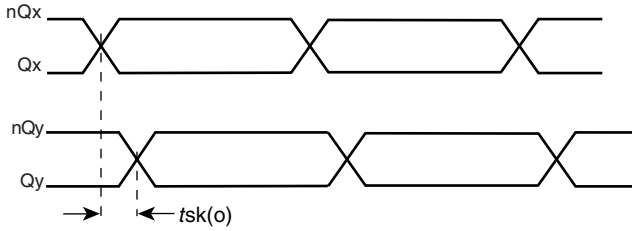
3.3V OUTPUT LOAD AC TEST CIRCUIT



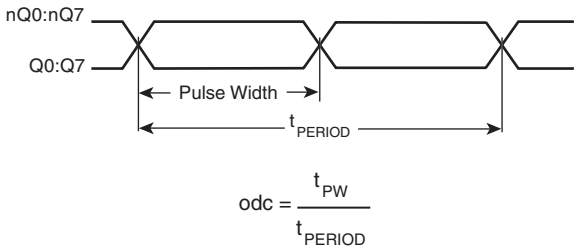
DIFFERENTIAL INPUT LEVEL



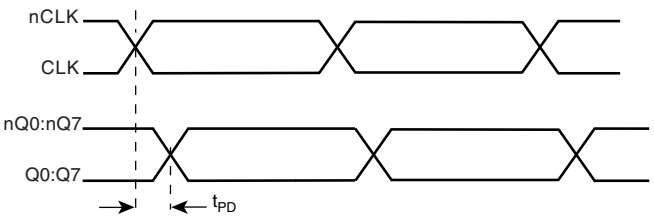
PART-TO-PART SKEW



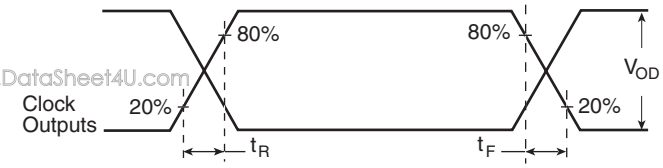
OUTPUT SKEW



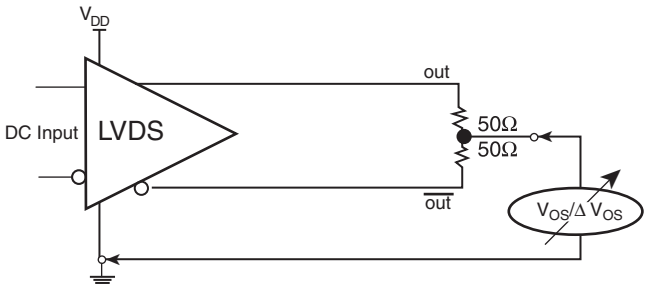
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



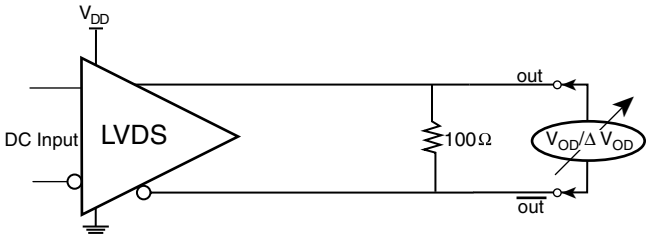
PROPAGATION DELAY



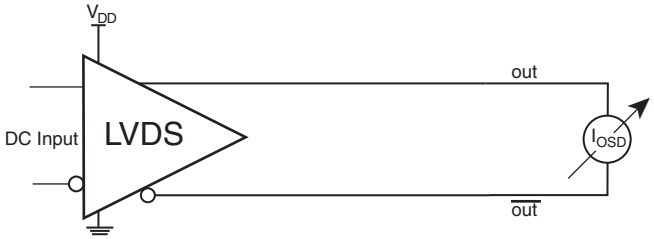
OUTPUT RISE/FALL TIME



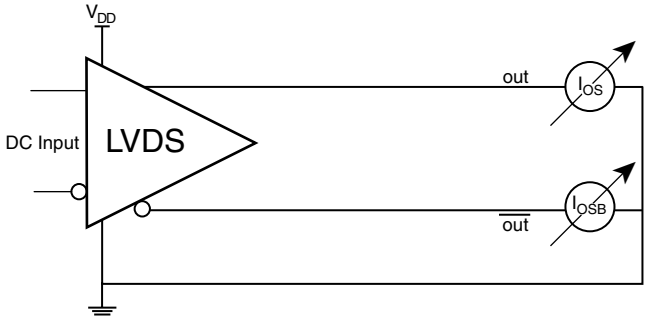
V_{OS} SETUP



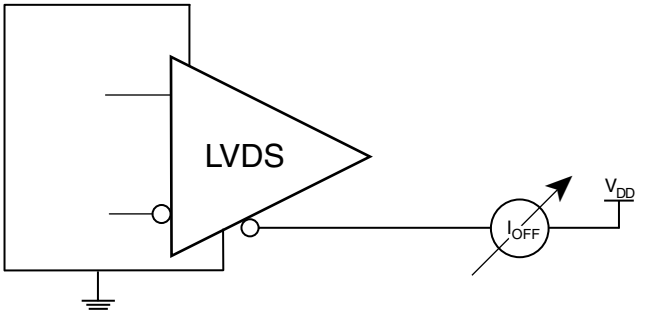
V_{OD} SETUP



I_{OSD} SETUP



I_{OS} SETUP



I_{OFF} SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

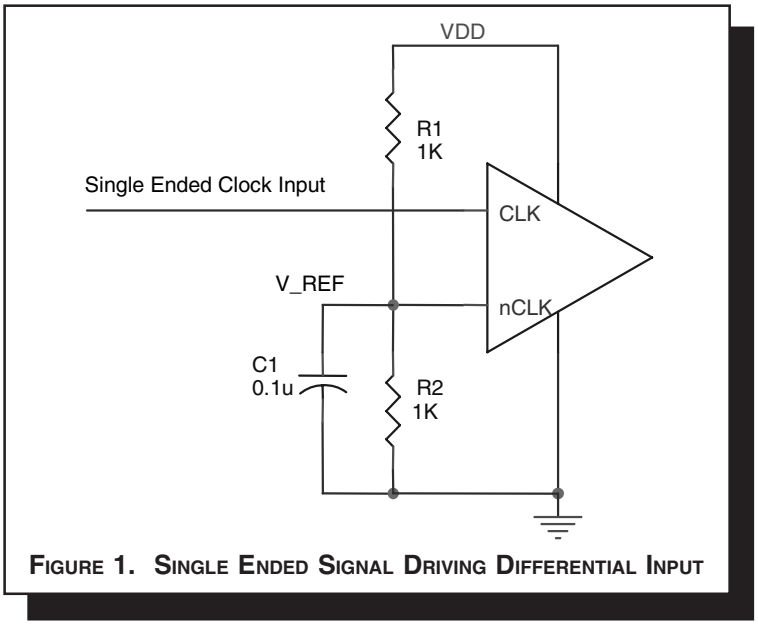


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 2.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

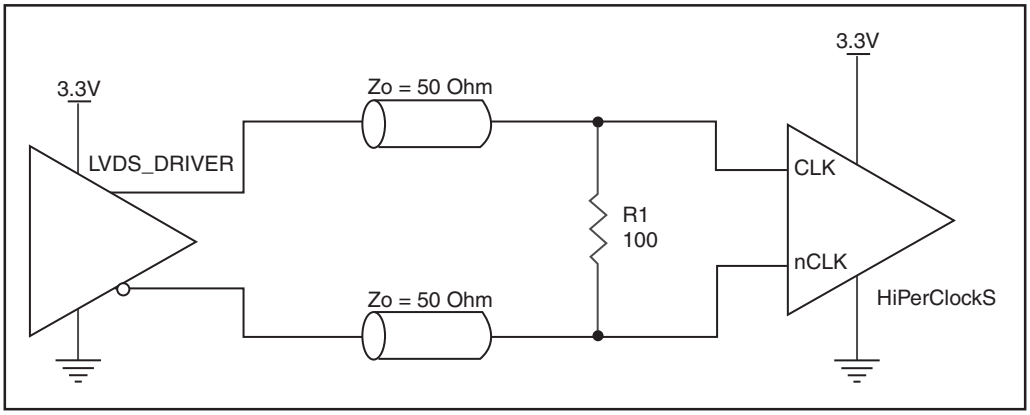


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

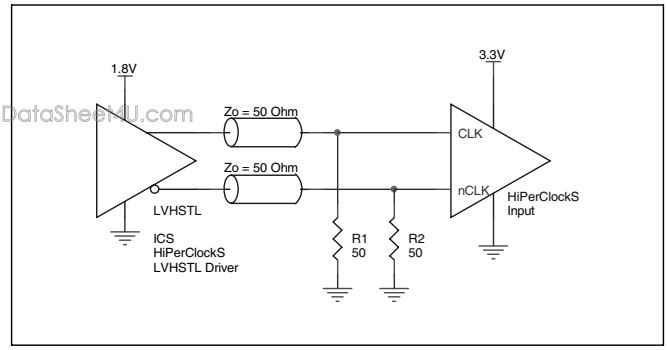


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

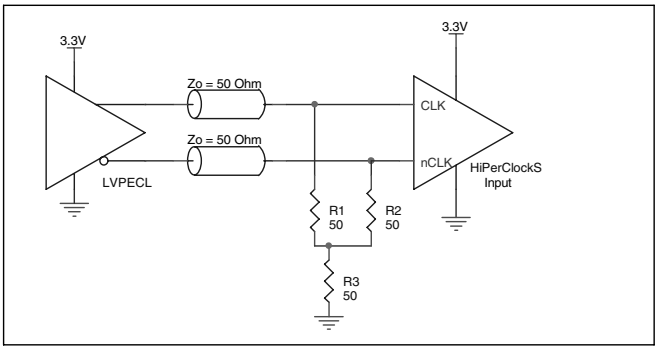


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

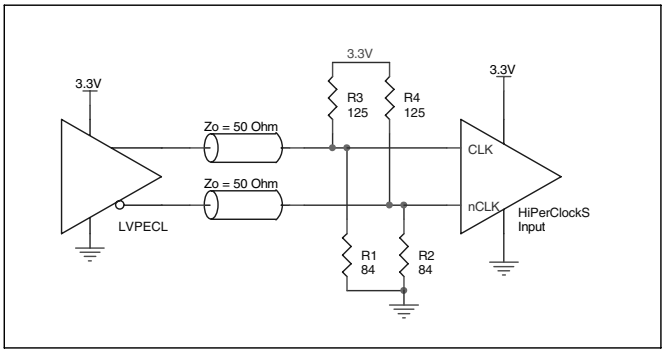


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

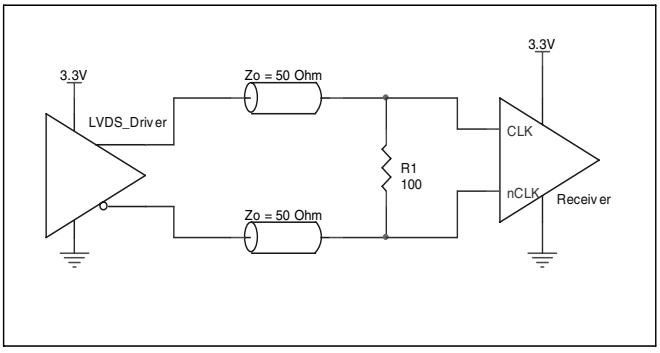


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

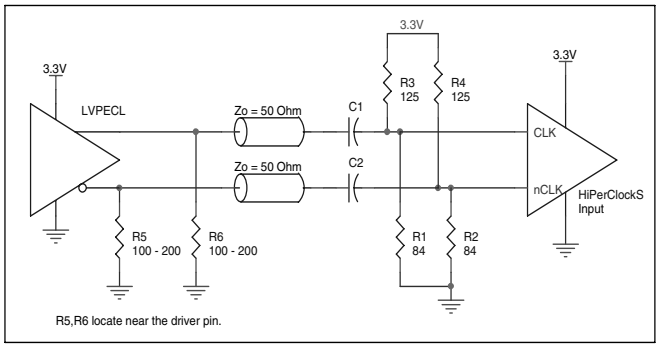


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS85408 is: 1821

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

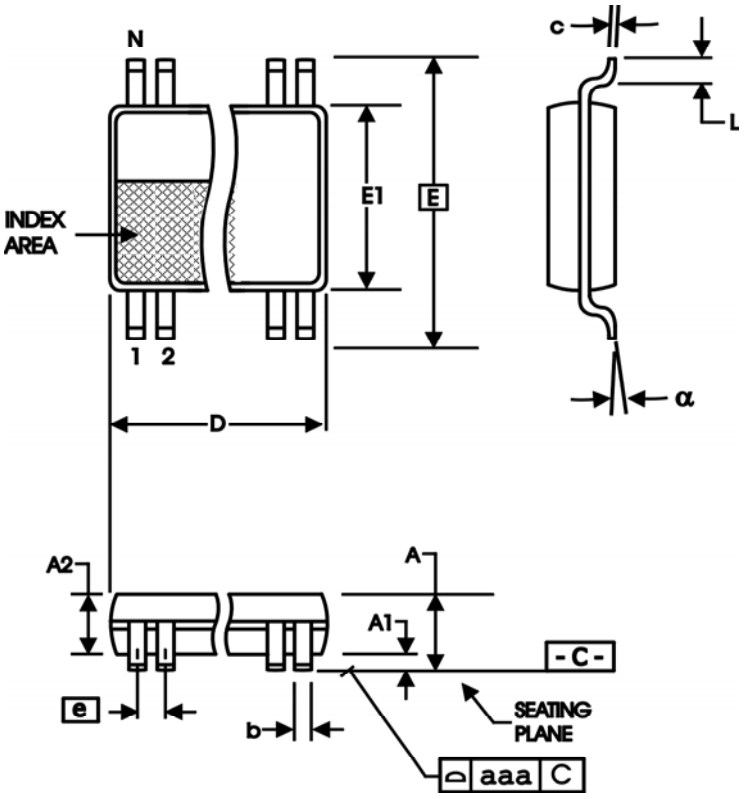


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85408BG	ICS85408BG	24 Lead TSSOP	tube	0°C to 70°C
ICS85408BGT	ICS85408BG	24 Lead TSSOP	1000 tape & reel	0°C to 70°C
ICS85408BGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS85408BGLFT	TBD	24 Lead "Lead-Free" TSSOP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T6 T8	9 11	Reliability Table - revised air flow from Linear Feet per Minute to Meters per Second. Ordering Information Table - corrected typo in Part/Order Number from ICS8540BG to ICS85408BG.	5/6/04
A		1	Pin Assignment - corrected package information from 300-MIL to 173-MIL	8/25/04
A	 T8	1 11	Features Section - added Lead-Free bullet. Corrected Block Diagram. Ordering Information Table - Added Lead-Free part number.	4/25/05