PRELIMINARY

LOW SKEW, DUAL, 1-TO-3 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS854S013

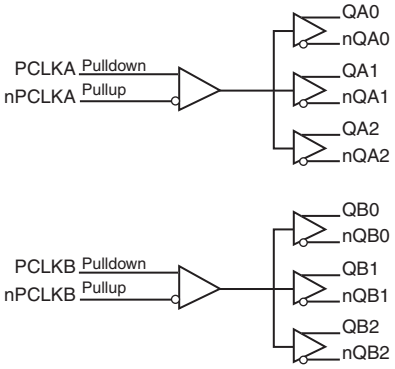
General Description

The ICS854S013 is a low skew, high performance Dual 1-to-3 Differential-to-LVDS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The PCLKx, nPCLKx pairs can accept most standard differential input levels. The ICS854S013 is characterized to operate from a 3.3V power supply. Guaranteed output and bank skew characteristics make the ICS854S013 ideal for those clock distribution applications demanding well defined performance and repeatability.

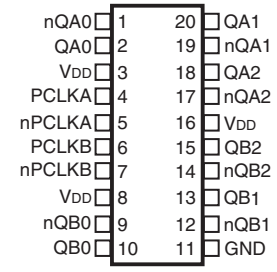
Features

- Two differential LVDS output banks
- Two differential clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >3GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Output skew: <25ps (typical)
- Bank skew: <50ps (typical)
- Propagation delay: TBD
- Additive phase jitter, RMS: 0.15ps (typical)
- Full 3.3V power supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS854S013
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body

G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQA0, QA0	Output		Differential output pair. LVDS interface levels.
3, 8, 16	V_{DD}	Power		Power supply pins.
4	PCLKA	Input	Pulldown	Non-inverting differential clock input.
5	nPCLKA	Input	Pullup	Inverting differential clock input. $V_{DD}/2$ default when left floating.
6	PCLKB	Input	Pulldown	Non-inverting differential clock input.
7	nPCLKB	Input	Pullup	Inverting differential clock input. $V_{DD}/2$ default when left floating.
9, 10	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
11	GND	Power		Power supply ground.
12, 13	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
14, 15	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
17, 18	nQA2, QA2	Output		Differential output pair. LVDS interface levels.
19, 20	nQA1, QA1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
PCLKA, PCLKB	nPCLKA, nPCLKB	QA[0:2], QB[0:2]	nQA[0:2], nQB[0:2]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-ended to Differential	Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	87.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			135		mA

Table 4B. LVPECL Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLKA, PCLKB	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLKA, nPCLKB	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLKA, nPCLKB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			360		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

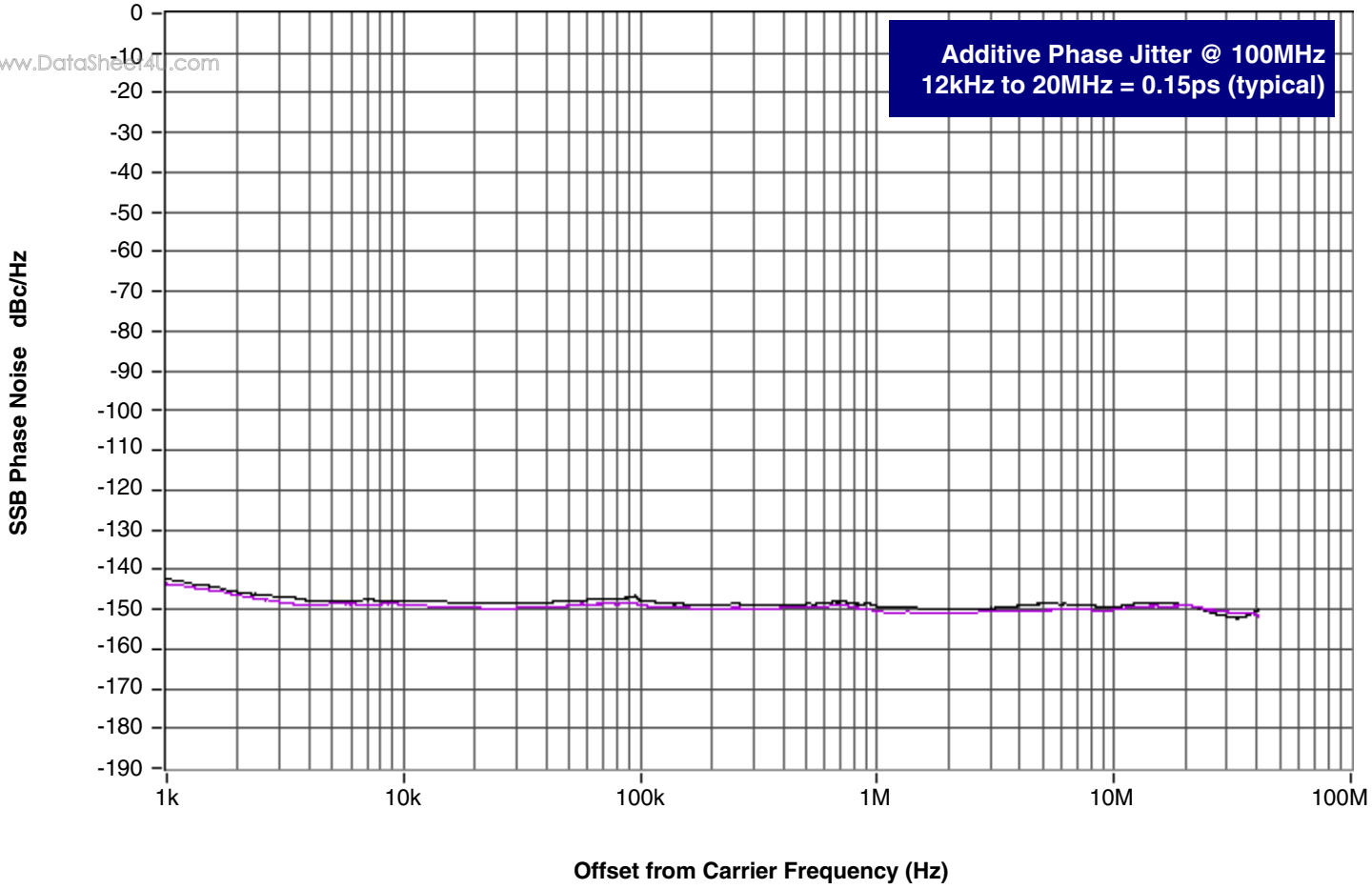
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
t_{PD}	Propagation Delay; NOTE 1			TBD		ps
tsk(o)	Output Skew; NOTE 2, 4			<25		ps
tsk(b)	Bank Skew; NOTE 3, 4			<50		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.15		
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

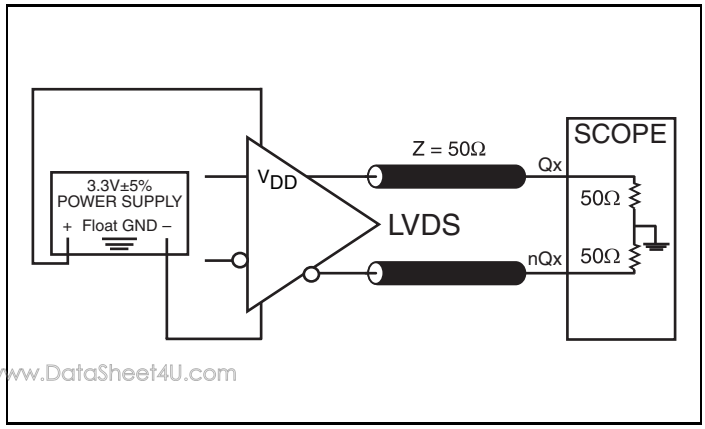
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

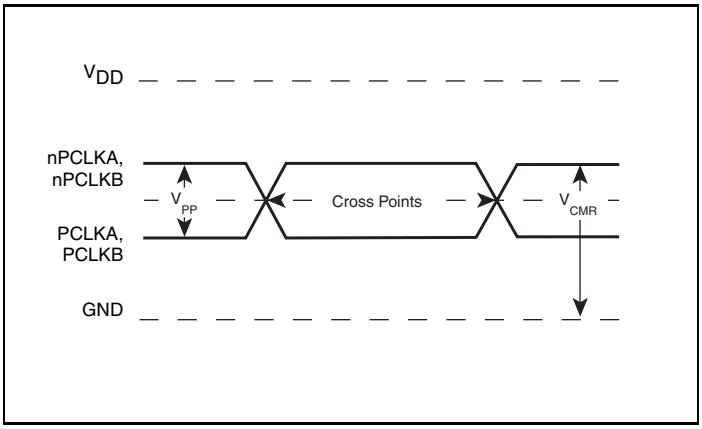


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

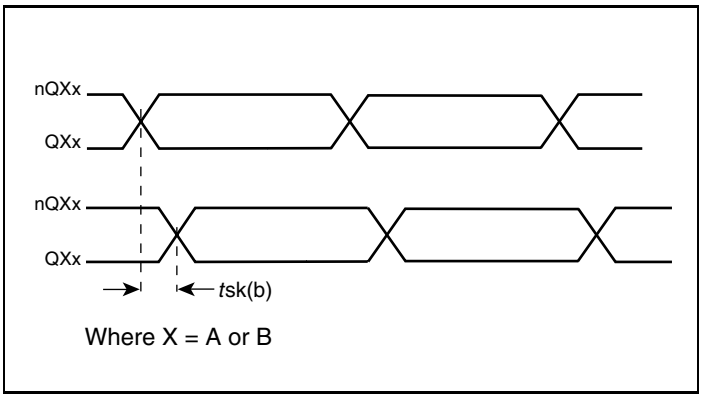
Parameter Measurement Information



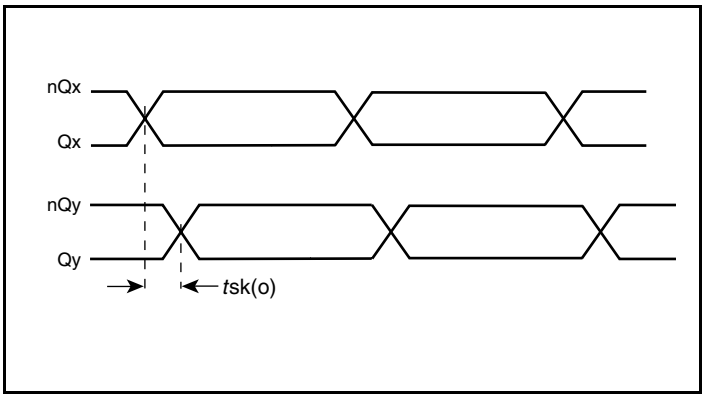
3.3V LVDS Output Load AC Test Circuit



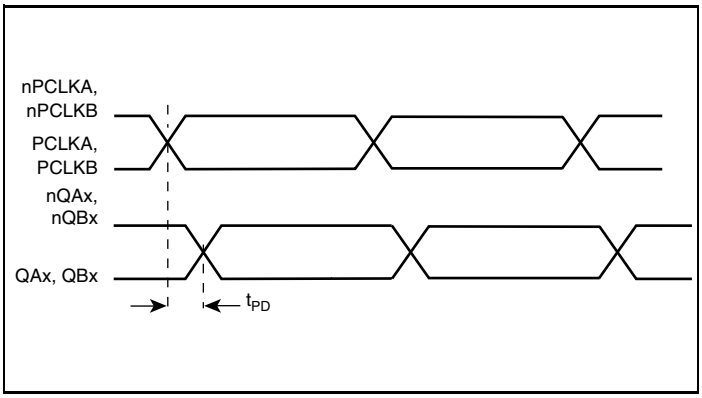
Differential Input Level



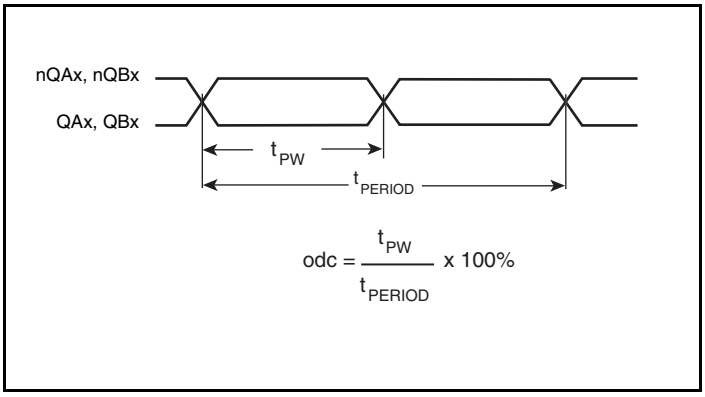
Bank Skew



Output Skew

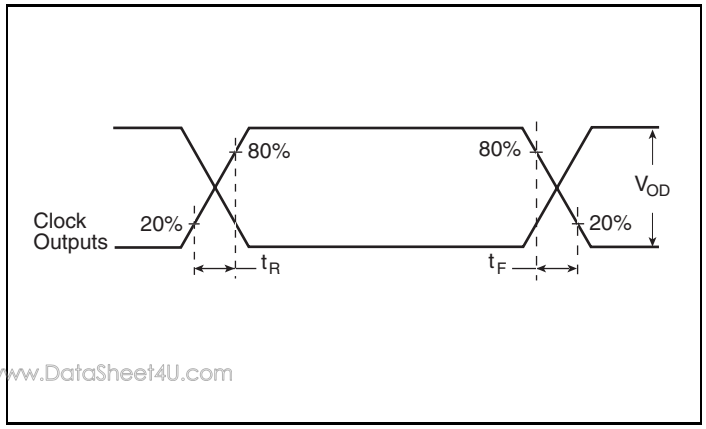


Propagation Delay

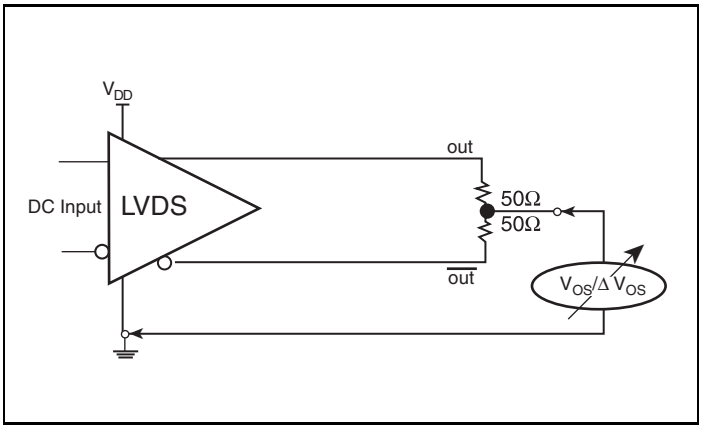


Output Duty Cycle/Pulse Width/Period

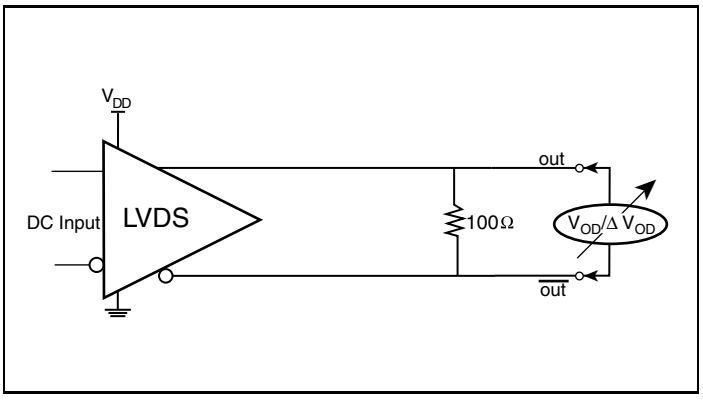
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

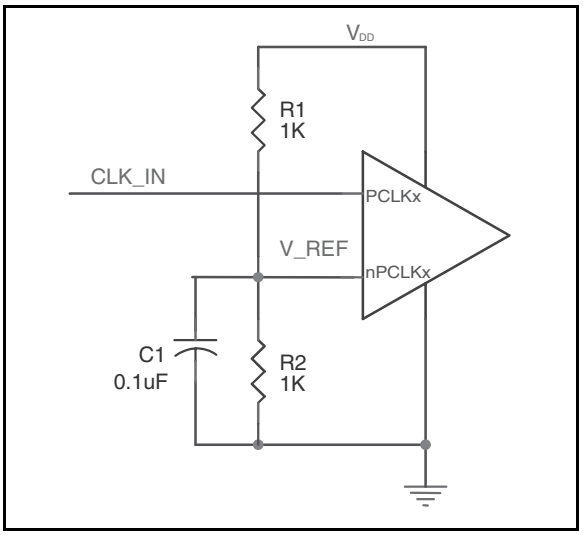


Figure 1. Single-Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

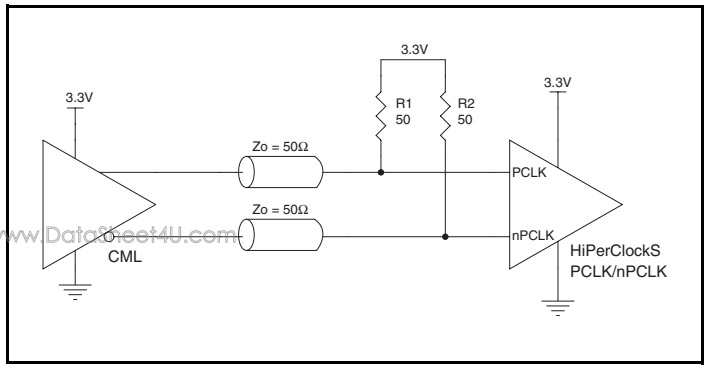


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

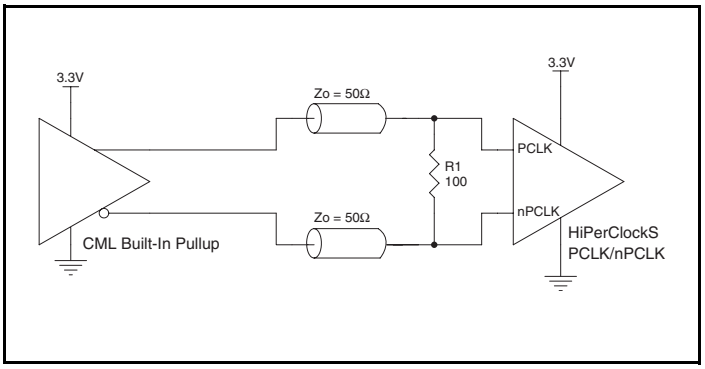


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

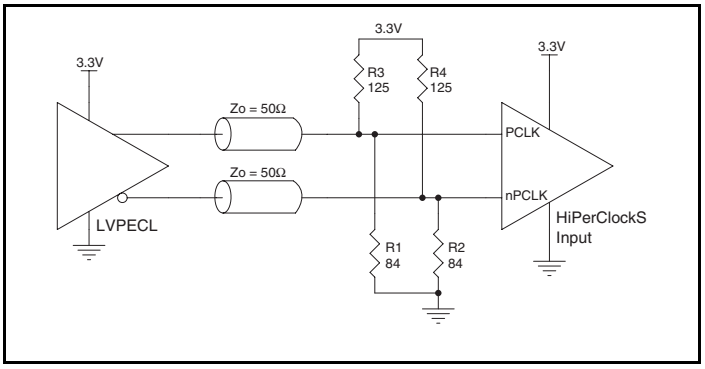


Figure 2C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

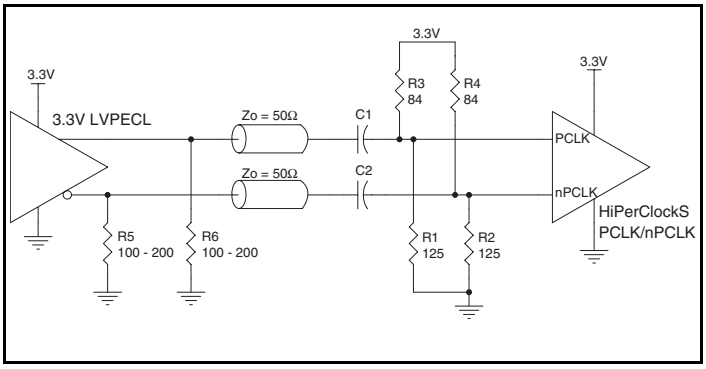


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

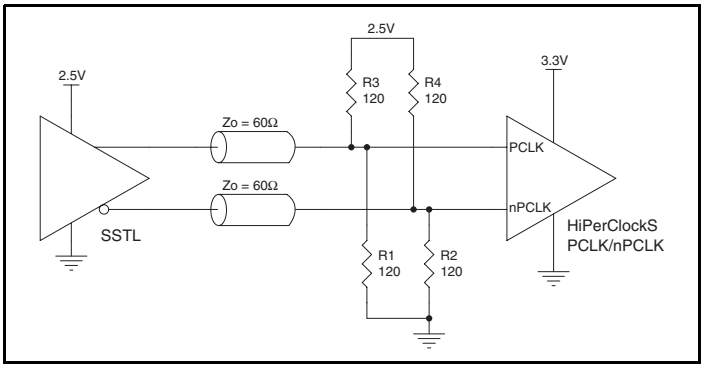


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

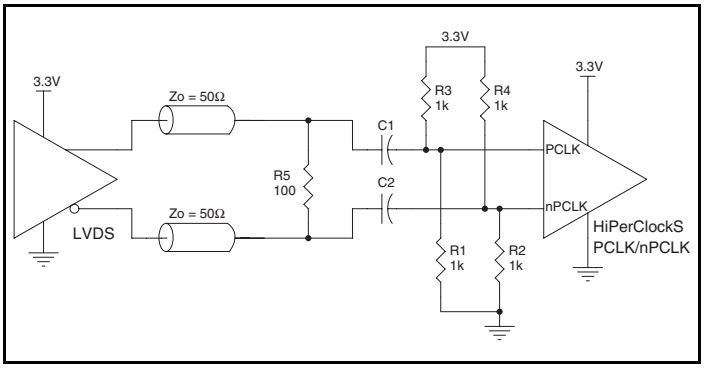


Figure 2F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

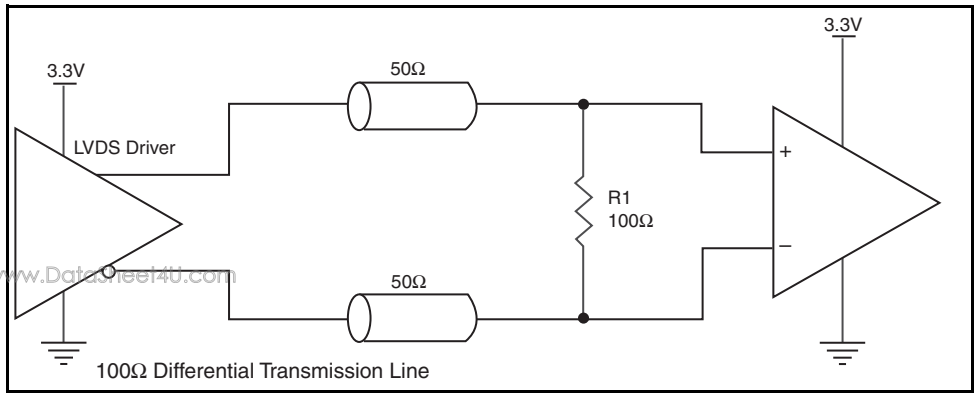


Figure 3. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S013.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S013 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 135mA = **467.77mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.468W * 87.2°C/W = 110.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

Transistor Count

The transistor count for ICS854S013 is: 363

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

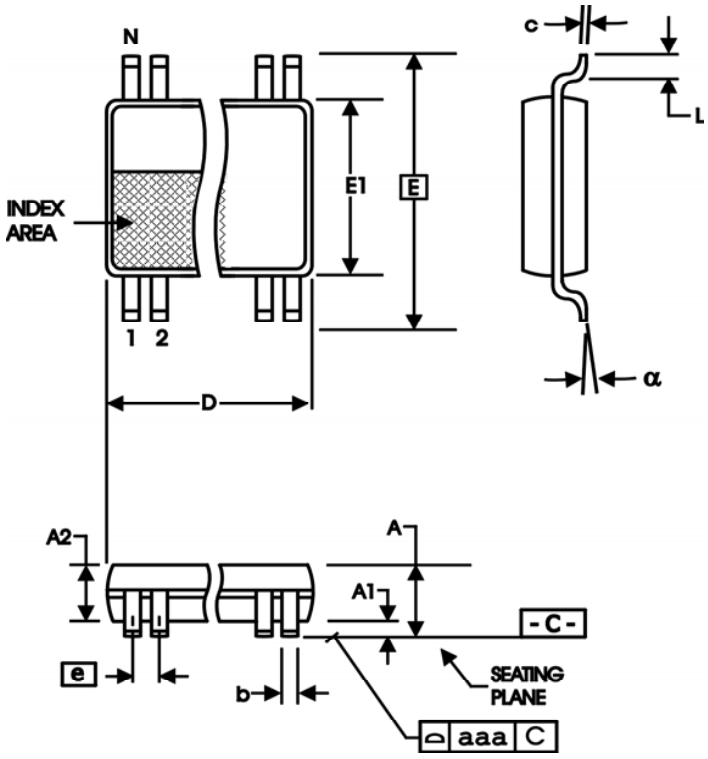


Table 8 Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854S013BG	ICS854S013BG	20 Lead TSSOP	Tube	0°C to 70°C
ICS854S013BGT	ICS854S013BG	20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
ICS854S013BGLF	ICS54S013BL	“Lead-Free” 20 Lead TSSOP	Tube	0°C to 70°C
ICS854S013BGLFT	ICS54S013BL	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia
Integrated Device Technology
IDT (S) Pte. Ltd.
1 Kallang Sector, #07-01/06
Kolam Ayer Industrial Park
Singapore 349276
+65 67443356
Fax: +65 67441764

Japan
NIPPON IDT KK
Sanbancho Tokyu, Bld. 7F,
8-1 Sanbancho
Chiyoda-ku, Tokyo 102-0075
+81 3 3221 9822
Fax: +81 3 3221 9824

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 37885
idteurope@idt.com

www.IDT.com