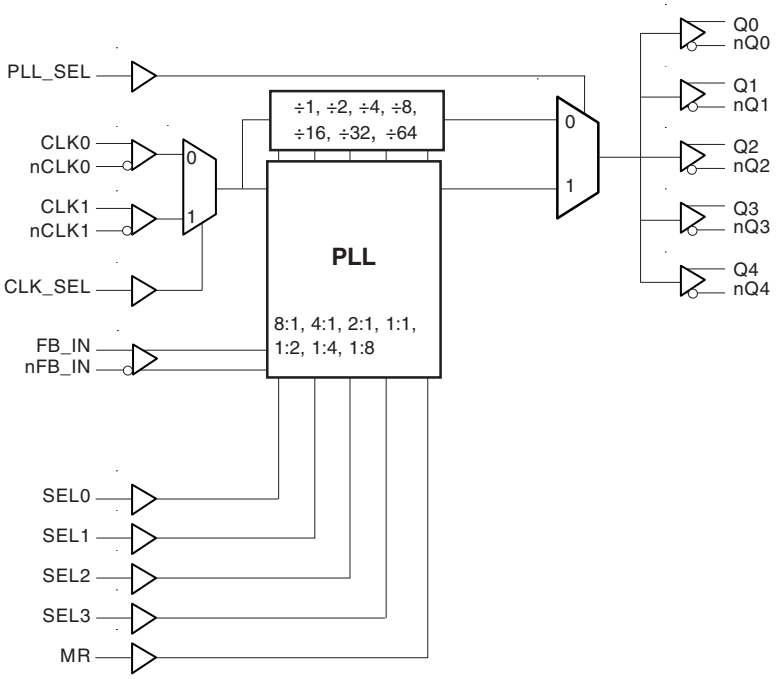
GENERAL DESCRIPTION

The ICS8745B is a highly versatile 1:5 LVDS Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8745B has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The Reference Divider, Feedback Divider and Output Divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

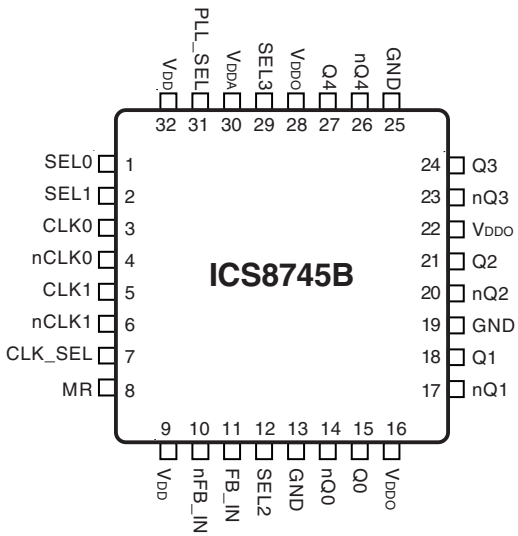
FEATURES

- 5 differential LVDS outputs designed to meet or exceed the requirements of ANSI TIA/EIA-644
- Selectable differential clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 30ps (maximum)
- Output skew: 35ps (maximum)
- Static phase offset: 25ps ± 125ps
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	SEL0	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
2	SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	CLK1	Input	Pulldown	Non-inverting differential clock input.
6	nCLK1	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTL interface levels.
8	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
9, 32	V_{DD}	Power		Core supply pins.
10	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
11	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
12	SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
13, 19, 25	GND	Power		Power supply ground.
14, 15	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
16, 22, 28	V_{DDO}	Power		Output supply pins.
17, 18	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
20, 21	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
26, 27	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
29	SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
30	V_{DDA}	Power		Analog supply pin.
31	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q0:Q4, nQ0:nQ4
0	0	0	0	250 - 700	÷ 1
0	0	0	1	125 - 350	÷ 1
0	0	1	0	62.5 - 175	÷ 1
0	0	1	1	31.25 - 87.5	÷ 1
0	1	0	0	250 - 700	÷ 2
0	1	0	1	125 - 350	÷ 2
0	1	1	0	62.5 - 175	÷ 2
0	1	1	1	250 -700	÷ 4
1	0	0	0	125 - 350	÷ 4
1	0	0	1	250 - 700	÷ 8
1	0	1	0	125 - 350	x 2
1	0	1	1	62.5 - 175	x 2
1	1	0	0	31.25 - 87.5	x 2
1	1	0	1	62.5 - 175	x 4
1	1	1	0	31.25 - 87.5	x 4
1	1	1	1	31.25 - 87.5	x 8

*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

TABLE 3B. PLL BYPASS FUNCTION TABLE

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q0:Q4, nQ0:nQ4
0	0	0	0	÷ 4
0	0	0	1	÷ 4
0	0	1	0	÷ 4
0	0	1	1	÷ 8
0	1	0	0	÷ 8
0	1	0	1	÷ 8
0	1	1	0	÷ 16
0	1	1	1	÷ 16
1	0	0	0	÷ 32
1	0	0	1	÷ 64
1	0	1	0	÷ 2
1	0	1	1	÷ 2
1	1	0	0	÷ 4
1	1	0	1	÷ 1
1	1	1	0	÷ 2
1	1	1	1	÷ 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				125	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				59	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3	$V_{DD} = V_{IN} = 3.465V$			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, FB_IN	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK0, nCLK1, nFB_IN	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, FB_IN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK0, nCLK1, nFB_IN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		320	440	550	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	50	mV
V_{OS}	Offset Voltage		1.05	1.2	1.35	V
ΔV_{OS}	V_{OS} Magnitude Change				25	mV

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

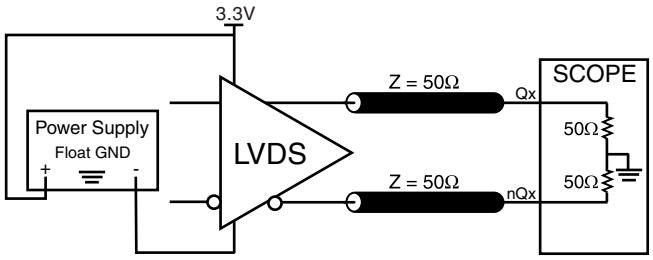
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

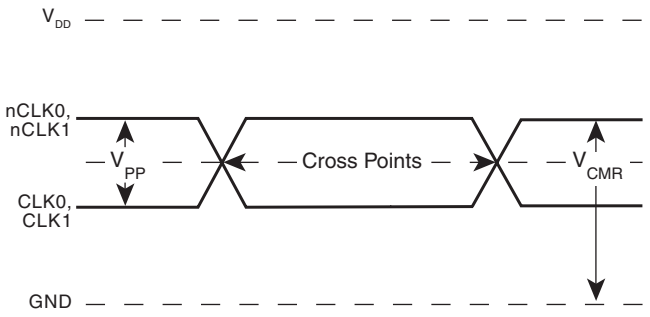
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 700MHz	3.1	3.4	3.7	ns
*t*sk(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-100	25	150	ps
*t*sk(o)	Output Skew; NOTE 3, 5				35	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				30	ps
*t*jit(θ)	Phase Jitter; NOTE 4, 5, 6				±52	ps
odc	Output Duty Cycle		46	50	54	%
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time; NOTE 7		200		700	ps

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Characterized at VCO frequency of 622MHz.
NOTE 7: Measured from the 20% to 80% points. Guaranteed by characterization. Not production tested.

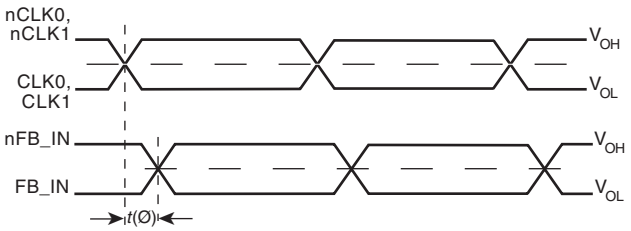
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL

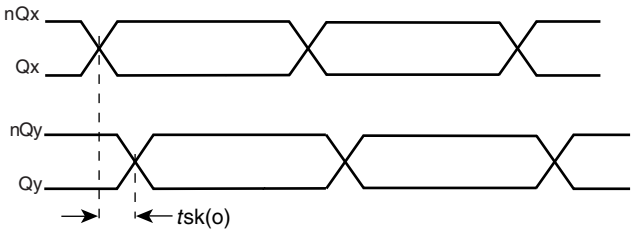


$t_{jit}(Ø) = \left| t(Ø) - t(Ø)_{mean} \right|$ = Phase Jitter

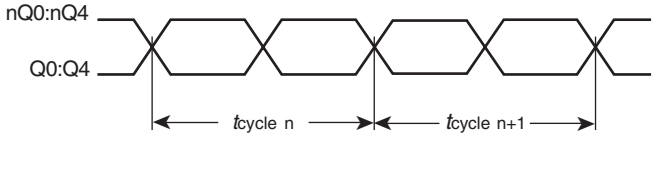
$t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

PHASE JITTER AND STATIC PHASE OFFSET



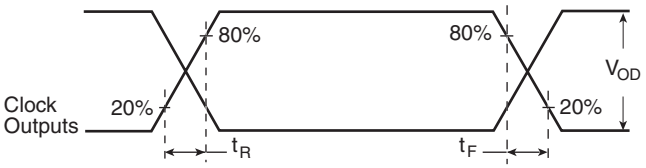
OUTPUT SKEW



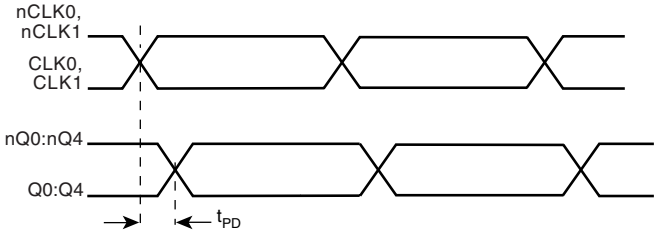
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

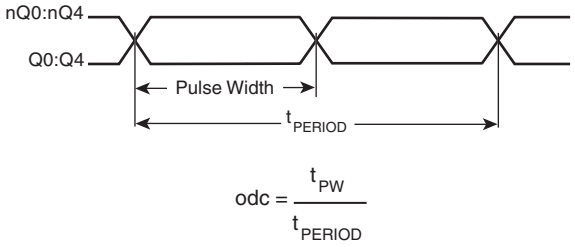
CYLE-TO-CYCLE JITTER



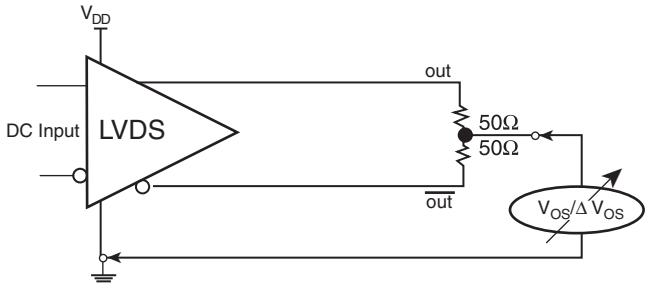
OUTPUT RISE/FALL TIME



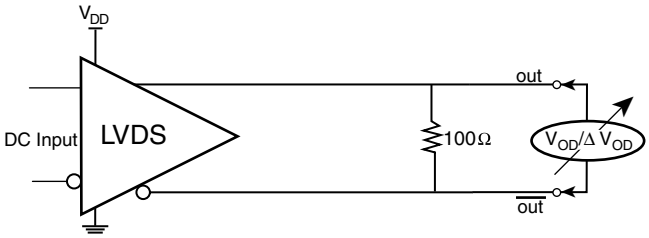
PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

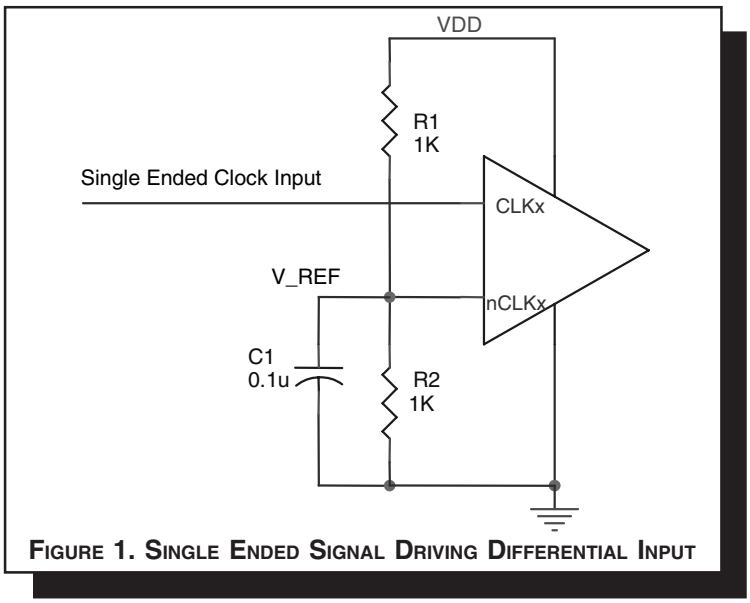


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 2.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

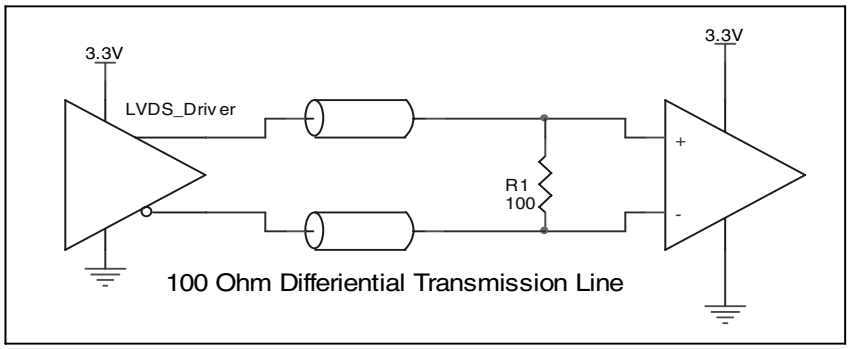


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8745B provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} pin.

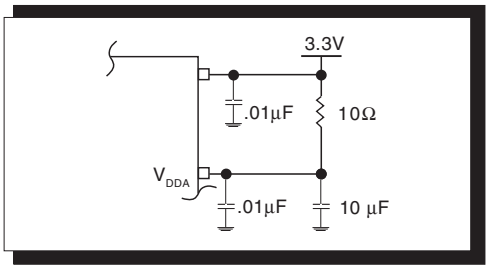


FIGURE 3. POWER SUPPLY FILTERING

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

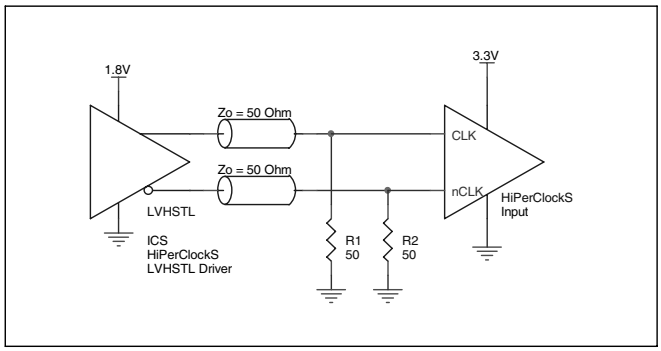


FIGURE 4A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

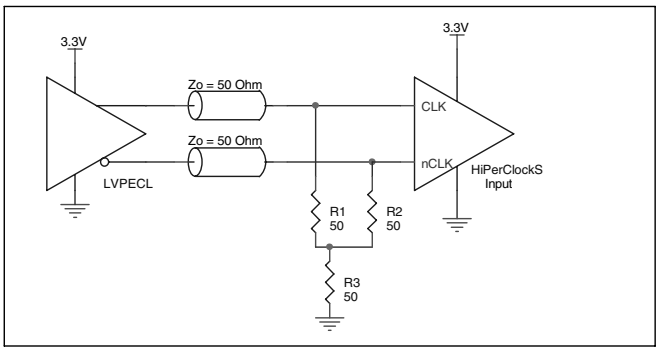


FIGURE 4B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

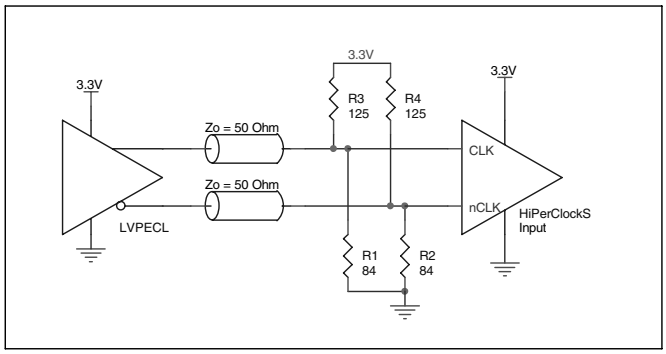


FIGURE 4C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

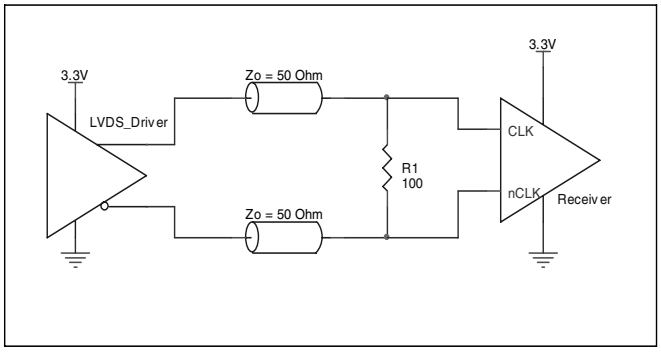


FIGURE 4D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

LAYOUT GUIDELINE

The schematic of the ICS8745B layout example is shown in *Figure 5A.* The ICS8745B recommended PCB board layout for this example is shown in *Figure 5B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

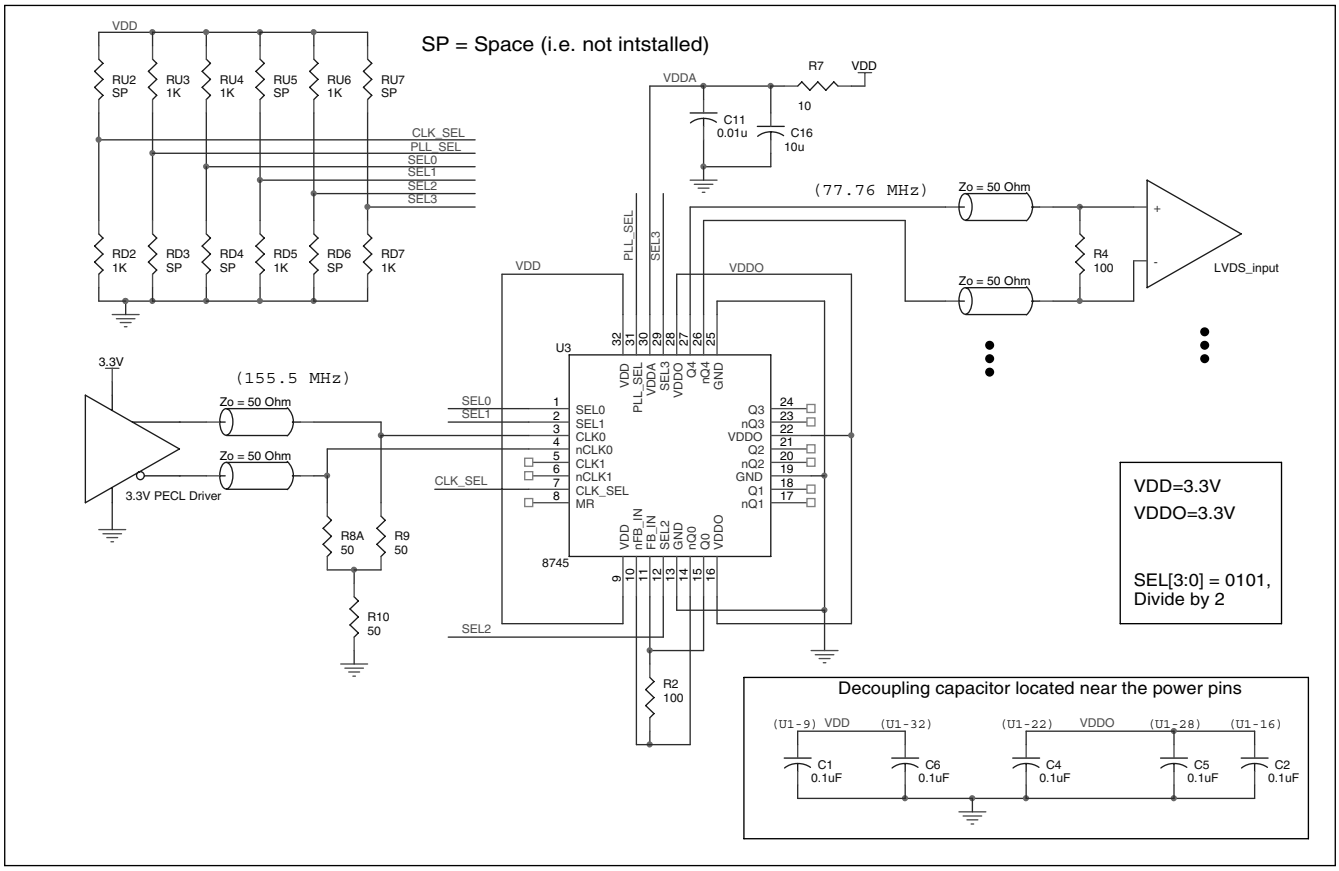


FIGURE 5A. ICS8745B LVDS ZERO DELAY BUFFER SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C1, C6, C2, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

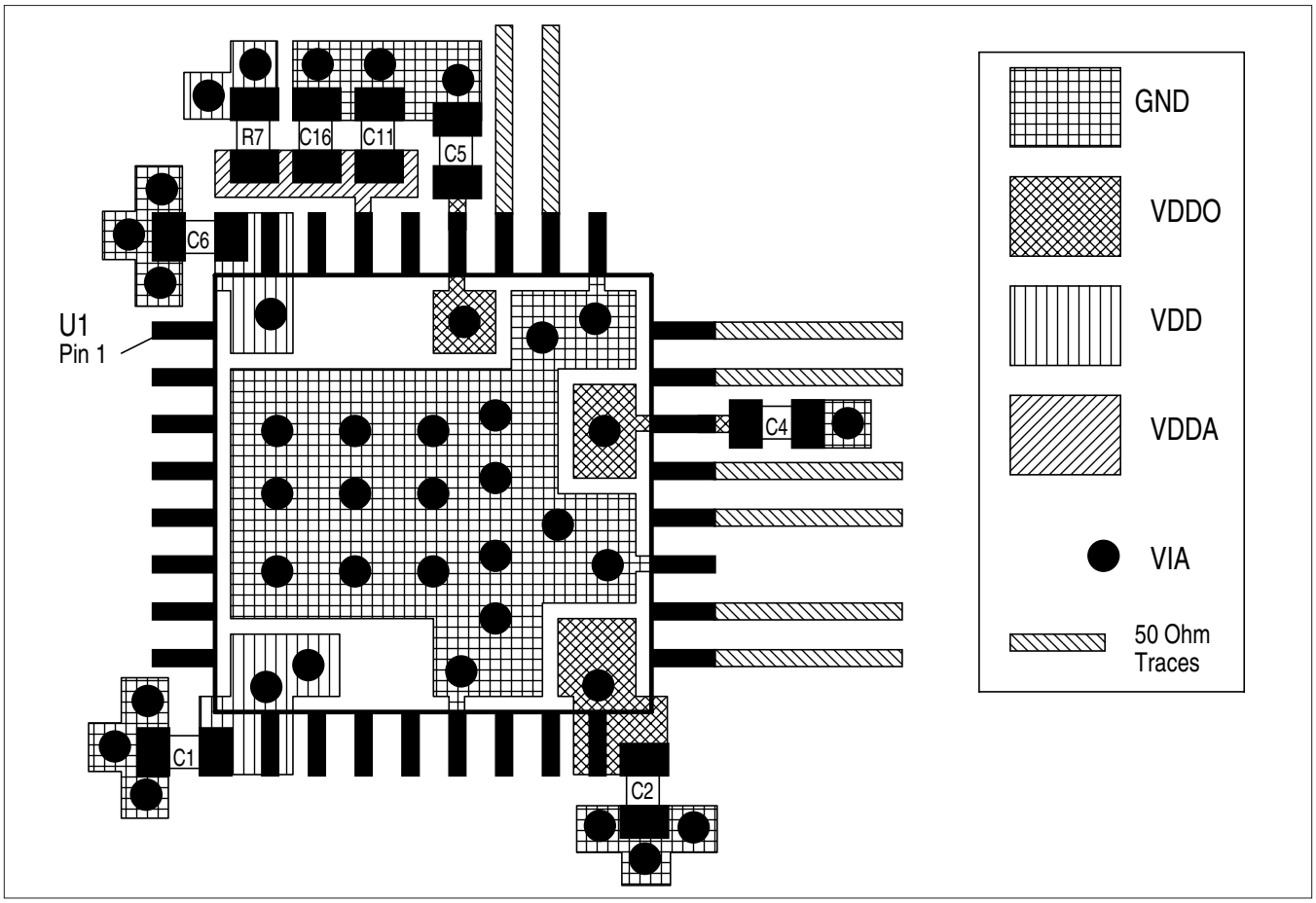


FIGURE 5B. PCB BOARD LAYOUT FOR ICS8745B

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8745B is: 2772

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

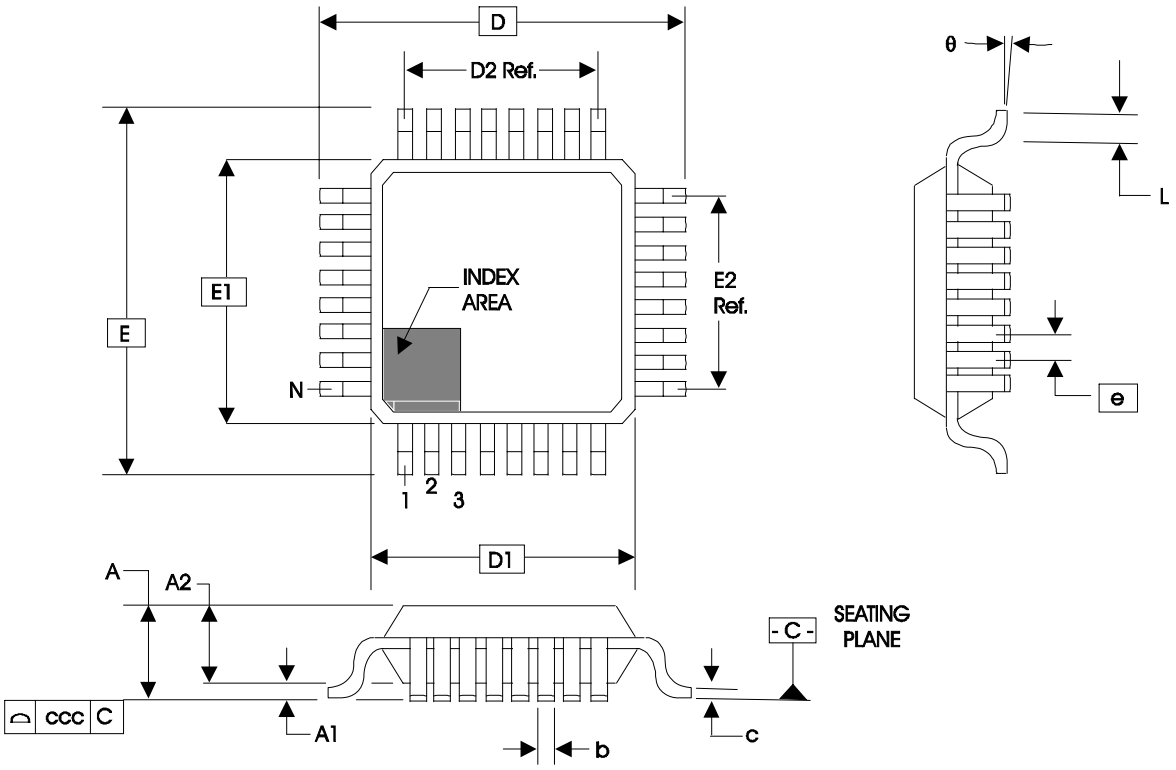


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8745BY	ICS8745BY	32 Lead LQFP	tray	0°C to 70°C
ICS8745BYT	ICS8745BY	32 Lead LQFP	1000 tape & reel	0°C to 70°C
ICS8745BYLF	ICS8745BYLF	32 Lead "Lead-Free" LQFP	tray	0°C to 70°C
ICS8745BYLFT	ICS8745BYLF	32 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4D	5	LVDS DC Characteristics Table - modified V_{OS} 0.90V min. to 1.05V min, 1.15V typical to 1.2V typical, and 1.4V max. to 1.35V max.	3/17/04
B	T9	1 14	Added Lead-Free bullet. Ordering Information Table - added Lead-Free part.	12/2/04
B	T9	1 14	Features Section - delete bullet, "Industrial temperature available upon request." Ordering Information Table - added Lead-Free note.	3/18/05