



Frequency Generator & Integrated Buffers for PENTIUM™

General Description

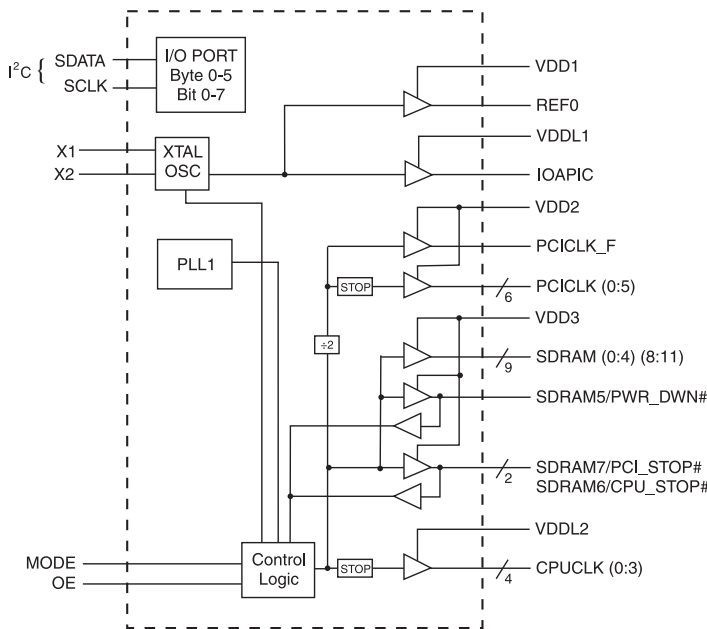
The ICS9148-11 generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. An output enable pin is provided for testability. MODE allows power management functions: CPU_STOP#, PCI_STOP# & PWR_DWN#.

High drive BCLK outputs typically provide greater than 1V/ns slew rate into 30 pF loads. PCLK outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

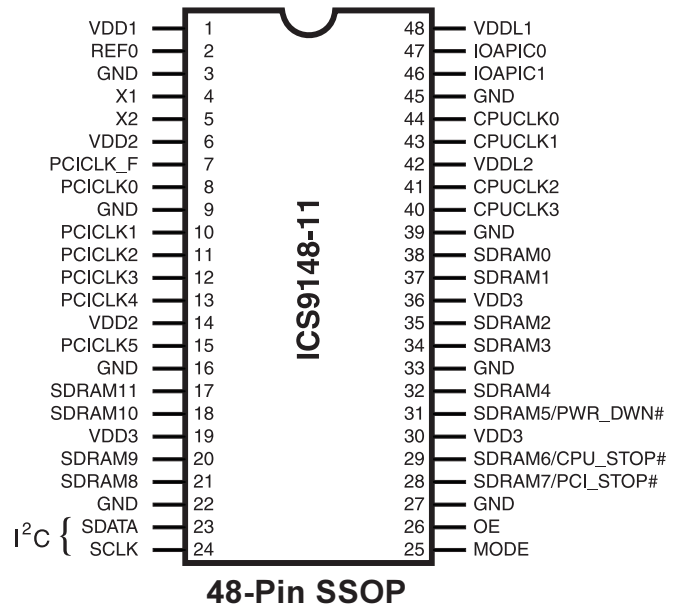
Features

- Generates four processor, six bus, one 14.318MHz and 12 SDRAM clocks.
- Synchronous clocks skew matched to 250ps window on CPU, SDRAM and 500ps window on BUS clocks.
- CPUCLKs to BUS clocks skew 1-4 ns (CPU early)
- Test clock mode eases system design
- Custom configurations available
- VDD(1:3) - 3.3V ±10% (inputs 5V tolerant w/series R)
- VDDL(1:2) - 2.5V or 3.3V ±5%
- PC serial configuration interface
- Power Management Control Input pins
- 48-pin SSOP package

Block Diagram



Pin Configuration



Functionality

| OE | CPUCLK, SDRAM (MHz) | X1, REF (MHz) | PCICLK (MHz) |
|----|---------------------|---------------|--------------|
| 0 | High-Z | High-Z | High-Z |
| 1 | 66.6 | 14.318 | 33.3 |

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Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|------------------------------------|--------------------|------|--|
| 2 | REF0 | OUT | 14.318 MHz reference clock outputs. |
| 3, 9, 16, 22, 27, 33, 39, 45 | GND | PWR | Ground. |
| 4 | X1 | IN | XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2 |
| 5 | X2 | OUT | XTAL_OUT Crystal output, has internal load cap 33pF |
| 25 | MODE | IN | Mode select pin for enabling power management features. |
| 7 | PCLK_F | OUT | Free running BUS clock during PCI_STOP# = 0. |
| 8, 10, 11, 12, 13, 15 | PCICLK (0:5) | OUT | BUS clock outputs. |
| 26 | OE | IN | Logic input for output enable, tristates all outputs when low. |
| 23 | SDATA | IN | Serial data in for serial config port. |
| 24 | SCLK | IN | Clock input for serial config port. |
| 1, 6, 14, 19, 30, 36, | VDD1, VDD2, VDD3 | PWR | Nominal 3.3V power supply, see power groups for function. |
| 17, 18, 20, 21, 32, 34, 35, 37, 38 | SDRAM (0:4) (8:11) | OUT | SDRAM clocks 66.6MHz. |
| 42, 48 | VDDL2, VDDL1 | PWR | CPU and IOAPIC clock power supply, either 2.5 or 3.3V nominal |
| 40, 41, 43, 44 | CPUCLK (0:3) | OUT | CPU output clocks, powered by VDDL2 (66.6 MHz) |
| 46, 47 | IOAPIC (0:1) | OUT | IOAPIC clock output, (14.318 MHz) powered by VDDL1 |
| 28 | SDRAM7 | OUT | SDRAM clock 66.6 MHz selected |
| | PCI_STOP# | IN | Halts PCICLK (0:5) at logic "0" level when low |
| 29 | SDRAM6 | OUT | SDRAM clock 66.6 MHz selected |
| | CPU_STOP# | IN | Halts CPUCLK clocks at logic "0" level when low |
| 31 | SDRAM5 | OUT | SDRAM clock 66.6 MHz selected |
| | PWR_DWN# | IN | Powers down chip, active low |

Power Groups

VDD1 = REF0, X1, X2

VDD2 = PCICLK_F, PCICLK (0:5)

VDD3 = SDRAM(0:4) (8:11) SDRAM5/PWR_DWN#,

SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#, supply for PLL Core.

VDDL1 = IOAPIC (0:1)

VDDL2 = CPUCLK (0:3)



Power-On Conditions

| MODE | PIN # | DESCRIPTION | FUNCTION |
|-----------------------|--|--|--|
| 1 | 44, 43, 41, 40 | CPUCLKs | 66.6 MHz - w/serial config enable/disable |
| | 38, 37, 35, 34, 32, 31, 21, 20, 18, 17, 29, 28 | SDRAM | 66.6 MHz - All SDRAM outputs |
| | 8, 10, 11, 12, 14, 15, 7 | PCICLKs | 33.3 MHz - w/serial config enable/disable |
| 0 | 28 | PCI_STOP# | Power Management, PCI (0:5) Clocks Stopped when low |
| | 29 | CPU_STOP# | Power Management, CPU (0:3) Clocks Stopped when low |
| | 31 | SDRAM/PWR_DWN# | Used as PWR_DWN# when low |
| | 7 | PCICLK_F | 33.3 MHz - 33.3 MHz - PCI Clock Free running for Power Management |
| | 44, 43, 41, 40 | CPUCLKs | 66.6 MHz - CPU Clocks w/external Stop Control and serial config individual enable/disable. |
| | 38, 37, 35, 34, 32, 21, 20, 18, 17 | SDRAM | 66.6 MHz - SDRAM Clocks w/serial config individual enable/disable. |
| 8, 10, 11, 12, 14, 15 | PCICLKs | 33.3 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable. | |

Example:

- a) if MODE = 1, pins 28, 29 and 31 are configured as SDRAM7, SDRAM6 and SDRAM5 respectively.
- b) if MODE = 0, pins 28, 29 and 31 are configured as PCI_STOP#, CPU_STOP# and PWR_DWN# respectively.

Power-On Default Conditions

At power-up and before device programming, all clocks will default to an enabled and “on” condition. The frequencies that are then produced are on the FS and MODE pin as shown in the table below.

| CLOCK | DEFAULT CONDITION AT POWER-UP |
|--------------|-------------------------------|
| REF 0 | 14.31818 MHz |
| IOAPIC (0:1) | 14.31818 MHz |



Technical Pin Function Descriptions

VDD(1,2,3)

This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, 48/24MHzA/B and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2

This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND

This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1

This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. With a nominal value of 33pF no external load cap is needed for a $C_L=17$ to 18pF crystal.

X2

This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor nominally 33pF.

CPUCLK(0:3)

These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

SDRAM(0:11)

These Output Clocks are used to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts.

IOAPIC(0:1)

This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz). Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF0

The REF Output is a fixed frequency Clock that runs at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F

This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#.

PCICLK(0:5)

These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

MODE

This Input pin is used to select the Input function of the I/O pins. An active Low will place the I/O pins in the Input mode and enable those stop clock functions.

PWR_DWN#

This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms. The I²C inputs will be Tri-States and the device will retain all programming information. This input pin only valid when MODE=0 (Power Management Mode)

CPU_STOP#

This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin only valid when MODE=0 (Power Management Mode)

PCI_STOP#

This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin only valid when MODE=0 (Power Management Mode)

I²C

The SDATA and SCLOCK Inputs are used to program the device. The clock generator is a slave-receiver device in the I²C protocol. It will allow read-back of the registers. See configuration map for register functions. The I²C specification in Philips I²C Peripherals Data Handbook (1996) should be followed.

OE

Output Enable tristates the outputs when held low. This pin will override the I²C Byte 0 function, so that the outputs will be tristated when the OE is low regardless of the I²C defined function. When OE is high, the I²C function is in active control.



General I²C serial interface information

- A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

| | | | | | |
|----------------------------------|-----|-----------------------------|-----|---------------------------|-----|
| Clock Generator Address (7 bits) | ACK | + 8 bits dummy command code | ACK | + 8 bits dummy Byte count | ACK |
| A(6:0) & R/W# | | | | | |
| D2(H) | | | | | |

Then Byte 0, 1, 2, etc in sequence until STOP.

- B. The clock generator is a slave/receiver I²C component. It can "read back "(in Philips I²C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

| | | | | | |
|----------------------------------|-----|--------|-----|--------|-----|
| Clock Generator Address (7 bits) | ACK | Byte 0 | ACK | Byte 1 | ACK |
| A(6:0) & R/W# | | | | | |
| D3(H) | | | | | |

Byte 0, 1, 2, etc in sequence until STOP.

- C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)
- D. The input is operating at 3.3V logic levels.
- E. The data byte format is 8 bit bytes.
- F. To simplify the clock generator I²C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- G. In the power down mode (PWR_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.
- H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state)

Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (Default=0)

| BIT | PIN# | DESCRIPTION | PWD |
|-------|------|---|-----|
| Bit 7 | - | Reserved | 0 |
| Bit 6 | - | Must be 0 for normal operation | 0 |
| Bit 5 | - | Must be 0 for normal operation | 0 |
| | | In Spread Spectrum, Controls type (0=centered, 1=down spread) | 0 |
| Bit 4 | - | Must be 0 for normal operation | 0 |
| | | In Spread Spectrum, Controls Spreading (0=1.8%, 1=0.6%) | 0 |
| Bit 3 | - | Reserved | 0 |
| Bit 2 | - | Reserved | 0 |
| Bit 1 | - | Bit1 | 0 |
| Bit 0 | | Bit0 | |
| | | 1 - Tri-State | |
| | | 0 - Spread Spectrum Enable | |
| | | 0 - Testmode | 0 |
| | | 0 - Normal operation | 0 |

Note: PWD = Power-Up Default



Select Functions

| FUNCTION DESCRIPTION | OUTPUTS | | | | |
|----------------------|---------------------|---------------------|---------------------|-------------------|-------------------|
| | CPU | PCI, PCI_F | SDRAM | REF | IOAPIC |
| Tri - State | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| Test Mode | TCLK/2 ¹ | TCLK/4 ¹ | TCLK/2 ¹ | TCLK ¹ | TCLK ¹ |

Notes:

1. REF is a test clock on the X1 inputs during test mode.

Byte 1: CPU Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|---------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | 40 | 1 | CPUCLK3 (Act/Inact) |
| Bit 2 | 41 | 1 | CPUCLK2 (Act/Inact) |
| Bit 1 | 43 | 1 | CPUCLK1 (Act/Inact) |
| Bit 0 | 44 | 1 | CPUCLK0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|----------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | 7 | 1 | PCICLK_F (Act/Inact) |
| Bit 5 | 15 | 1 | PCICLK5 (Act/Inact) |
| Bit 4 | 13 | 1 | PCICLK4 (Act/Inact) |
| Bit 3 | 12 | 1 | PCICLK3 (Act/Inact) |
| Bit 2 | 11 | 1 | PCICLK2 (Act/Inact) |
| Bit 1 | 10 | 1 | PCICLK1 (Act/Inact) |
| Bit 0 | 8 | 1 | PCICLK0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|------------------------------------|
| Bit 7 | 28 | 1 | SDRAM7 (Act/Inact) Desktop only |
| Bit 6 | 29 | 1 | SDRAM6 (Act/Inact) Desktop only |
| Bit 5 | 31 | 1 | SDRAM5 (Act/Inact) Desktop only |
| Bit 4 | 32 | 1 | SDRAM4 (Act/Inact) |
| Bit 3 | 34 | 1 | SDRAM3 (Act/Inact) |
| Bit 2 | 35 | 1 | SDRAM2 (Act/Inact) |
| Bit 1 | 37 | 1 | SDRAM1 (Act/Inact) |
| Bit 0 | 38 | 1 | SDRAM0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|---------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | 17 | 1 | SDRAM11 (Act/Inact) |
| Bit 2 | 18 | 1 | SDRAM10 (Act/Inact) |
| Bit 1 | 20 | 1 | SDRAM9 (Act/Inact) |
| Bit 0 | 21 | 1 | SDRAM8 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default



Byte 5: Peripheral Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|---------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | 46 | 1 | IOAPIC1 (Act/Inact) |
| Bit 4 | 47 | 1 | IOAPIC0 (Act/Inact) |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | - | 1 | Reserved |
| Bit 0 | 2 | 1 | REF0(Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

Byte 6: Optional Register for Future

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|-------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | - | 1 | Reserved |
| Bit 0 | - | 1 | Reserved |

Notes:

1. Byte 6 is reserved by Integrated Circuit Systems for future applications.

Power Management

Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK | PCICLK | Other Clocks, SDRAM, REF, IOAPICs | Crystal | VCOs |
|-----------|-----------|----------|----------|----------|--|---------|---------|
| X | X | 0 | Low | Low | Stopped | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running |
| 0 | 1 | 1 | Low | 33.3 MHz | Running | Running | Running |
| 1 | 0 | 1 | 66.6 MHz | Low | Running | Running | Running |
| 1 | 1 | 1 | 66.6 MHz | 33.3 MHz | Running | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9148-11 Power Management Requirements

| SIGNAL | SIGNAL STATE | Latency No. of rising edges of free running PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PCI_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PWR_DWN# | 1 (Normal Operation) ³ | 3mS |
| | 0 (Power Down) ⁴ | 2max |

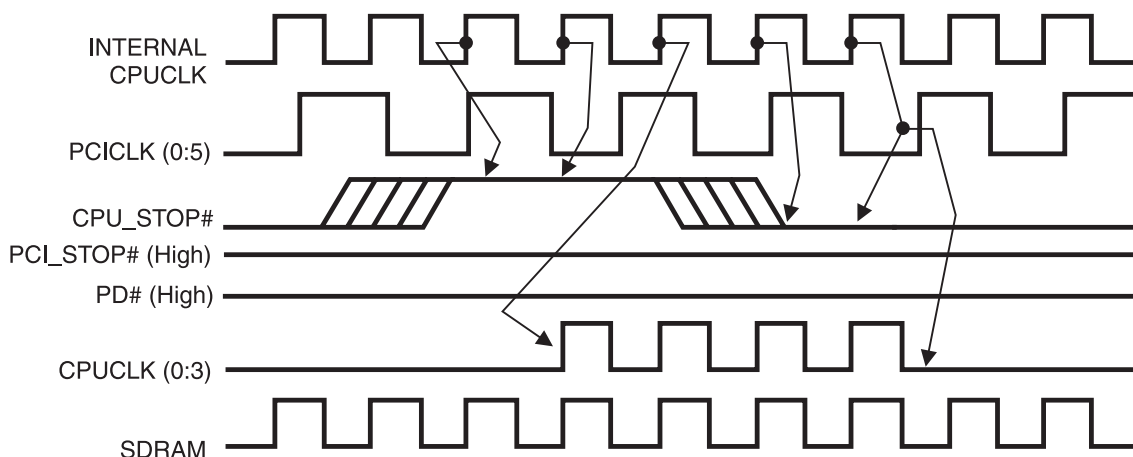
Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, SDRAM, PCICLK only.
The REF and IOAPIC will be stopped independent of these.



CPU_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the ICS9148-11. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



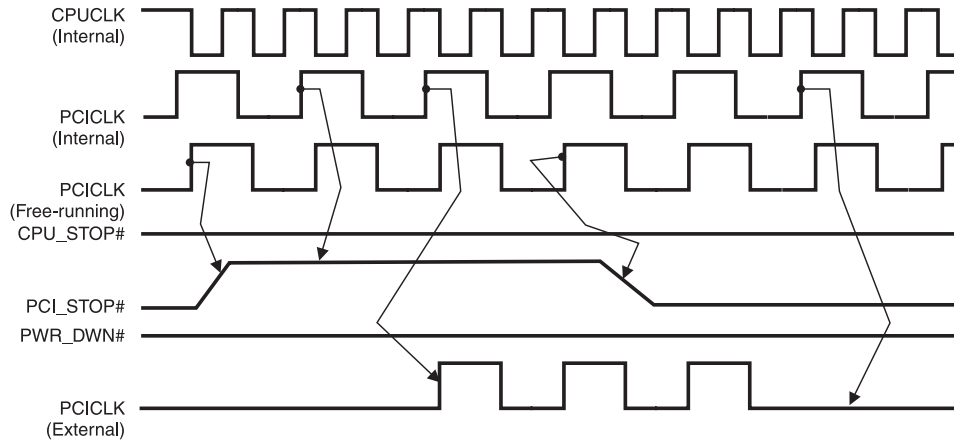
Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9148-11.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the ICS9148-11. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the ICS9148-11 internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

(Drawing shown on next page.)

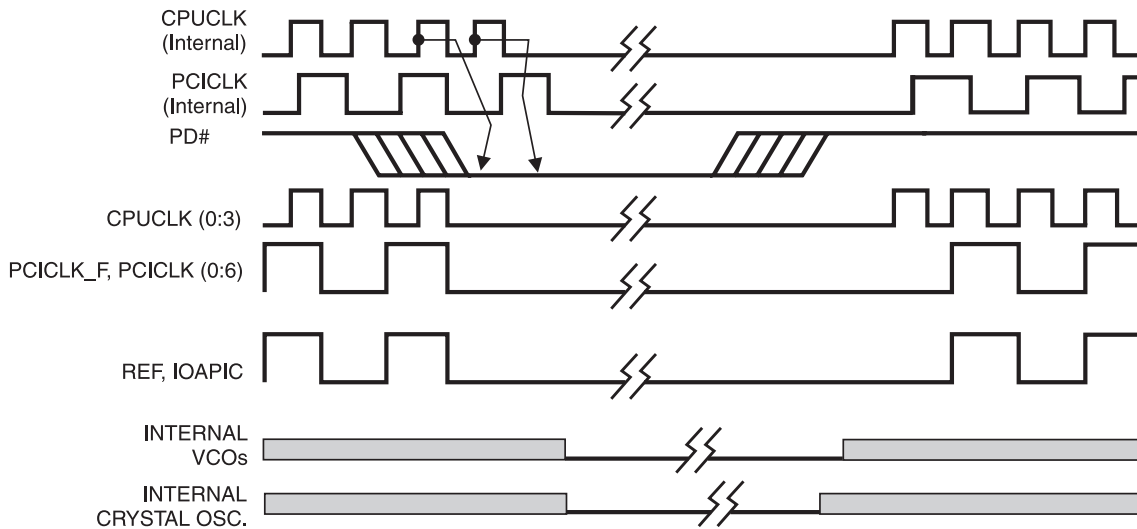


Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
- 2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
- 3. All other clocks continue to run undisturbed.
- 4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the ICS9148-11 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3 mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
- 2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
- 3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------------|
| Supply Voltage | 7.0 V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-------------------------|---|----------------------|------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | μA |
| Operating Supply Current | I _{DD3.3OP} | CL = 0 pF; Select @ 66M | | 75 | 95 | mA |
| Outputs Disabled Supply Current | I _{DD3.3OE} | CL = 0 pF; With input address to V _{DD} or GND | | 18 | 25 | mA |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Settling Time ¹ | T _s | From 1st crossing to 1% target Freq. | | 5 | | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | 5 | 3 | ms |
| Skew ¹ | T _{CPU-SDRAM2} | V _T = 1.5 V | | 200 | 500 | ps |
| | T _{CPU-PCI2} | V _T = 1.5 V | 1 | 2 | 4 | ns |
| | T _{REF-IOAPIC} | V _T = 1.5 V | | 900 | | ps |



Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|---|-----|-----|-----|-------|
| Operating Supply Current | IDD2.5OP | CL = 0 pF; Select @ 66M | 6 | 8 | 9.5 | mA |
| Skew ¹ | T _{CPU-SDRAM2} | V _T = 1.5 V; V _{TL} = 1.25 V; SDRAM Leads | | 250 | 500 | ps |
| | T _{CPU-PCI2} | V _T = 1.5 V; V _{TL} = 1.25 V; CPU Leads | 1 | 2 | 4 | ns |
| | T _{REF-IOAPIC} | V _T = 1.5 V; V _{TL} = 1.25 V; CPU Leads | | 860 | | ps |

¹Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|--------------------------------------|--|------|-----|------|-------|
| Output Impedance | R _{DSP2B} ¹ | V _O = V _{DD} *(0.5) | 15 | | 45 | Ω |
| Output Impedance | R _{DSN2B} ¹ | V _O = V _{DD} *(0.5) | 15 | | 45 | Ω |
| Output High Voltage | V _{OH2B} | I _{OH} = -12.0 mA | 2 | 2.6 | | V |
| Output Low Voltage | V _{OL2B} | I _{OL} = 12 mA | | 0.3 | 0.4 | V |
| Output High Current | I _{OH2B} | V _{OH} = 1.7 V | | -25 | -16 | mA |
| Output Low Current | I _{OL2B} | V _{OL} = 0.7 V | 19 | 26 | | mA |
| Rise Time | t _{r2B} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.0 V | | 1.7 | 2 | ns |
| Fall Time | t _{f2B} ¹ | V _{OH} = 2.0 V, V _{OL} = 0.4 V | | 1.5 | 2 | ns |
| Duty Cycle | d _{t2B} ¹ | V _T = 1.25 V | 45 | 50 | 55 | % |
| Skew | t _{sk2B} ¹ | V _T = 1.25 V | | 60 | 250 | ps |
| Jitter | t _{jcyc-cyc2B} ¹ | V _T = 1.25 V | | 150 | 250 | ps |
| | t _{j1s2B} ¹ | V _T = 1.25 V | | 30 | 150 | ps |
| | t _{jabs2B} ¹ | V _T = 1.25 V | -250 | 80 | +250 | ps |

¹Guarenteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|-------------------------------------|--|-------|------|------|-------|
| Output Impedance | R _{DSP4B} ¹ | V _O = V _{DD} *(0.5) | 10 | | 30 | Ω |
| Output Impedance | R _{DSN4B} ¹ | V _O = V _{DD} *(0.5) | 10 | | 30 | Ω |
| Output High Voltage | V _{OH4B} | I _{OH} = -18 mA | 2 | 2.4 | | V |
| Output Low Voltage | V _{OL4B} | I _{OL} = 18 mA | | 0.45 | 0.5 | V |
| Output High Current | I _{OH4B} | V _{OH} = 1.7 V | | -25 | -16 | mA |
| Output Low Current | I _{OL4B} | V _{OL} = 0.7 V | 19 | 26 | | mA |
| Rise Time | t _{r4B} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.0 V | | 1.4 | 1.6 | ns |
| Fall Time | t _{f4B} ¹ | V _{OH} = 2.0 V, V _{OL} = 0.4 V | | 1.2 | 1.6 | ns |
| Duty Cycle | d _{t4B} ¹ | V _T = 1.25 V | 40 | 54 | 60 | % |
| Jitter | t _{jyc-cyc4B} ¹ | V _T = 1.25 V | | 1400 | | ps |
| | t _{j1s4B} ¹ | V _T = 1.25 V | | 300 | 400 | ps |
| | t _{jabs4B} ¹ | V _T = 1.25 V | -1000 | 800 | 1000 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0 - 70°C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 45 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|-------------------------------------|--|-------|------|------|-------|
| Output Impedance | R _{DSP7} | V _O = V _{DD} *(0.5) | 10 | | 24 | Ω |
| Output Impedance | R _{DSN7} | V _O = V _{DD} *(0.5) | 10 | | 24 | Ω |
| Output High Voltage | V _{OH7} | I _{OH} = -30 mA | 2.6 | 2.75 | | V |
| Output Low Voltage | V _{OL7} | I _{OL} = 23 mA | | 0.3 | 0.4 | V |
| Output High Current | I _{OH7} | V _{OH} = 2.0 V | | -62 | -54 | mA |
| Output Low Current | I _{OL7} | V _{OL} = 0.8 V | 42 | 50 | | mA |
| Rise Time | T _{r7} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 0.9 | 2 | ns |
| Fall Time | T _{f7} ¹ | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 0.9 | 2 | ns |
| Duty Cycle | D _{t7} ¹ | V _T = 1.5 V | 40 | 54 | 60 | % |
| Jitter | t _{jyc-cyc7B} ¹ | V _T = 1.25 V | | 1400 | | ps |
| | t _{j1s7B} ¹ | V _T = 1.25 V | | 350 | | ps |
| | t _{jabs7B} ¹ | V _T = 1.25 V | -1000 | 900 | 1000 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

TA = 0 - 70C; VDD = VDDL = 3.3 V +/-5%; CL = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|---------------------|--------------------------|------|------|-----|-------|
| Output Impedance | RDSP1 ¹ | VO = VDD*(0.5) | 12 | | 55 | Ω |
| Output Impedance | RDSN1 ¹ | VO = VDD*(0.5) | 12 | | 55 | Ω |
| Output High Voltage | VOH1 | IOH = -11 mA | 2.6 | 3.1 | | V |
| Output Low Voltage | VOL1 | IOL = 9.4 mA | | 0.15 | 0.4 | V |
| Output High Current | IOH1 | VOH = 2.0 V | | -65 | -54 | mA |
| Output Low Current | IOL1 | VOL = 0.8 V | 40 | 54 | | mA |
| Rise Time | tr1 ¹ | VOL = 0.4 V, VOH = 2.4 V | | 1.5 | 2 | ns |
| Fall Time | tf1 ¹ | VOH = 2.4 V, VOL = 0.4 V | | 1.4 | 2 | ns |
| Duty Cycle | dt1 ¹ | VT = 1.5 V | 45 | 50 | 55 | % |
| Skew | tsk1 ¹ | VT = 1.5 V | | 200 | 500 | ps |
| Jitter | tj1s1 ¹ | VT = 1.5 V | | 10 | 150 | ps |
| | tjabs1 ¹ | VT = 1.5 V | -250 | 65 | 250 | ps |

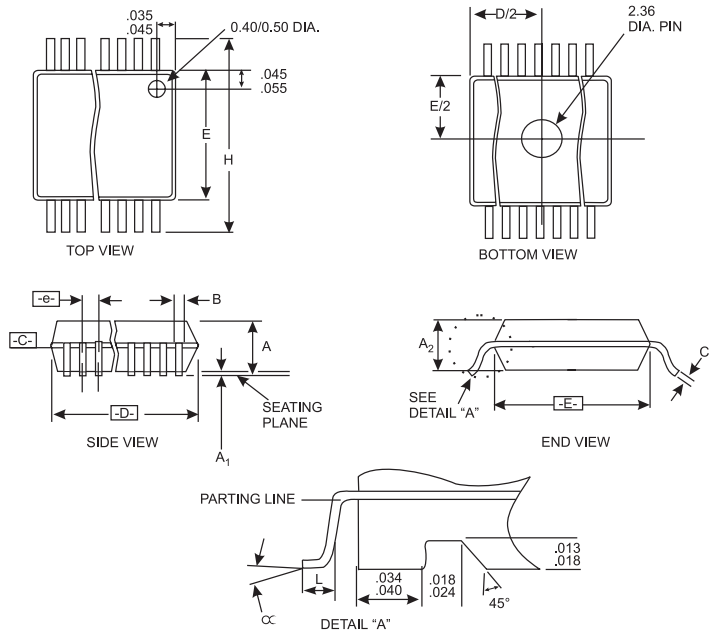
¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

TA = 0 - 70C; VDD = VDDL = 3.3 V +/-5%; CL = 20 - 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|---------------------|--------------------------|------|-----|-----|-------|
| Output Impedance | RDSP3 ¹ | VO = VDD*(0.5) | 10 | | 24 | Ω |
| Output Impedance | RDSN3 ¹ | VO = VDD*(0.5) | 10 | | 24 | Ω |
| Output High Voltage | VOH3 | IOH = -30 mA | 2.6 | 2.8 | | V |
| Output Low Voltage | VOL3 | IOL = 23 mA | | 0.3 | 0.4 | V |
| Output High Current | IOH3 | VOH = 2.0 V | | -67 | -54 | mA |
| Output Low Current | IOL3 | VOL = 0.8 V | 40 | 55 | | mA |
| Rise Time | Tr3 ¹ | VOL = 0.4 V, VOH = 2.4 V | | 1.5 | 2 | ns |
| Fall Time | Tf3 ¹ | VOH = 2.4 V, VOL = 0.4 V | | 1.4 | 2 | ns |
| Duty Cycle | Dt3 ¹ | VT = 1.5 V | 45 | 50 | 55 | % |
| Skew | Tsk3 ¹ | VT = 1.5 V | | 200 | 500 | ps |
| Jitter | Tj1s3 ¹ | VT = 1.5 V | | 50 | 150 | ps |
| | Tjabs3 ¹ | VT = 1.5 V | -250 | 100 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



SSOP Package

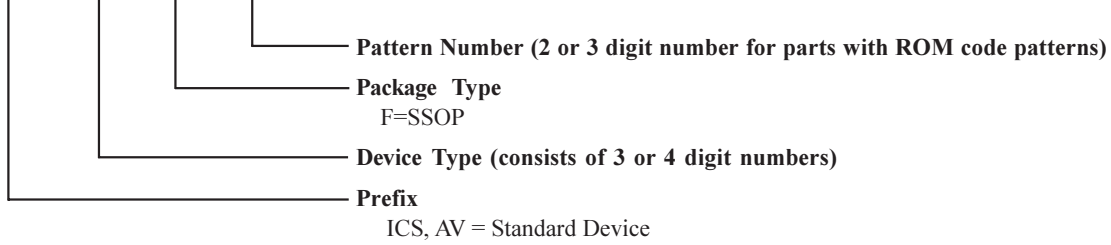
| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|------------|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .101 | .110 | AC | .620 | .625 | .630 | 48 |
| A1 | .008 | .012 | .016 | | | | | |
| A2 | .088 | .090 | .092 | | | | | |
| B | .008 | .010 | .0135 | | | | | |
| C | .005 | - | .010 | | | | | |
| D | See Variations | | | | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | 5° | 8° | | | | | |
| X | .085 | .093 | .100 | | | | | |

Ordering Information

ICS9148F-11

Example:

ICS XXXX F - PPP



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.