Integrated Circuit Systems, Inc.

ICS9248-135

Frequency Generator & Integrated Buffers for Celeron & PII/III™& K6

Recommended Application:

Motherboard Single chip clock solution for SIS540, SIS630 Pentium II/III and K6 chipsets.

Output Features:

- 3- CPUs @ 2.5/3.3V, up to 166MHz.
- 10 - SDRAM @ 3.3V, up to 166MHz including 2 SDRAM_F's
- 7- PCI @3.3V,
- 1- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V selectable by I^2C (Default is 24MHz).
- 2- REF @3.3V, 14.318MHz.

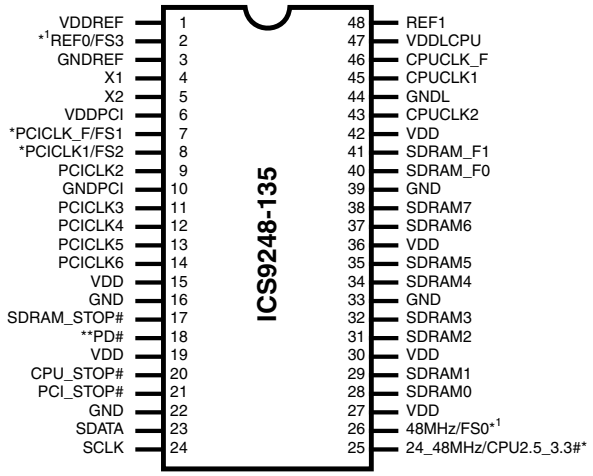
Features:

- Up to 166MHz frequency support
- Support FS0-FS3 trapping status bit for I^2C read back.
- Support power management: CPU, PCI, SDRAM stop and Power down Mode form I^2C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- FS0, FS1, FS3 must have a internal 120K pull-Down to GND.
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU - CPU: < 175ps
- SDRAM - SDRAM < 250ps
- PCI - PCI: < 500ps
- CPU - SDRAM: < 500ps
- CPU (early) - PCI: 1-4ns (typ. 2ns)

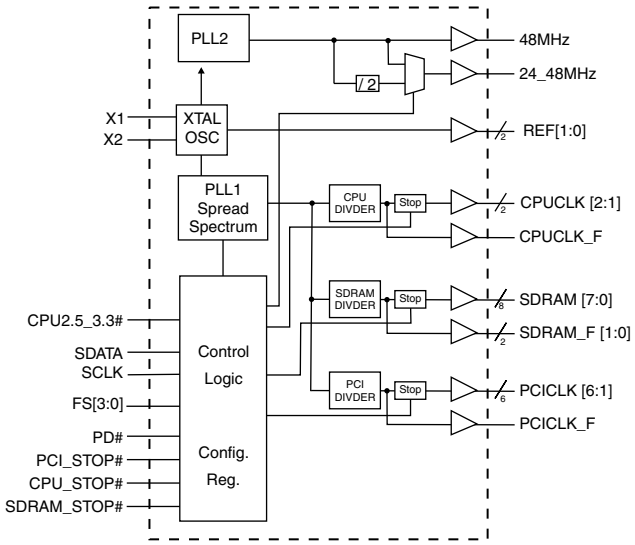
Pin Configuration



48-Pin 300mil SSOP

* These inputs have a 120K pull down to GND.
** These inputs have a 120K pullup to VDD.
1 These are double strength.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCICLK (MHz)
0	0	0	0	66.6	100.0	33.3
0	0	0	1	100.0	100.0	33.3
0	0	1	0	150.0	100.0	37.5
0	0	1	1	133.3	100.0	33.3
0	1	0	0	66.8	133.6	33.4
0	1	0	1	100.0	133.3	33.3
0	1	1	0	100.0	150.0	37.5
0	1	1	1	133.3	133.3	33.3
1	0	0	0	66.8	66.8	33.4
1	0	0	1	97.0	97.0	32.3
1	0	1	0	70.0	105.0	35.0
1	0	1	1	95.0	95.0	31.7
1	1	0	0	95.0	126.7	31.7
1	1	0	1	112.0	112.0	37.3
1	1	1	0	97.0	129.3	32.2
1	1	1	1	96.2	96.2	32.1

General Description

The **ICS9248-135** is the single chip clock solution for Desktop/Notebook designs using the SIS 540/630 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-135 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 15, 19, 27, 30, 36, 42	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output
2	REF0	OUT	14.318 MHz reference clock.
	FS3	IN	Frequency select pin.
3, 10, 16, 22, 33, 39, 44	GND	PWR	Ground pin for 3V outputs.
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, nominally 14.318MHz.
7	FS1	IN	Frequency select pin.
	PCICLK_F	OUT	Free running PCICLK clock output. Not affected by PCI_STOP#
8	FS2	IN	Frequency select pin.
	PCICLK1	OUT	PCI clock outputs.
14, 13, 12, 11, 9	PCICLK (6:2)	OUT	PCI clock outputs.
17	SDRAM_STOP#	IN	Stops all SDRAMs besides the SDRAM_F clocks at logic 0 level, when input low
18	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
20	CPU_STOP#	IN	Stops all CPUCLKs clocks at logic 0 level, when input low
21	PCI_STOP#	IN	Stops all PCICLKs clocks at logic 0 level, when input low
38, 37, 35, 34, 32, 31, 29, 28	SDRAM (7:0)	OUT	SDRAM clock outputs
23	SDATA	IN	Data input for I^2C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
25	CPU2.5_3.3#	IN	Voltage select 2.5V when high - 3.3V when low
	24_48MHz	OUT	Clock output for super I/O/USB default is 24MHz
26	FS0	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
41, 40	SDRAM_F (1:0)	OUT	Free running SDRAM clock outputs. Not affected by SDRAM_STOP#
45, 43	CPUCLK (1:2)	OUT	CPU clock outputs.
46	CPUCLK_F	OUT	Free running CPUCLK clock output. Not affected by CPU_STOP#
47	VDDLCPU	PWR	Power pin for the CPUCLKs. 2.5V
48	REF1	OUT	14.318 MHz reference clock.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description									PWD
	Bit7	Bit2	Bit6	Bit5	Bit4	CPU	SDRAM	PCI	SS	
Bit 7, 2, Bit 6:4	0	0	0	0	0	66.6	100.0	33.3	0 to-0.5%	00010 Note1
	0	0	0	0	1	100.0	100.0	33.3	0 to-0.5%	
	0	0	0	1	0	150.0	100.0	37.5	±0.25%	
	0	0	0	1	1	133.3	100.0	33.3	0 to-0.5%	
	0	0	1	0	0	66.8	133.6	33.4	0 to-0.5%	
	0	0	1	0	1	100.0	133.3	33.3	0 to-0.5%	
	0	0	1	1	0	100.0	150.0	37.5	±0.25%	
	0	0	1	1	1	133.3	133.3	33.3	0 to-0.5%	
	0	1	0	0	0	66.8	66.8	33.4	±0.25%	
	0	1	0	0	1	97.0	97.0	32.3	0 to-0.5%	
	0	1	0	1	0	70.0	105.0	35.0	±0.25%	
	0	1	0	1	1	95.0	95.0	31.7	±0.25%	
	0	1	1	0	0	95.0	126.7	31.7	±0.25%	
	0	1	1	0	1	112.0	112.0	37.3	±0.25%	
	0	1	1	1	0	97.0	129.3	32.3	0 to-0.5%	
	0	1	1	1	1	96.2	96.2	32.1	0 to-0.5%	
	1	0	0	0	0	66.8	100.2	33.4	±0.25%	
	1	0	0	0	1	100.2	100.2	33.4	±0.25%	
	1	0	0	1	0	166.0	110.7	27.7	±0.25%	
	1	0	0	1	1	100.2	133.6	33.4	±0.25%	
	1	0	1	0	0	75.0	100.0	37.5	±0.25%	
	1	0	1	0	1	83.3	125.0	31.3	±0.25%	
	1	0	1	1	0	105.0	140.0	35.0	±0.25%	
	1	0	1	1	1	133.6	133.6	33.4	±0.25%	
	1	1	0	0	0	110.3	147.0	36.8	±0.25%	
	1	1	0	0	1	115.0	153.3	38.3	±0.25%	
	1	1	0	1	0	120.0	120.0	30.0	±0.25%	
	1	1	0	1	1	138.0	138.0	34.5	±0.25%	
	1	1	1	0	0	140.0	140.0	35.0	±0.25%	
	1	1	1	0	1	145.0	145.0	36.3	±0.25%	
	1	1	1	1	0	147.5	147.5	36.9	±0.25%	
	1	1	1	1	1	160.0	160.0	26.7	±0.25%	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 7, 2, 6:4									0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled									1
Bit 0	0 - Running 1- Tristate all outputs									0

Note: PWD = Power-Up Default

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3. The I^2C readback for Bits 7, 2, 6:4 indicate the revision code.

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Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	SEL24_48# (48MHz when set to 0) (24MHz when set to 1)
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	43	1	CPUCLK2 (Act/Inact)
Bit 2	45	1	CPUCLK1 (Act/Inact)
Bit 1	46	1	CPUCLK0 (Act/Inact)
Bit 0	-	1	Reserved

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(CPU2.5_3.3#)
Bit 6	14	1	PCICLK6 (Act/Inact)
Bit 5	13	1	PCICLK5 (Act/Inact)
Bit 4	12	1	PCICLK4 (Act/Inact)
Bit 3	11	1	PCICLK3 (Act/Inact)
Bit 2	9	1	PCICLK2 (Act/Inact)
Bit 1	8	1	PCICLK1 (Act/Inact)
Bit 0	7	1	PCICLK_F (Act/Inact)

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	32	1	SDRAM3 (Act/Inact)
Bit 6	31	1	SDRAM2 (Act/Inact)
Bit 5	29	1	SDRAM1 (Act/Inact)
Bit 4	28	1	SDRAM0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	25	1	24_48MHz
Bit 6	26	1	48MHz
Bit 5	41	1	SDRAM_F1
Bit 4	40	1	SDRAM_F0
Bit 3	38	1	SDRAM7
Bit 2	37	1	SDRAM6
Bit 1	35	1	SDRAM5
Bit 0	34	1	SDRAM4

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	FS3#
Bit 4	-	1	FS2#
Bit 3	-	1	FS1#
Bit 2	-	1	FS0#
Bit 1	48	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used both to provide the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. When no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, then only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

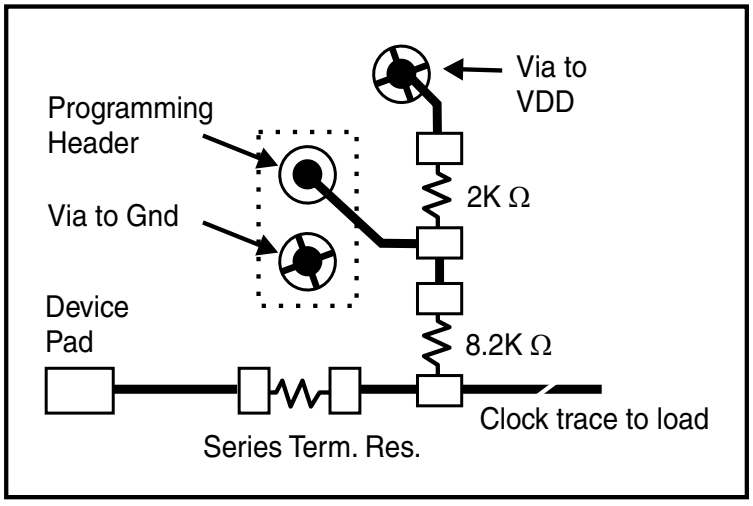
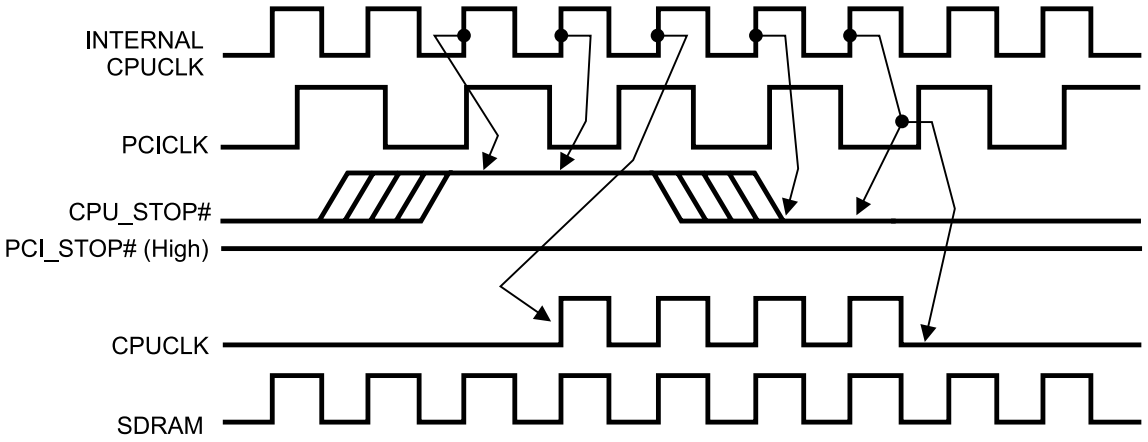


Fig. 1

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-135**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

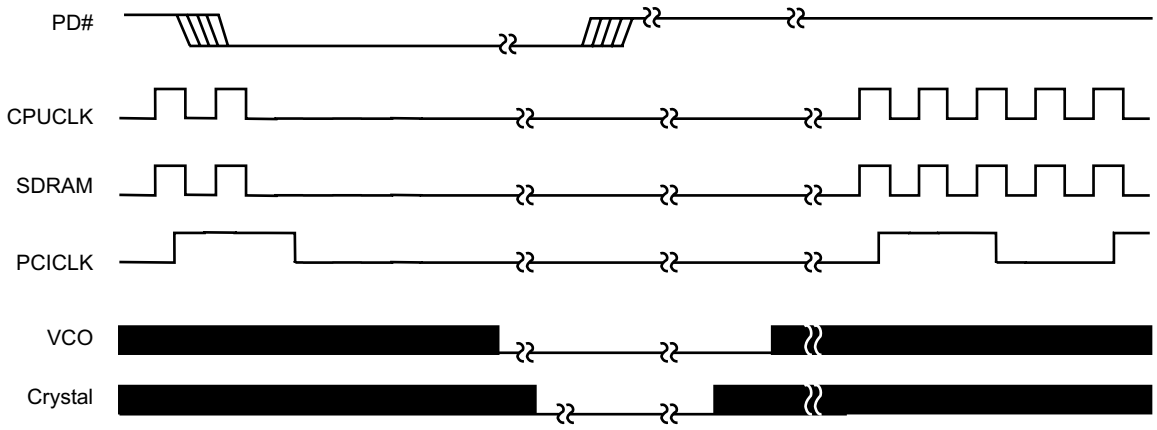


Notes:
1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-135.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

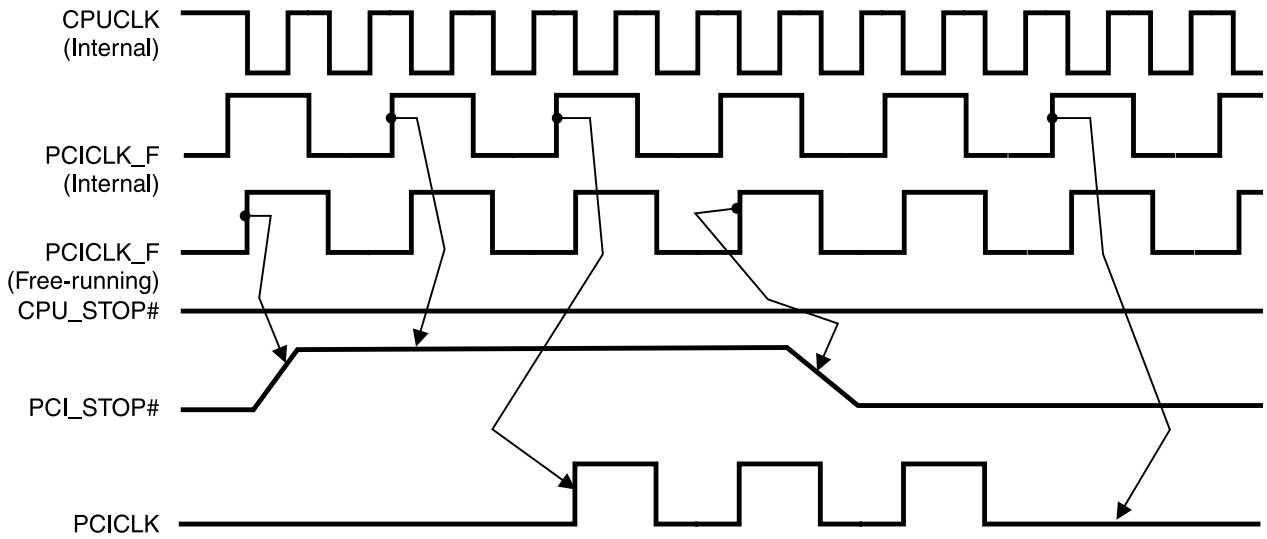
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-135 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-135**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-135** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

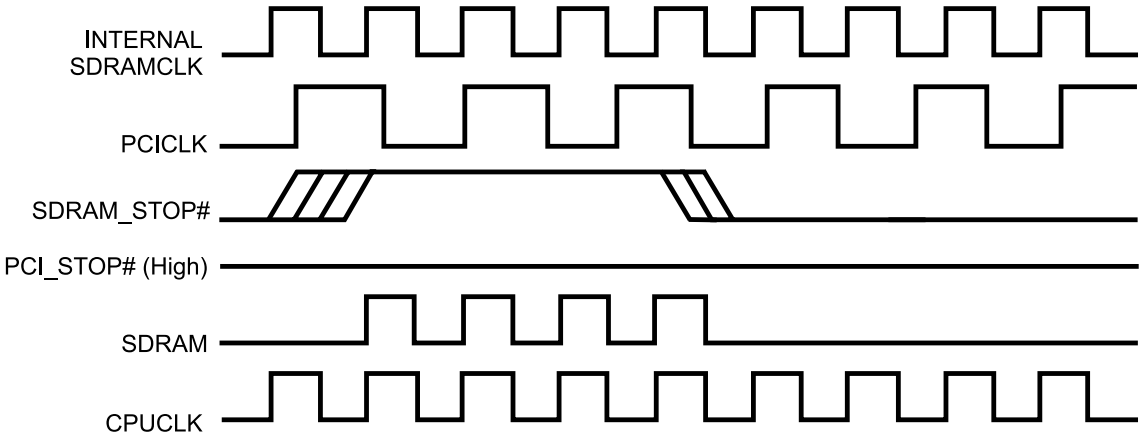


Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-135 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-135.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

SDRAM_STOP# Timing Diagram

SDRAM_STOP# is an asychronous input to the clock synthesizer. It is used to stop SDRAM clocks for low power operation. SDRAM_STOP# is synchronized to complete it's current cycle, by the **ICS9248-135**. All other clocks will continue to run while the SDRAM clocks are disabled. The SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse.



Notes:

1. All timing is referenced to the internal CPU clock.
2. SDRAM is an asynchronous input and metastable conditions may exist. This signal is synchronized to the SDRAM clocks inside the ICS9248-135.
3. All other clocks continue to run undisturbed.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz		148	180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz		150	180	mA
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz		161		mA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew	$t_{CPU-PCI}$	V_T = 1.5 V	1	2.39	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.8 MHz		6.13	30	mA
	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		9.22		mA
	$I_{DD2.5OP133}$	C_L = 0 pF; Select @ 133 MHz		11.6		mA
Skew[1]	$t_{CPU-SDRAM}$	V_T = 1.5 V; V_{TL} = 1.25 V		273	500	ps
	$t_{CPU-PCI}$	V_T = 1.5 V; V_{TL} = 1.25 V	1	2.25	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = VDDL = 3.3 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	VO=VDD*(0.5)	10	36.5	40	Ω
Output Impedance	R_{DSN2A}[1]	VO=VDD*(0.5)	10	29	40	Ω
Output High Voltage	V_{OH1a}	I_{OH} = -20.0 mA	2	2.85		V
Output Low Voltage	V_{OL1a}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH1a}	V_{OH} = 2 V		-45	-19	mA
Output Low Current	I_{OL1a}	V_{OL} = 0.8 V	22	29		mA
Rise Time	t_{r1a}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.24	2	ns
Fall Time	t_{f1a}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.6	2	ns
Duty Cycle	d_{t1a}[1]	V_T = 1.5 V	45	52.6	62	%
Skew	t_{sk1a}[1]	V_T = 1.5 V		80.8	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc1a}$[1]	V_T = 1.5 V		128	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	VO=VDD*(0.5)	10	36.5	40	Ω
Output Impedance	R_{DSN2A}[1]	VO=VDD*(0.5)	10	29	40	Ω
Output High Voltage	V_{OH1B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL1B}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH1B}	V_{OH} = 1.7 V		-39	-21	mA
Output Low Current	I_{OL1B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r1B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.03	1.6	ns
Fall Time	t_{f1B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.26	1.6	ns
Duty Cycle	d_{t1a}[1]	V_T = 1.5 V	45	51.7	55	%
Skew	t_{sk1a}[1]	V_T = 1.5 V		66.1	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc1B}$[1]	V_T = 1.25 V CPU, SDRAM Synchronous		170	250	ps
	$t_{jcyc-cyc1B}$[1]	V_T = 1.25 V CPU, SDRAM Asynchronous		124.5	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O=V_{DD}*(0.5)$	12	21	55	Ω
Output Impedance	R_{DSP1}[1]	$V_O=V_{DD}*(0.5)$	12	21	55	Ω
Output High Voltage	V_{OH2}	I_{OH} = -18 mA	2.4	3.3		V
Output Low Voltage	V_{OL2}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH2}	V_{OH} = 2.0 V		-62	-33	mA
Output Low Current	I_{OL2}	V_{OL} = 0.8 V	38	43		mA
Rise Time[1]	t_{r2}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.62	2.2	ns
Fall Time[1]	t_{f2}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.81	2.2	ns
Duty Cycle[1]	d_{t2}	V_T = 1.5 V	45	49.8	55	%
Skew[1]	t_{sk2}	V_T = 1.5 V		200	500	ps
Jitter, Cycle-to-cycle	t_{jcyc2}	V_T = 1.5 V	-350	306	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O=V_{DD}*(0.5)$	10	17	20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O=V_{DD}*(0.5)$	10	18	20	Ω
Output High Voltage	V_{OH3}	I_{OH} = -25 mA	2.4	2.9		V
Output Low Voltage	V_{OL3}	I_{OL} = 20 mA		0.32	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-73	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41	50		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.14	2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.38	2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	47	51.8	57	%
$Skew^1_{(0\text{-}1,2,4,5,7,10,11)}$	T_{sk1}	V_T = 1.5 V		155.5	250	ps
$Skew^1_{(0\text{-}6,6,8,9,12,13)}$	T_{sk1}	V_T = 1.5 V		298.5	500	ps
Jitter, Cycle-to-cycle	t_{jcyc}	V_T = 1.5 V		369.17	650	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz, REF_0

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%; C_L = 30 pF

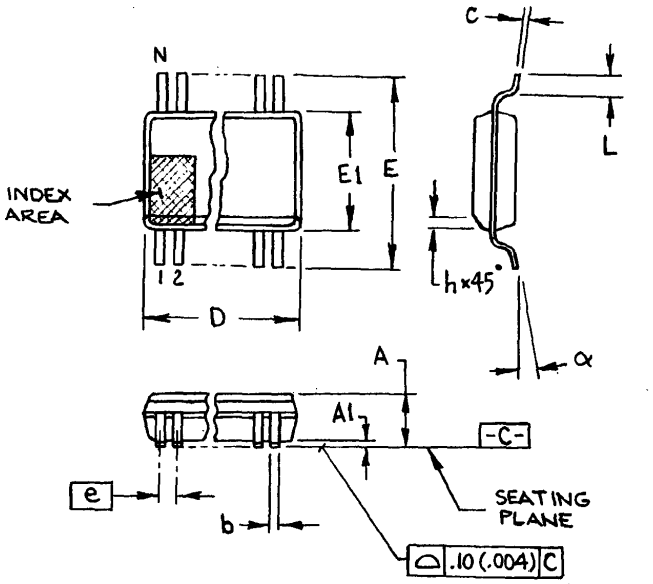
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O=V_{DD}*(0.5)$	12	21	55	Ω
Output Impedance	R_{DSP1}[1]	$V_O=V_{DD}*(0.5)$	12	21	55	Ω
Output High Voltage	V_{OH2}	I_{OH} = -18 mA	2.4	3.3		V
Output Low Voltage	V_{OL2}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH2}	V_{OH} = 2.0 V		-62	-22	mA
Output Low Current	I_{OL2}	V_{OL} = 0.8 V	16	57		mA
Rise Time[1] 48MHz	t_{r2}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.78	2	ns
Fall Time[1] 48MHz	t_{f2}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.92	2	ns
Duty Cycle[1] 48MHz	d_{t2}	V_T = 1.5 V	45	52	55	%
Rise Time[1] REF_0	tr2	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.32	2	ns
Fall Time[1] REF_0	t_{f2}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.56	2	ns
Duty Cycle[1] REF_0	dt2	V_T = 1.5 V	45	52.2	55	%
Jitter, 48MHz	t_{jcyc2}	V_T = 1.5 V		500.6	700	ps
Jitter, REF_0	tjcyc2	V_T = 1.5 V	-350	1243	1500	ps

Electrical Characteristics - REF_1;24/48MHz

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O=V_{DD}*(0.5)$ Output P	20	42	60	Ω
Output Impedance	R_{DSN5}1	$V_O=V_{DD}*(0.5)$ Output N	20	43	60	Ω
Output High Voltage	V_{OH4}	I_{OH} = -14 mA	2.4	2.6		V
Output Low Voltage	V_{OL4}	I_{OL} = 6mA		0.3	0.4	V
Output High Current	I_{OH4}	V_{OH} = 2.0 V		-26	-22	mA
Output Low Current	I_{OL4}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1] 24_48MHz	t_{r4}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.75	4	ns
Fall Time[1] 24_48MHz	t_{f4}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.88	4	ns
Duty Cycle[1] 24_48MHz	d_{t4}	V_T = 1.5 V	45	52	55	%
Rise Time[1] REF_1	t_{r4}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.22	4	ns
Fall Time[1] REF_1	t_{f4}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.43	4	ns
Duty Cycle[1] REF_1	d_{t4}	V_T = 1.5 V	45	51.1	55	%
Jitter, 24_48MHz	t_{jcyc4}	V_T = 1.5 V		727	1000	ps
Jitter, REF_1	t_{jcyc4}	V_T = 1.5 V	-1	1208	1500	ns

[1]Guaranteed by design, not 100% tested in production.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9248yF-135-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device