

### Frequency Generator & Integrated Buffers for Celeron & PII/III™

**Recommended Application:**  
810/810E type chipset.

**Output Features:**

- 2- CPUs @2.5V, up to 155MHz.
- 9 - SDRAM @ 3.3V, up to 155MHz.
- 8 - PCICLK @ 3.3V
- 1 - IOAPIC @ 2.5V,
- 2 - 3V66MHz @ 3.3V
- 2- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V
- 1- REF @3.3V, 14.318MHz.

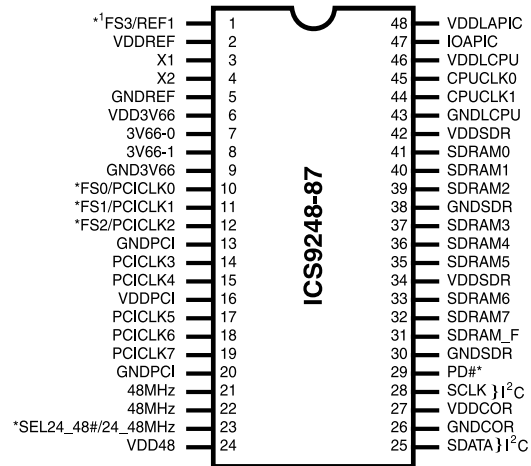
**Features:**

- Up to 155MHz frequency support
- Support FS0-FS3 strapping status bit for I<sup>2</sup>C read back.
- Support power management: Power down Mode from I<sup>2</sup>C programming.
- Spread spectrum for EMI control ( ± 0.25% center).
- Uses external 14.318MHz crystal

**Skew Specifications:**

- CPU – CPU: <175ps
- SDRAM - SDRAM: < 250ps
- 3V66 – 3V66: <175ps
- PCI – PCI: <500ps
- For group skew specification, please refer to group timing relationships table.

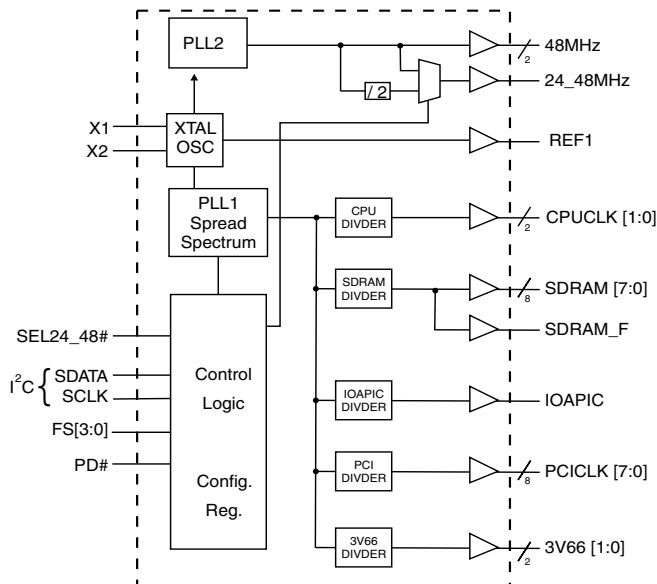
**Pin Configuration**



**48-Pin 300mil SSOP**

\*: These inputs have a 120K pull up to VDD.  
1: These are double strength.

**Block Diagram**



**Functionality**

FS3	FS2	FS1	FS0	CPU (MHz)	CPU/SDRAM	SDRAM (MHz)	3V66 (MHz)	PCICLK (3V66* 1/2) (MHz)	IOAPIC (PCI* 1/2) (MHz)	IOAPIC (PCI) (MHz)
0	0	0	0	83.3	1.00	83.3	55.48	27.74	13.87	27.74
0	0	0	1	124.00	1.00	124.00	82.67	41.33	20.67	41.33
0	0	1	0	155.00	1.00	155.00	103.33	51.67	25.83	51.67
0	0	1	1	143.96	1.33	108.00	72.00	36.00	18.00	36.00
0	1	0	0	70.00	0.67	105.00	70.00	35.00	17.50	35.00
0	1	0	1	112.00	1.00	112.00	74.67	37.33	18.67	37.33
0	1	1	0	150.00	1.00	150.00	100.00	50.00	25.00	50.00
0	1	1	1	140.00	1.33	105.00	70.00	35.00	17.50	35.00
1	0	0	0	68.33	0.67	102.50	68.33	34.17	17.08	34.17
1	0	0	1	107.00	1.00	107.00	71.33	35.67	17.83	35.67
1	0	1	0	138.00	1.00	138.00	92.00	46.00	23.00	46.00
1	0	1	1	137.33	1.33	103.00	68.67	34.34	17.17	34.34
1	1	0	0	66.80	0.67	100.20	66.80	33.40	16.70	33.40
1	1	0	1	100.30	1.00	100.30	66.80	33.40	16.70	33.40
1	1	1	0	133.60	1.00	133.60	89.07	44.53	22.27	44.53
1	1	1	1	133.60	1.33	100.20	66.80	33.40	16.70	33.40

## General Description

The **ICS9248-87** is the single chip clock solution for designs using 810/810E style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-87 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection.

## Power Groups

GNDREF, VDDREF = REF1, X1, X2  
 GNDPCI, VDDPCI = PCICLK [7:0]  
 GNDSDRAM, VDDSDRAM = SDRAM [8:0]  
 GND3V66, VDD3V66 = 3V66  
 VDD48 = 48MHz, 24MHz  
 GNDCOR, VDDCOR = supply for PLL core  
 VDDLAPIC = IOAPIC  
 GNDLCPU, VDDLCPU = CPUCLKL [1:0]

## Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF1	OUT	14.318 MHz reference clock.
	FS3	IN	Frequency select pin.
2, 6, 16, 24, 27, 34, 42	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output
3	X1	IN	Crystal input, nominally 14.318MHz.
4	X2	OUT	Crystal output, nominally 14.318MHz.
5, 9, 13, 20, 26, 30, 38	GND	PWR	Ground pin for 3V outputs.
8, 7	3V66 [1:0]	OUT	3V66 clock outputs.
10	FS0	IN	Frequency select pin.
	PCICLK0	OUT	PCI clock output.
11	FS1	IN	Frequency select pin.
	PCICLK1	OUT	PCI clock output.
12	FS2	IN	Frequency select pin.
	PCICLK2	OUT	PCI clock output.
19, 18, 17, 15, 14	PCICLK [7:3]	OUT	PCI clock outputs.
21, 22	48MHz	OUT	48MHz output clocks
23	SEL24_48#	IN	Sel pin for enabling 24MHz or 48MHz H=24MHz L=48MHz
	24_48MHz	OUT	Clock output for super I/O/USB
25	SDATA	IN	Data input for I2C serial input, 5V tolerant input
28	SCLK	IN	Clock input of I2C input, 5V tolerant input
29	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
31	SDRAM_F	OUT	SDRAM clock output - free running not affected by I <sup>2</sup> C
32, 33, 35, 36, 37, 39, 40, 41	SDRAM [7:0]	OUT	SDRAM clock outputs
43	GNDLCPU	PWR	Ground pin for the CPU clocks.
44, 45	CPUCCLK [1:0]	OUT	CPU clock outputs.
46	VDDLCPU	PWR	Power pin for the CPUCLKs. 2.5V
47	IOAPIC	OUT	2.5V clock output
48	VDDLAPIC	PWR	Power pin for the IOAPIC. 2.5V

## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only **"Block-Writes"** from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

## Serial Configuration Command Bitmap

Byte4: Functionality and Frequency Select Register (default = 0)

Bit	Description											PWD	
	Bit (2, 7:4)					CPUCLK (MHz)	CPU/ SDRAM	SDRAM (MHz)	3V66 (MHz)	PCICLK (MHz)	IOAPIC (MHz)		
											=PCI/2	=PCI	
Bit 2, Bit 7:4	0	0	0	0	0	83.3	1.00	83.3	55.48	27.74	13.87	27.74	00100 Note1
	0	0	0	0	1	124.00	1.00	124.00	82.67	41.33	20.67	41.33	
	0	0	0	1	0	155.00	1.00	155.00	103.33	51.67	25.83	51.67	
	0	0	0	1	1	143.96	1.33	108.00	72.00	36.00	18.00	36.00	
	0	0	1	0	0	70.00	0.67	105.00	70.00	35.00	17.50	35.00	
	0	0	1	0	1	112.00	1.00	112.00	74.67	37.33	18.67	37.33	
	0	0	1	1	0	150.00	1.00	150.00	100.00	50.00	25.00	50.00	
	0	0	1	1	1	140.00	1.33	105.00	70.00	35.00	17.50	35.00	
	0	1	0	0	0	68.33	0.67	102.50	68.33	34.17	17.08	34.17	
	0	1	0	0	1	107.00	1.00	107.00	71.33	35.67	17.83	35.67	
	0	1	0	1	0	138.00	1.00	138.00	92.00	46.00	23.00	46.00	
	0	1	0	1	1	137.33	1.33	103.00	68.67	34.34	17.17	34.34	
	0	1	1	0	0	66.80	0.67	100.20	66.80	33.40	16.70	33.40	
	0	1	1	0	1	100.30	1.00	100.30	66.80	33.40	16.70	33.40	
	0	1	1	1	0	133.60	1.00	133.60	89.07	44.53	22.27	44.53	
	0	1	1	1	1	133.60	1.33	100.20	66.80	33.40	16.70	33.40	
	1	0	0	0	0	145.00	1.00	145.00	96.67	48.33	24.17	48.33	
	1	0	0	0	1	140.00	1.00	140.00	93.33	46.67	23.33	46.67	
	1	0	0	1	0	136.00	1.00	136.00	90.67	45.33	22.67	45.33	
	1	0	0	1	1	130.00	1.00	130.00	86.67	43.33	21.67	43.33	
	1	0	1	0	0	129.00	1.00	129.00	86.00	43.00	21.50	43.00	
	1	0	1	0	1	127.00	1.00	127.00	84.67	42.33	21.17	42.33	
	1	0	1	1	0	121.00	1.00	121.00	80.67	40.33	20.17	40.33	
	1	0	1	1	1	119.00	1.00	119.00	79.33	39.67	19.83	39.67	
	1	1	0	0	0	117.00	1.00	117.00	78.00	39.00	19.50	39.00	
	1	1	0	0	1	114.00	1.00	114.00	76.00	38.00	19.00	38.00	
	1	1	0	1	0	110.00	1.00	110.00	73.33	36.67	18.33	36.67	
	1	1	0	1	1	105.00	1.00	105.00	70.00	35.00	17.50	35.00	
	1	1	1	0	0	75.33	0.67	113.00	75.33	37.67	18.83	37.67	
	1	1	1	0	1	153.33	1.33	115.00	76.67	38.33	19.17	38.33	
	1	1	1	1	0	150.63	1.33	113.00	75.33	37.67	18.83	37.67	
	1	1	1	1	1	146.63	1.33	110.00	73.33	36.67	18.33	36.67	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4											0	
Bit 1	0 - Normal 1 - Spread Spectrum Enabled $\pm$ 0.25% Center Spread											1	
Bit 0	0 - Running 1 - Tristate all outputs											0	

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

- 1) All entries selectable through I<sup>2</sup>C. Entries 1 -16 are also selectable through FS pins.
- 2) The IOAPIC Frequency change from IOAPIC=PCICLK/2 to IOAPIC=PCICLK is controlled by IOAPC\_Freq control in I<sup>2</sup>C Byte 3 Bit 1, default is IOAPIC=PCICLK/2.
- 3) Read back code of PWD shows revision ID.

I<sup>2</sup>C is a trademark of Philips Corporation

**Byte 0: Control Register Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved
Bit6	-	0	Reserved
Bit5	-	0	Reserved
Bit4	-	0	Reserved
Bit3	-	0	Reserved
Bit2	23	1	24/48MHz
Bit1	21,22	1	48MHz
Bit0	-	0	Reserved

**Byte 1: SDRAM, Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	32	1	SDRAM7
Bit6	33	1	SDRAM6
Bit5	35	1	SDRAM5
Bit4	36	1	SDRAM4
Bit3	37	1	SDRAM3
Bit2	39	1	SDRAM2
Bit1	40	1	SDRAM1
Bit0	41	1	SDRAM0

**Byte 2: PCI, Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	19	1	PCICLK7
Bit6	18	1	PCICLK6
Bit5	17	1	PCICLK5
Bit4	15	1	PCICLK4
Bit3	14	1	PCICLK3
Bit2	12	1	PCICLK2
Bit1	11	1	PCICLK1
Bit0	10	1	PCICLK0

**Byte 3: Reserved , Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved
Bit6	-	X	FS2#
Bit5	-	X	FS1#
Bit4	-	X	FS0#
Bit3	-	1	IOAPIC
Bit2	-	X	(SEL24_48#)#
Bit1	-	1	FREQ_IOAPIC =1=>IOAPIC=PCICLK/2 FREQ_IOAPIC=0=> IOAPIC= PCICLK
Bit0	-	X	FS3#

**Byte 5: Peripheral , Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved
Bit6	-	0	Reserved
Bit5	-	0	Reserved
Bit4	-	0	Reserved
Bit3	-	0	Reserved
Bit2	-	0	Reserved
Bit1	-	0	Reserved
Bit0	-	0	Reserved

**Byte 6: Peripheral , Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.
3. SDRAM\_F is free running and cannot be turned off by I<sup>2</sup>C

**Note: Don't write into this register, writing into this register can cause malfunction**

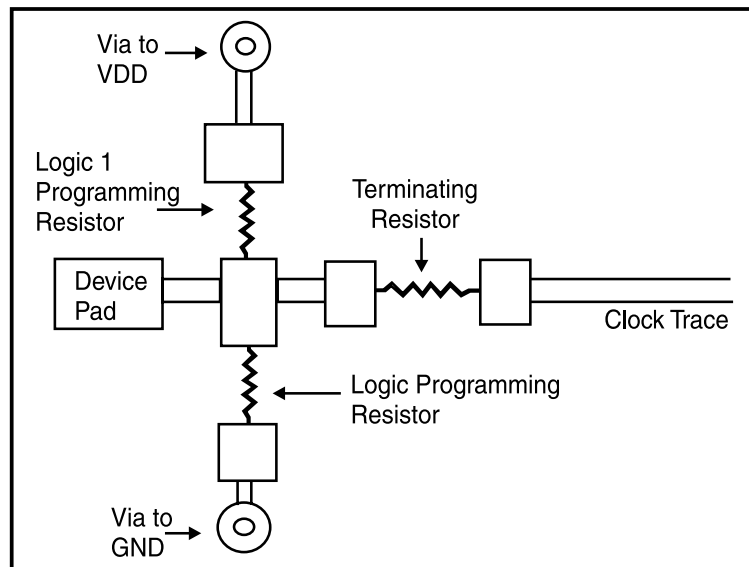
## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9248-87** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).



**Fig. 1**

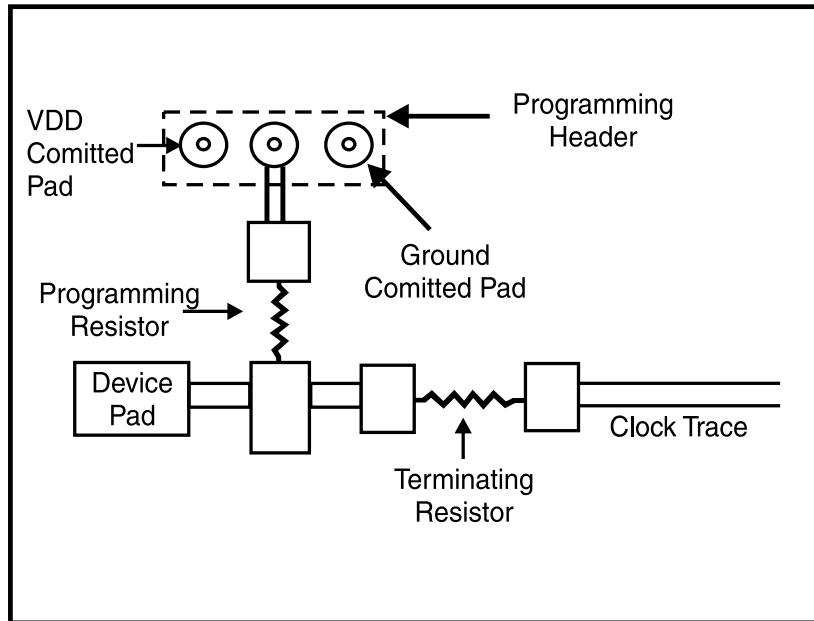


Fig. 2a

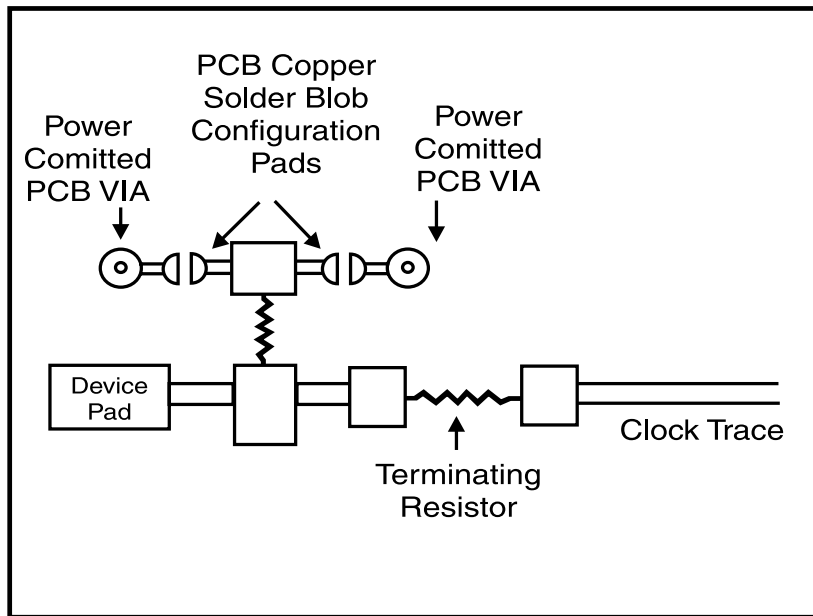


Fig. 2b

## PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI\_STOP# and CPU\_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-87 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



## Absolute Maximum Ratings

Core Supply Voltage .....	4.6 V
I/O Supply Voltage .....	3.6V
Logic Inputs .....	GND-0.5 V to V <sub>DD</sub> +0.5 V
Ambient Operating Temperature .....	0°C to +70°C
Storage Temperature .....	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Group Timing Relationship Table

Group	CPU 66MHz		CPU 100MHz		CPU 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V ±5%, VDDL=2.5 V ±5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2		V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>		V <sub>SS</sub> -0.3		0.8	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-5		5	μA
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5	2.0		μA
Input Low Current	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-200	-100		μA
Operating Supply Current	I <sub>DD3.3OP</sub>	C <sub>L</sub> = 0 pF; Select @ 66M		60	100	mA
Power Down Supply Current	I <sub>DD3.3PD</sub>	C <sub>L</sub> = 0 pF; With input address to V <sub>DD</sub> or GND		400	600	μA
Input frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V;		14.318		MHz
Pin Inductance	L <sub>pin</sub>				7	nH
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	Logic Inputs			5	pF
	C <sub>out</sub>	Out put pin capacitance			6	pF
	C <sub>INX</sub>	X1 & X2 pins	27		45	pF
Transition Time <sup>1</sup>	T <sub>trans</sub>	To 1st crossing of target Freq.			3	mS
Settling Time <sup>1</sup>	T <sub>s</sub>	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization <sup>1</sup>	T <sub>STAB</sub>	From V <sub>DD</sub> = 3.3 V to 1% target Freq.			3	mS
Delay	t <sub>PZH</sub> , t <sub>PZH</sub>	output enable delay (all outputs)	1		10	nS
	t <sub>PLZ</sub> , t <sub>PZH</sub>	output disable delay (all outputs)	1		10	nS

<sup>1</sup>Guarenteed by design, not 100% tested in production.

## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$ ,  $V_{DD} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP2B}^1$	$V_O = V_{DD}^*(0.5)$	13.5		45	$\Omega$
Output Impedance	$R_{DSN2B}^1$	$V_O = V_{DD}^*(0.5)$	13.5		45	$\Omega$
Output High Voltage	$V_{OH2B}$	$I_{OH} = -1 \text{ mA}$	2			V
Output Low Voltage	$V_{OL2B}$	$I_{OL} = 1 \text{ mA}$			0.4	V
Output High Current	$I_{OH2B}$	$V_{OH@MIN} = 1.0 \text{ V}$ , $V_{OH@MAX} = 2.375 \text{ V}$	-27		-27	mA
Output Low Current	$I_{OL2B}$	$V_{OL@MIN} = 1.2 \text{ V}$ , $V_{OL@MAX} = 0.3 \text{ V}$	27		30	mA
Rise Time	$t_{r2B}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$	0.4		1.6	ns
Fall Time	$t_{f2B}^1$	$V_{OH} = 0.4 \text{ V}$ , $V_{OL} = 2.0 \text{ V}$	0.4		1.6	ns
Duty Cycle	$d_{l2B}^1$	$V_T = 1.25 \text{ V}$	45	50	55	%
Skew	$t_{sk2B}^1$	$V_T = 1.25 \text{ V}$			175	ps
Jitter	$t_{jeye-eye}^1$	$V_T = 1.25 \text{ V}$			250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10-30 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP1}^1$	$V_O = V_{DD}^*(0.5)$	12		55	$\Omega$
Output Impedance	$R_{DSN1}^1$	$V_O = V_{DD}^*(0.5)$	12		55	$\Omega$
Output High Voltage	$V_{OH1}$	$I_{OH} = -1 \text{ mA}$	2.4			V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 1 \text{ mA}$			0.55	V
Output High Current	$I_{OH1}$	$V_{OH@MIN} = 1.0 \text{ V}$ , $V_{OH@MAX} = 3.135 \text{ V}$	-33		-33	mA
Output Low Current	$I_{OL1}$	$V_{OL@MIN} = 1.95 \text{ V}$ , $V_{OL@MAX} = 0.4$	30		38	mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$	0.5		2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$	0.5		2	ns
Duty Cycle	$d_{l1}^1$	$V_T = 1.5 \text{ V}$	45		55	%
Skew	$t_{sk1}^1$	$V_T = 1.5 \text{ V}$			175	ps
Jitter	$t_{jeye-eye}$	$V_T = 1.5 \text{ V}$			500	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP4B}^1$	$V_O = V_{DD}^*(0.5)$	9		30	$\Omega$
Output Impedance	$R_{DSN4B}^1$	$V_O = V_{DD}^*(0.5)$	9		30	$\Omega$
Output High Voltage	$V_{OH4B}$	$I_{OH} = -5.5 \text{ mA}$	2			V
Output Low Voltage	$V_{OL4B}$	$I_{OL} = 9.0 \text{ mA}$			0.4	V
Output High Current	$I_{OH4B}$	$V_{OH@MIN} = 1.0 \text{ V}$ , $V_{OH@MAX} = 2.375 \text{ V}$	-27		-27	mA
Output Low Current	$I_{OL4B}$	$V_{OL@MIN} = 1.2 \text{ V}$ , $V_{OL@MAX} = 0.3 \text{ V}$	27		30	mA
Rise Time	$t_{r4B}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$	0.4		1.6	ns
Fall Time	$t_{f4B}^1$	$V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$	0.4		1.6	ns
Duty Cycle	$d_{t4B}^1$	$V_T = 1.25 \text{ V}$	45		55	%
Jitter	$t_{j\text{cyc-cyc}}$	$V_T = 1.25 \text{ V}$			500	ps
Skew	$T_{sk4}^1$				250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 20 - 30 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP3}^1$	$V_O = V_{DD}^*(0.5)$	10		24	$\Omega$
Output Impedance	$R_{DSN3}^1$	$V_O = V_{DD}^*(0.5)$	10		24	$\Omega$
Output High Voltage	$V_{OH3}$	$I_{OH} = -1 \text{ mA}$	2.4			V
Output Low Voltage	$V_{OL3}$	$I_{OL} = 1 \text{ mA}$			0.4	V
Output High Current	$I_{OH3}$	$V_{OH@MIN} = 2.0 \text{ V}$ , $V_{OH@MAX} = 3.135 \text{ V}$	-54		-46	mA
Output Low Current	$I_{OL3}$	$V_{OL@MIN} = 1.0 \text{ V}$ , $V_{OL@MAX} = 0.4 \text{ V}$	54		53	mA
Rise Time	$T_{r3}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$	0.4		1.6	ns
Fall Time	$T_{f3}^1$	$V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$	0.4		1.6	ns
Duty Cycle	$D_{t3}^1$	$V_T = 1.5 \text{ V}$	45		55	%
Skew	$T_{sk3}^1$	$V_T = 1.5 \text{ V}$			250	ps
Jitter	$t_{j\text{cyc-cyc}}$	$V_T = 1.5 \text{ V}$			250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10\text{-}30 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP1}^1$	$V_O = V_{DD}^*(0.5)$	12		55	$\Omega$
Output Impedance	$R_{DSN1}^1$	$V_O = V_{DD}^*(0.5)$	12		55	$\Omega$
Output High Voltage	$V_{OH1}$	$I_{OH} = -1 \text{ mA}$	2.4			V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 1 \text{ mA}$			0.55	V
Output High Current	$I_{OH1}$	$V_{OH@MIN} = 1.0 \text{ V}$ , $V_{OH@MAX} = 3.135 \text{ V}$	-33		-33	mA
Output Low Current	$I_{OL1}$	$V_{OL@MIN} = 1.95 \text{ V}$ , $V_{OL@MAX} = 0.4$	30		38	mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$	0.5		2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$	0.5		2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.5 \text{ V}$	45		55	%
Skew	$t_{sk1}^1$	$V_T = 1.5 \text{ V}$			500	ps
Jitter	$t_{jeyc\text{-}eyc}$	$V_T = 1.5 \text{ V}$			500	ps

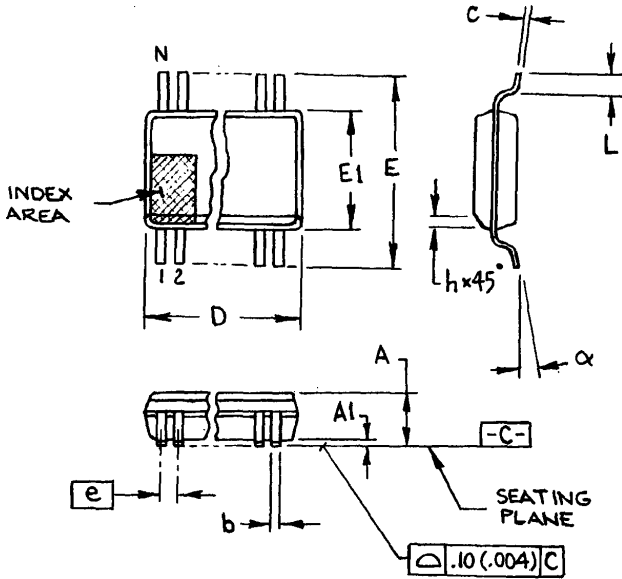
<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF, 48MHz\_0 (Pin 25)

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP5}^1$	$V_O = V_{DD}^*(0.5)$	20		60	$\Omega$
Output Impedance	$R_{DSN5}^1$	$V_O = V_{DD}^*(0.5)$	20		60	$\Omega$
Output High Voltage	$V_{OH5}$	$I_{OH} = 1 \text{ mA}$	2.4			V
Output Low Voltage	$V_{OL5}$	$I_{OL} = -1 \text{ mA}$			0.4	V
Output High Current	$I_{OH5}$	$V_{OH@MIN} = 1 \text{ V}$ , $V_{OH@MAX} = 3.135 \text{ V}$	-29		-23	mA
Output Low Current	$I_{OL5}$	$V_{OL@MIN} = 1.95 \text{ V}$ , $V_{OL@MAX} = 0.4 \text{ V}$	29		27	mA
Rise Time	$t_{r5}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$		1.8	4	nS
Fall Time	$t_{f5}^1$	$V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$		1.7	4	nS
Duty Cycle	$d_{t5}^1$	$V_T = 1.5 \text{ V}$	45		55	%
Jitter	$t_{jeyc\text{-}eyc}^1$	$V_T = 1.5 \text{ V}$ ; Fixed Clocks			500	pS
	$t_{jeyc\text{-}eyc}^1$	$V_T = 1.5 \text{ V}$ ; Ref Clocks			1000	pS
Skew	$T_{sk}$	$V_T = 1.5 \text{ V}$			250	pS

<sup>1</sup>Guaranteed by design, not 100% tested in production.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

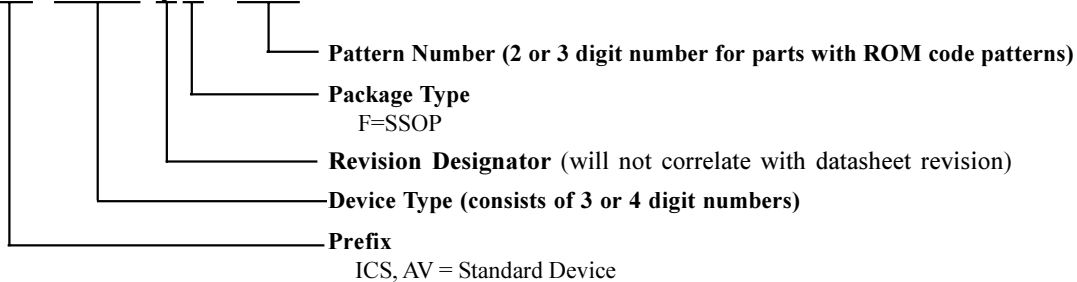
JEDEC MO-118  
DOC# 10-0034  
6/1/00  
REV B

Ordering Information

ICS9248yF-87

Example:

ICS XXXX y F - PPP



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(Rev.1.0 Mar 2020)

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